

S.A. Distributor

ELECTRONIC BUILDING ELEMENTS (PTY) LTD
PURVEYORS OF ALL ELECTRONIC COMPONENTS

Telephone 78-9221/6
P.O. Box 4609, Pretoria
Telex 3-0181 SA

Pine Square Berea Street
(2nd Floor) Hazelwood
Pretoria

B-SERIES CMOS

INTEGRATED CIRCUITS



quantum electronics

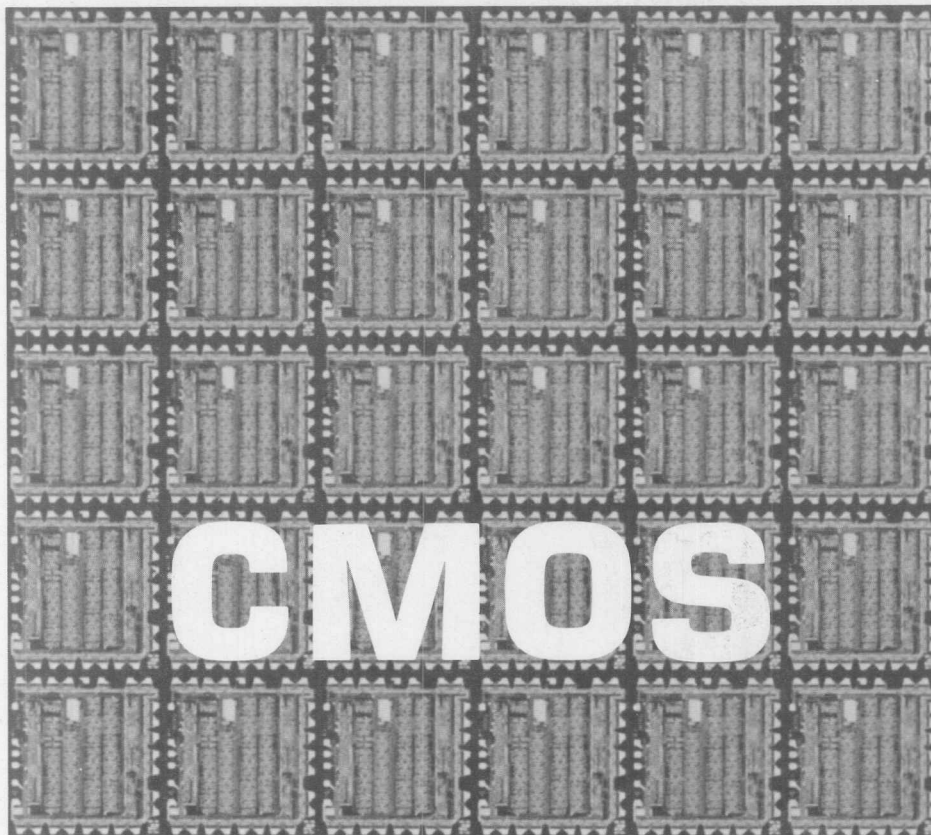
Box 391262

Bramley

SOLID STATE SCIENTIFIC INC.

MONTGOMERYVILLE, PA. 18936 • (215) 855-8400

TWX 510-661-7267



SOLID STATE SCIENTIFIC INC.

MONTGOMERYVILLE, PA. 18936 • (215) 855-8400

TWX 510-661-7267

NOVEMBER, 1976

Solid State Scientific has been a leading supplier of high-performance CMOS Integrated Circuits since 1969. In addition to the family of standard commercial and military products described in this book, Solid State Scientific also maintains product lines in CMOS memories, CMOS timekeeping circuits, and RF power and small-signal transistors.

This book presents complete technical data for the SCL4000 Series of CMOS Integrated Circuits. Detailed design information and family characteristic data provide a foundation for effectively utilizing the individual device data sheets. Selector guides and cross-reference information are included to simplify the task of implementing system design efficiently and economically. Reliability screening programs, both military and commercial, are presented; these programs offer a variety of screening levels designed to maximize the reliability/cost ratio as a function of system performance requirements.

CMOS

SOLID STATE SCIENTIFIC, INC.

MONTGOMERYVILLE, PA 18936 • (717) 853-8400

TELEX 210-681-1281



NOVEMBER, 1973

Solid State Scientific has been a leading supplier of high-performance CMOS integrated circuits since 1968. In addition to the family of standard commercial and military products described in this book, Solid State Scientific also maintains product lines in CMOS memories, CMOS timing circuits, and RF power and signal transistors. This book presents complete technical data for the SCL-4000 Series of CMOS integrated circuits. Detailed design information and family characteristics data provide a foundation for effectively utilizing the individual device data.

Solid State Scientific reserves the right to make changes in the circuitry or specifications in this book at any time without notice.

Information furnished by Solid State Scientific is believed to be accurate and reliable. However, no responsibility is assumed by Solid State Scientific for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Solid State Scientific.

Solid State Scientific, Inc. Montgomeryville Industrial Center, Montgomeryville, PA, USA 18936

INDEX TO PRODUCT DATA SHEETS

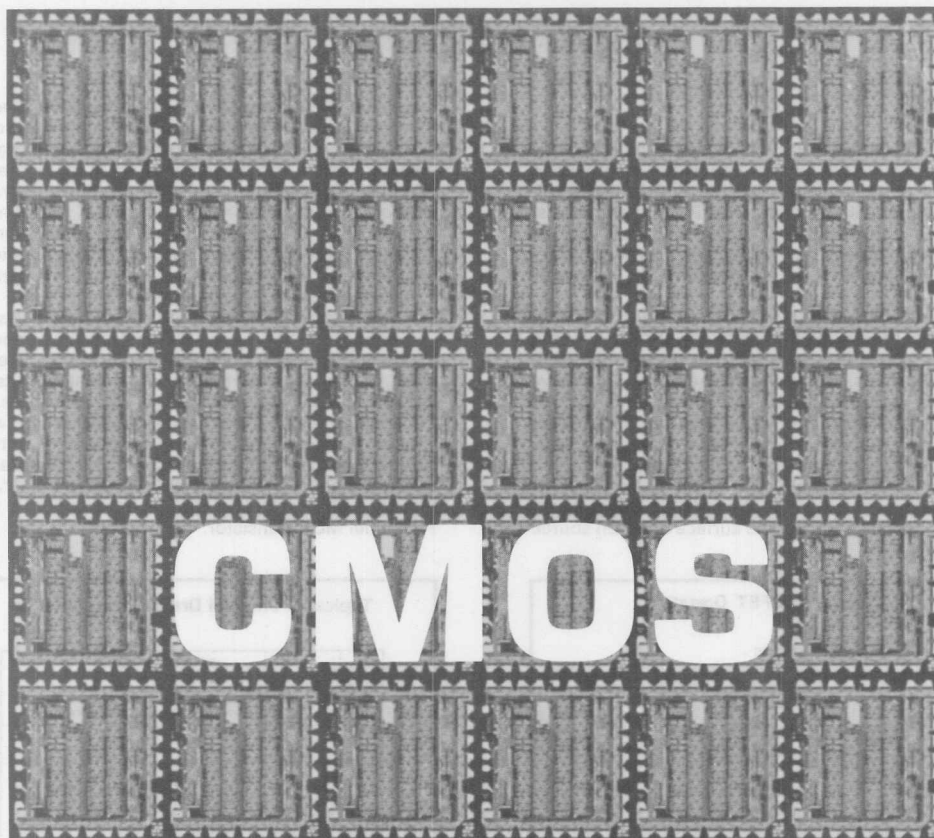
To simplify data reference, data sheets are arranged as nearly as possible in numerical sequence of device type numbers. Because some data sheets include more than one part type, however, some types may be out of sequence.

NUMERICAL DEVICE INDEX

DEVICE		PAGE
SCL4000B	Dual 3-Input NOR Gate and Inverter	52
SCL4001B	Quad 2-Input NOR Gate	54
SCL4001UB	Quad 2-Input NOR Gate (Unbuffered)	56
SCL4002B	Dual 4-Input NOR Gate	54
SCL4006AB	18-Stage Shift Register	59
SCL4007UB	Dual Complementary Pair and Inverter	61
SCL4008B	Four-Bit Full Adder	64
SCL4009UB	Hex Inverting Buffer/Level Shifter	68
SCL4010B	Hex Non-Inverting Buffer/Level Shifter	68
SCL4011B	Quad 2-Input NAND Gate	71
SCL4011UB	Quad 2-Input NAND Gate (Unbuffered)	73
SCL4012B	Dual 4-Input NAND Gate	71
SCL4013B	Dual D-Type Flip-Flop	76
SCL4014B	8-Stage Parallel-Input/Serial-Output Shift Register	78
SCL4015B	Dual 4-Stage Serial-Input/Parallel-Output Shift Register	80
SCL4016AB	Quad Analog Switch	82
SCL4017AB	Decade Counter w/10 Decoded Outputs	88
SCL4018B	Presetable Divide-by-N Counter	93
SCL4019B	Quad AND-OR Select Gate	96
SCL4020AB	14-Stage Binary Counter	98
SCL4021B	8-Stage Parallel-Input/Serial-Output Shift Register	101
SCL4022AB	Binary Counter w/8 Decoded Outputs	104
SCL4023B	Triple 3-Input NAND Gate	71
SCL4024B	7-Stage Binary Counter	109
SCL4025B	Triple 3-Input NOR Gate	54
SCL4026AB	Decade Counter w/7-Segment Outputs	112
SCL4027B	Dual JK-Type Flip-Flop	117
SCL4028B	BCD-to-Decimal Decoder	119
SCL4029B	Presetable Up/Down Binary/Decade Counter	122
SCL4030B	Quad 2-Input Exclusive-OR Gate	126
SCL4033AB	Decade Counter w/7-Segment Outputs	112
SCL4034AB	8-Stage Universal Bus Register	128
SCL4035B	4-Stage Parallel-Input/Parallel-Output Shift Register	133
SCL4040AB	12-Stage Binary Counter	136
SCL4041UB	Quad True/Complement Buffer	139
SCL4042B	Quad Clocked Latch	143
SCL4043AB	Quad NOR-Type R/S Latch w/3-State Outputs	145
SCL4044AB	Quad NAND-Type R/S Latch w/3-State Outputs	145
SCL4046B	Phase-Locked Loop	148
SCL4049UB	Hex Inverting Buffer/Level Shifter	156
SCL4050B	Hex Non-Inverting Buffer/Level Shifter	156
SCL4051B	8-Channel Analog Multiplexer/Demultiplexer	159
SCL4052B	Differential 4-Channel Analog Multiplexer/Demultiplexer	159
SCL4053B	Triple 2-Channel Analog Multiplexer/Demultiplexer	159
SCL4060AB	14-Stage Binary Counter and Oscillator	164
SCL4066B	Quad Analog Switch	168
SCL4068B	8-Input NAND Gate	71
SCL4069UB	Hex Inverter	173
SCL4070B	Quad 2-Input Exclusive-OR Gate	175
SCL4071B	Quad 2-Input OR Gate	177

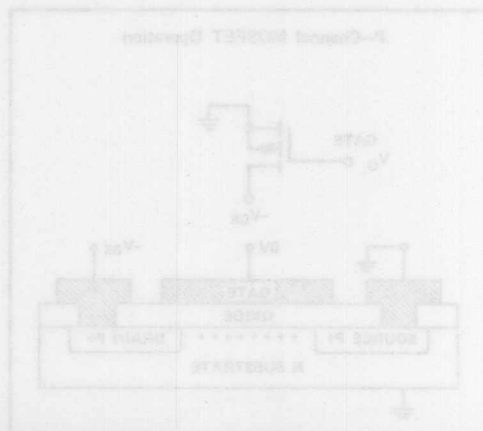
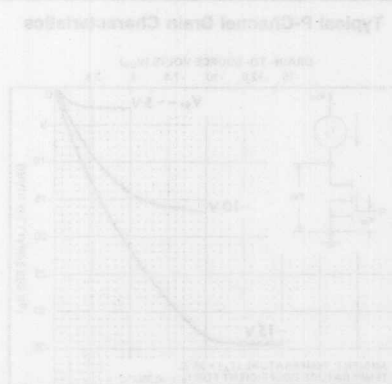
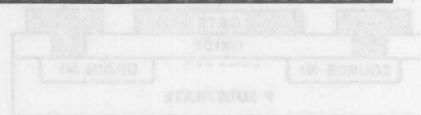
NUMERICAL DEVICE INDEX (Continued)

DEVICE		PAGE
SCL4072B	Dual 4-Input OR Gate	177
SCL4073B	Triple 3-Input AND Gate	184
SCL4075B	Triple 3-Input OR Gate	177
SCL4076B	4-Bit D-Type Register w/3-State Outputs	179
SCL4077B	Quad 2-Input Exclusive-NOR Gate	182
SCL4078B	8-Input NOR Gate	54
SCL4081B	Quad 2-Input AND Gate	184
SCL4082B	Dual 4-Input AND Gate	184
SCL4093B	Quad 2-Input NAND Schmitt Trigger	186
SCL4160B	BCD Decade Counter w/Asynchronous Clear	189
SCL4161B	4-Stage Binary Counter w/Asynchronous Clear	189
SCL4162B	BCD Decade Counter w/Synchronous Clear	189
SCL4163B	4-Stage Binary Counter w/Synchronous Clear	189
SCL4402B	Dual 4-Input Expandable NOR Gate	194
SCL4404B	8-Stage Binary Counter	196
SCL4412B	Dual 4-Input Expandable NAND Gate	194
SCL4416AB	Quad Analog Switch	198
SCL4426AB	Decade Counter w/7-Segment Driver Outputs	202
SCL4428B	Binary-to-Octal Decoder	207
SCL4433AB	Decade Counter w/7-Segment Driver Outputs	202
SCL4441UB	Quad Buffer/Driver	210
SCL4445B	21-Stage Frequency Divider and Oscillator	212
SCL4446B	Phase-Locked Loop	148
SCL4449UB	Hex Inverter	215
SCL4502B	Hex Strobed Inverting Buffer w/3-State Outputs	217
SCL4508B	Dual 4-Bit Latch w/3-State Outputs	219
SCL4510B	BCD Decade Programmable Up/Down Counter	222
SCL4511B	BCD-to-7 Segment Latch/Decoder/Driver	226
SCL4512B	8-Channel Data Selector	229
SCL4514B	4-to-16 Line Decoder with Latch (Active High Outputs)	233
SCL4515B	4-to-16 Line Decoder with Latch (Active Low Outputs)	233
SCL4516B	4-Stage Binary Programmable Up/Down Counter	236
SCL4518B	Dual BCD Decade Up Counter	240
SCL4520B	Dual 4-Stage Binary Up Counter	240
SCL4522B	BCD Decade Programmable Down Counter	243
SCL4526B	4-Stage Binary Programmable Down Counter	243
SCL4527B	BCD Rate Multiplier	247
SCL4528B	Dual Monostable Multivibrator	251
SCL4531B	12-Bit Parity Tree	255
SCL4543B	BCD-to-7 Segment Latch/Decoder/Driver	257
SCL4555B	Dual 2-to-4 Line Decoder (Active High Outputs)	260
SCL4556B	Dual 2-to-4 Line Decoder (Active Low Outputs)	260
SCL4581B	4-Bit Arithmetic Logic Unit	263
SCL4582B	Look-Ahead Carry Block	267
SCL4585B	4-Bit Magnitude Comparator	269



CMOS

CMOS FUNDAMENTALS



CMOS FUNDAMENTALS

MOS DEVICES

Complementary MOS (CMOS) logic, memory, and switching circuits are constructed with P-channel and N-channel enhancement-mode MOS transistors diffused on a monolithic silicon chip. Field-effect transistors are unipolar devices; that is, their operation is based on a function of only one type of charge carrier — holes in P-channel types, and electrons in N-channel types.

A simplified cross-section of an N-channel enhancement-mode MOS transistor is shown in Figure 1. This transistor is a four-terminal device. In CMOS logic applications, the substrate and the source are usually connected to a common point, which in the N-channel transistor is the most negative potential or V_{SS} . With no voltage applied between gate and source, the two N+ diffusions are electrically isolated from each other and no conduction occurs. As an increasingly positive voltage is applied to the gate, an N-type inversion layer begins to form at the surface between source

and drain. When a threshold voltage V_{TN} is reached, the inversion layer just begins to connect source and drain, allowing some conduction. As the gate voltage increases further, the inversion layer is driven deeper, resulting in greater conductivity from source to drain. A saturation point is reached when $+V_{DS}$ is forced higher than $V_G - V_{TN}$; the device, therefore, is self-current-limiting. Figure 2 shows typical drain characteristics for an N-channel MOS transistor. Note the similarity to equivalent vacuum tube characteristics.

Operation of the P-channel device (Figure 3) is similar, except that the source and substrate are connected to the most positive potential, V_{DD} . A P-type inversion layer, or channel, is formed when a negative voltage is applied to the gate with respect to the source. The threshold voltage V_{TP} is defined as that value of V_G which causes a specified minimum conductivity between source and drain. Saturation occurs when the drain-to-source voltage V_{DS} is forced more negative than $V_G - V_{TN}$. Figure 4 shows typical drain characteristics for a P-channel MOS transistor.

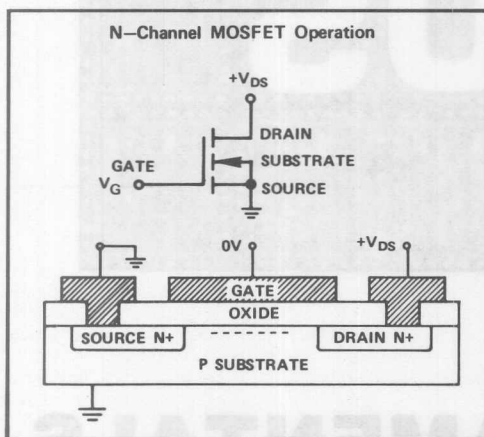


Figure 1

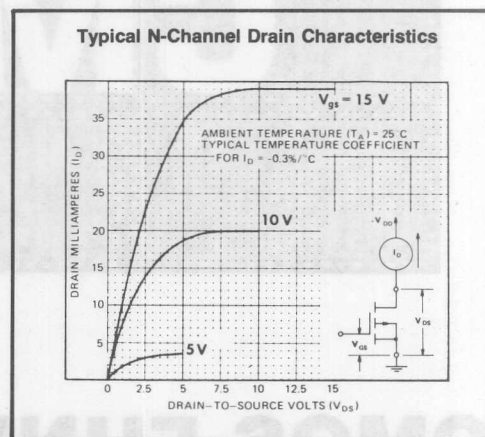


Figure 2

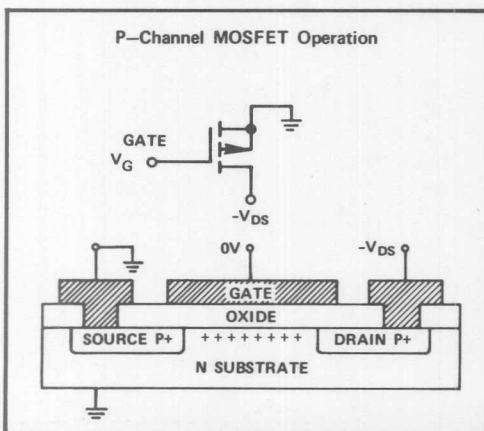


Figure 3

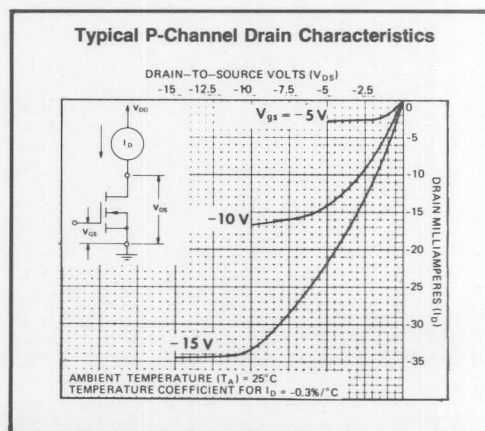


Figure 4

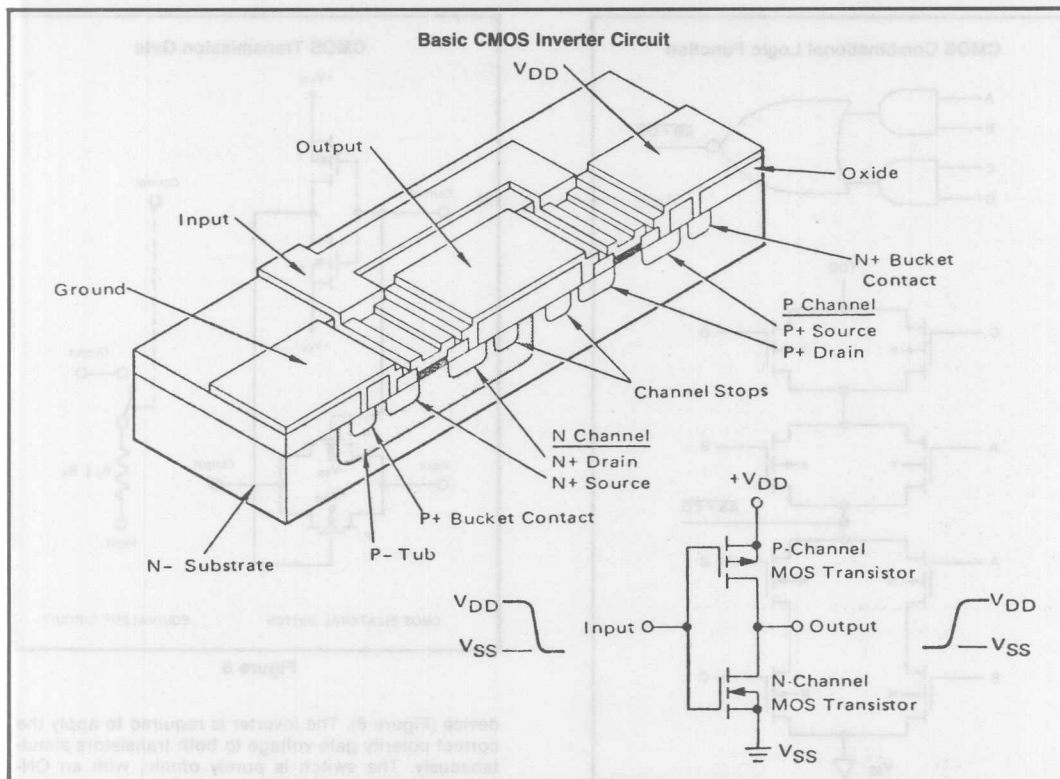


Figure 5

A major feature of the metal oxide semiconductor is the very high input resistance resulting from the dielectric oxide isolation between the gate and the channel. The input resistance is virtually unaffected by the polarity of the gate bias. Also, whatever leakage current does exist between gate and source is relatively independent of ambient temperature variations.

CMOS DEVICES

Complementary MOS logic circuits employ both P-channel and N-channel enhancement-mode MOS transistors. They have opposite, or complementary, switching characteristics and can therefore be used as virtually ideal switching components. Consider the implementation shown in Figure 5. The circuit consists of one P-channel device and one N-channel device. Note that to form the N-channel device, a P-doped "tub" must be created into which the device is placed. "Channel stops" must also be placed between the P-tub and the P-drain to prevent parasitic channeling effects.

When a positive voltage V_{DD} is applied at the input, the P-channel switches off and the N-channel switches on. Thus, the output is connected to V_{SS} through the low on-resistance of the N-channel device. Alternatively, applying V_{SS} to the input turns off the N-channel and turns on the P-channel. In this state, the output is connected to V_{DD} through the equivalent on-resistance of the P-channel device. Therefore, an input voltage of V_{DD} results in an output voltage of V_{SS} , and an input voltage of V_{SS} results in an output voltage of V_{DD} . The circuit is a simple digital inverter.

Gates

Any logic function capable of being constructed with ideal switches can be implemented in CMOS. Adding a parallel P-channel device and a series N-channel device to the basic inverter transforms the circuit into a positive-logic 2-input NAND gate (Figure 6). Adding a parallel N-channel and a series P-channel device instead transforms the inverter into a 2-input NOR gate.

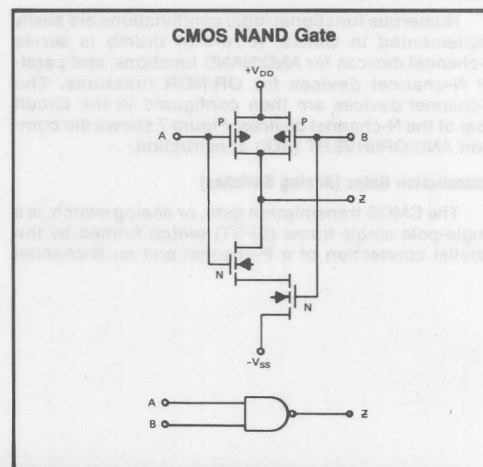


Figure 6

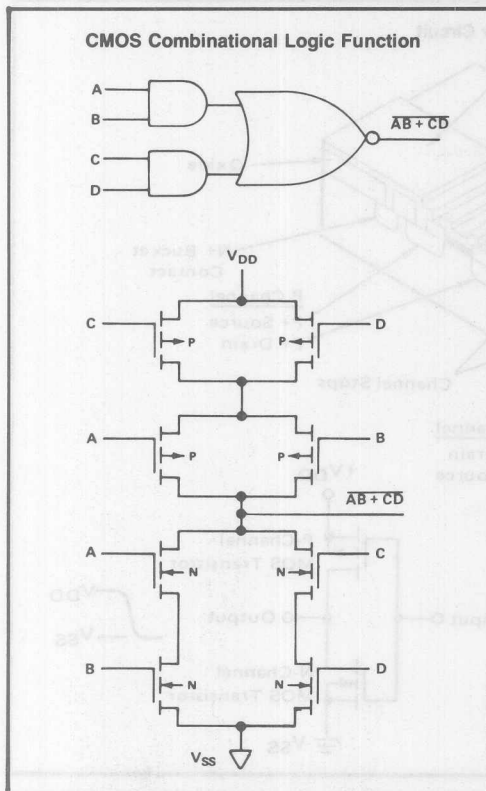


Figure 7

Note that in each circuit there exists no DC path from V_{DD} to V_{SS} : if a connection is made to V_{SS} through the N-channels, a corresponding P-channel blocks the connection to V_{DD} ; alternatively, if the P-channels are on, then a corresponding N-channel is off. Therefore, very low power dissipation results without sacrificing low output impedance.

Combinational Logic

Numerous functional logic combinations are easily implemented in CMOS. A rule of thumb is series N-channel devices for AND/NAND functions, and parallel N-channel devices for OR/NOR functions. The P-channel devices are then configured in the circuit dual of the N-channel devices. Figure 7 shows the common AND/OR/INVERT (AOI) construction.

Transmission Gates (Analog Switches)

The CMOS transmission gate, or analog switch, is a single-pole single-throw (SPST) switch formed by the parallel connection of a P-channel and an N-channel

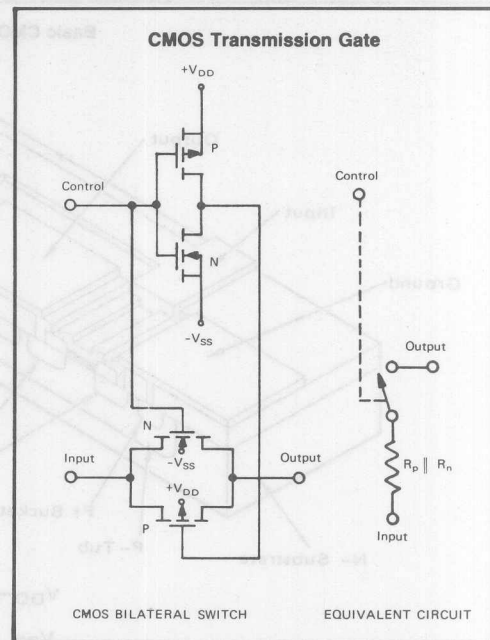


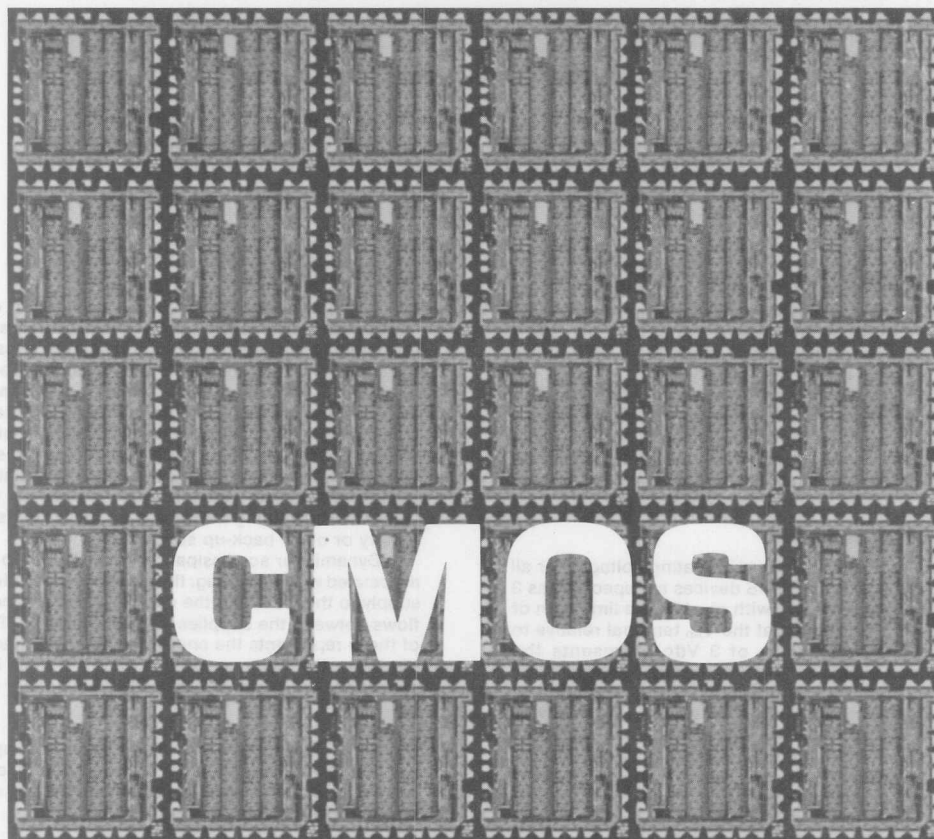
Figure 8

device (Figure 8). The inverter is required to apply the correct polarity gate voltage to both transistors simultaneously. The switch is purely ohmic, with an ON-resistance of about 200 - 400 Ω and OFF-resistance typically about $10^{11}\Omega$. There is no offset voltage across the switch. These characteristics approach those of the ideal switch ($R_{ON} = 0$, $R_{OFF} = \infty$). A single-transistor switch results in a source-follower circuit in which gate cut-off occurs and limits the load to charge only to within one threshold of the gate. When two complementary devices are operated in parallel, one of the two channels is always being operated as a drain-loaded stage, permitting a low-impedance path for all switched signal voltages.

The transmission gate is useful in digital applications as well. Combinational logic functions can be implemented, and the device provides a simple method for constructing 3-state (bussed) systems.

SCL4000 SERIES DEVICES

Using basic CMOS techniques, Solid State Scientific has developed the SCL4000 Series Family of building block elements and complex functions. Devices numbered SCL40xx and SCL45xx are equivalents to industry 40xx and 45xx types. The designation SCL44xx indicates proprietary devices; they are usually variations on standard 40xx devices, making them more suitable for specific applications.



CMOS

DESIGN INFORMATION

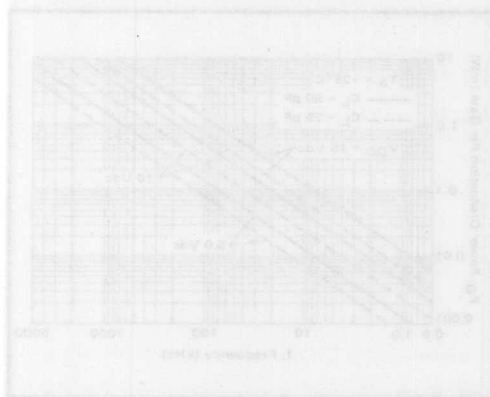


Fig. 2 — Transfer characteristics

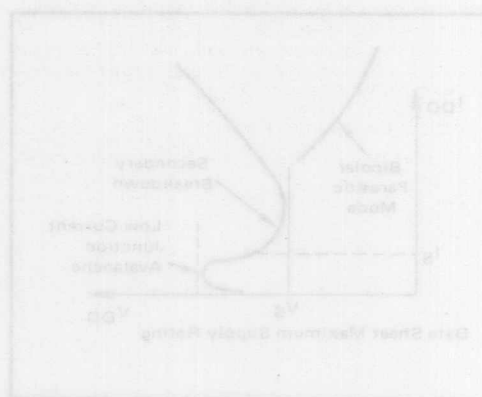


Fig. 3 — Secondary breakdown characteristics

CMOS DESIGN CONSIDERATIONS

This section is presented as an aid to the systems designer in proper application and use of CMOS devices. Areas such as power supply techniques and dissipation characteristics, thermal factors, operating considerations, interfacing parameters, and ac fan-out are covered in some detail.

POWER SUPPLY CONSIDERATIONS

CMOS offers the designer several important advantages over other technologies:

1. wide operating voltage range
2. very low power dissipation
3. constant switching threshold voltage ratio

These advantages permit operation from unregulated supplies, simplify filtering requirements, and eliminate the need for cooling equipment. In addition, battery-operated systems, either stand-alone or back-up, are feasible.

OPERATING VOLTAGE RANGE

Minimum and maximum operating voltages for all Solid State Scientific CMOS devices are specified as 3 and 15 Vdc, respectively, with an absolute limitation of -0.5 and 18 Vdc, applied at the V_{DD} terminal relative to V_{SS} . The minimum value of 3 Vdc represents the maximum expected value of either P-channel or N-channel transistor threshold voltages. Operation at lower voltages may, therefore, prevent half of the device from turning on. The absolute limitation of -0.5 Vdc merely prevents the internal device junctions from becoming forward-biased; the circuit is obviously non-operational under this condition.

The maximum value prevents avalanche of these internal junctions. While the 18 Vdc restriction on low-current avalanche is somewhat conservative, there is the possibility of on-chip current transients turning on the parasitic bipolar transistors inherent in CMOS construction. The chip can enter secondary breakdown because these transients can easily exceed the 10 - 50 mA sustaining current required. The result is a short circuit reflected at the supply and catastrophic device failure (see Figure 1).

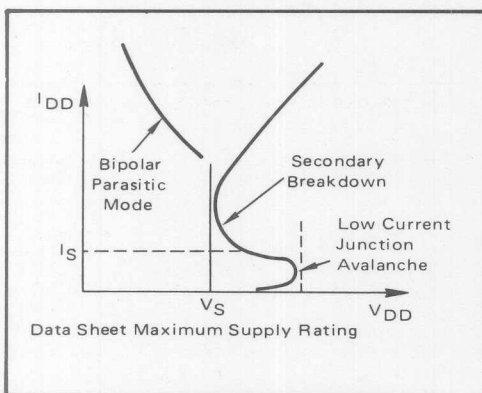


Fig. 1 — Secondary breakdown characteristics

POWER DISSIPATION

The quiescent, or DC, power dissipation component consists normally of only leakage currents across reverse-biased diode junctions. This is true because, in the quiescent state, there exists no direct path between V_{DD} and V_{SS} other than these leakages, which are typically in the nanoampere region. In reality, certain surface effects will contribute to the quiescent dissipation. These factors have been taken into account in specifying the worst-case values given in the individual device data sheets; these values should be used by the designer in determining the necessary capacity of standby battery or other back-up supplies.

Dynamic, or ac, dissipation consists of two factors associated with switching: the power delivered from the supply to the load, and the current which momentarily flows between the supplies during switching. The first of these represents the energy required to charge and discharge the load capacitance (plus the small internal capacitances). The energy stored by a capacitor is given by:

$$E_s = \frac{1}{2} CV^2$$

Since CMOS outputs switch from supply to supply, and the load capacitance is both charged and discharged once each cycle of the output frequency f , this component of power dissipation is given by:

$$P_D = \frac{2E_s}{t} = C_L V_{DD}^2 f \quad (V_{SS} = 0 \text{ Vdc})$$

Note that this component increases linearly with load capacitance C_L , operating frequency f , and the square of the operating voltage V_{DD} . Figure 2 shows this functional dependence for a typical CMOS gate.

The Figure assumes input rise and fall times of 20ns. As these transition times increase, however, cur-

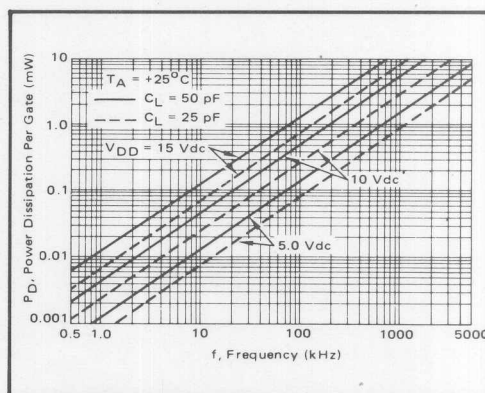


Fig. 2 — Typical gate power dissipation characteristics

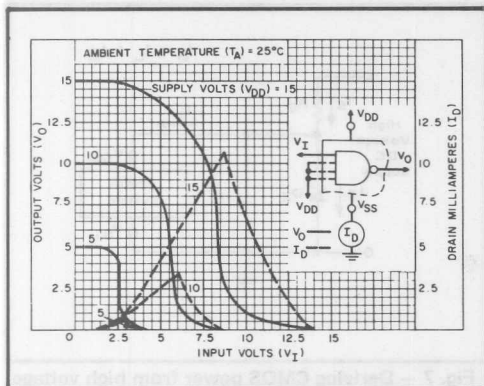


Fig. 3 — Typical current and voltage transfer characteristics

rent flows between the supplies because both P-channel and N-channel transistors are biased on momentarily. This through-current is a complex function of fabrication parameters, device geometries, operating voltage, temperature, rise and fall times, and operating frequency. A typical waveform of through-current I_{TC} in relation to voltage transfer characteristics is shown in Figure 3.

Power dissipation due to through-current can be shown to be proportional to the factors described above in the following way:

$$P_{TC} \propto f(t_r + t_f)V_{DD}^3$$

where the constant of proportionality is dependent upon device parameters.

The relationship between supply current I_{DD} and I_{SS} , load capacitance, and input rise and fall time is illustrated in Figure 4.

The waveforms (a) show I_{DD} , I_{SS} , and the through-current I_{TC} for a load capacitance of 15pF and t_r , t_f of 10μs. The smaller of the I_{DD} and I_{SS} pulses represents the maximum through-current of the device. The slight amplitude differences between pulses represent the current delivered to the load. The magnitude of the through-current pulses in (a) is used as the standard for (b) and (c).

The input rise and fall times are decreased to 400ns in (b). Here again, the smaller current pulses represent through-current, which has somewhat decreased from (a). Note that since the width of the current pulse has also decreased, the magnitude of the current delivered to the 15pF load has increased (to deliver the same charge).

Load capacitance in (c) is increased to 65pF, and input transition times decreased to 40ns. Through-current pulses have virtually disappeared, except for the current charging and discharging internal capacitance. The magnitude of the load current, however, has increased due to the increased load and narrower current pulse width.

All complex CMOS functional devices employ buffered inputs to minimize the through-current effects described here. Caution is urged when using high-current buffers and unbuffered gates in conjunction with large loads and high operating voltages; long input rise and fall times may cause the device power dissipation restriction to be exceeded.

REGULATION AND BATTERY OPERATION

The wide operating voltage range and constant switching voltage ratio of CMOS permit use of simple unregulated supplies, as shown in Figure 5.

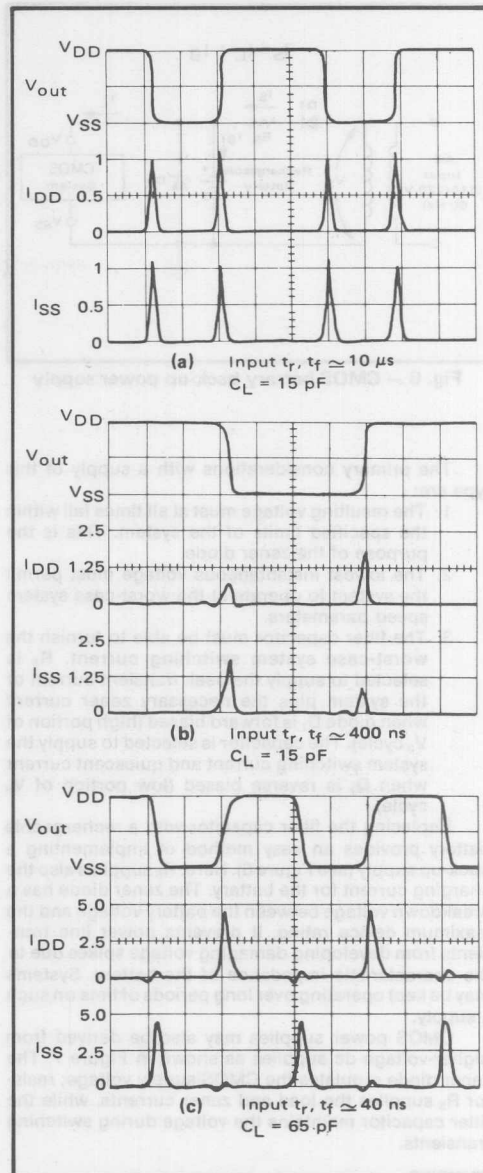


Fig. 4 — Switching current waveforms

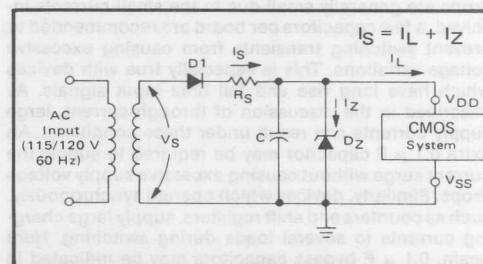


Fig. 5 — CMOS unregulated power supply

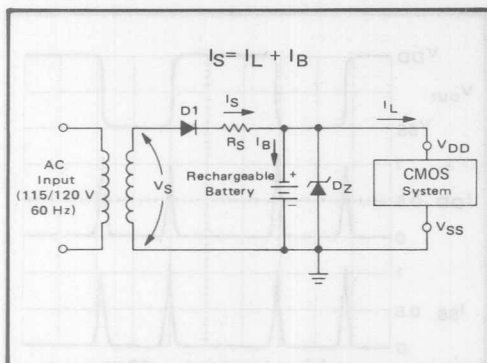


Fig. 6 — CMOS battery back-up power supply

The primary considerations with a supply of this type are:

1. The resulting voltage must at all times fall within the specified limits of the system. This is the purpose of the zener diode.
2. The lowest instantaneous voltage must permit the system to operate at the worst-case system speed parameters.
3. The filter capacitor must be able to furnish the worst-case system switching current. R_S is selected to supply the peak transient current of the system plus the necessary zener current when diode D_1 is forward biased (high portion of V_S cycle). The capacitor is selected to supply the system switching current and quiescent current when D_1 is reverse biased (low portion of V_S cycle).

Replacing the filter capacitor with a rechargeable battery provides an easy method of implementing a back-up supply (see Figure 6). Here, R_S supplies also the charging current for the battery. The zener diode has a breakdown voltage between the battery voltage and the maximum device rating. It prevents power line transients from developing damaging voltage spikes due to the characteristic impedance of the battery. Systems may be kept operating over long periods of time on such a supply.

CMOS power supplies may also be derived from higher-voltage dc supplies as shown in Figure 7. The zener diode regulates the CMOS supply voltage; resistor R_S supplies the load and zener currents, while the filter capacitor maintains the voltage during switching transients.

FILTERING

Most CMOS systems require less filtering on supply busses than other logic families. While V_{DD} and V_{SS} line drops are generally small due to the small currents involved, a few capacitors per board are recommended to prevent switching transients from causing excessive voltage variations. This is especially true with devices which have long rise and fall time input signals. As described in the discussion of through-current, large supply currents can result under these conditions. An extra $0.1 \mu F$ capacitor may be required to supply the current surge without causing excessive supply voltage drops. Similarly, devices which operate synchronously, such as counters and shift registers, supply large charging currents to several loads during switching. Here again, $0.1 \mu F$ bypass capacitors may be indicated in such cases.

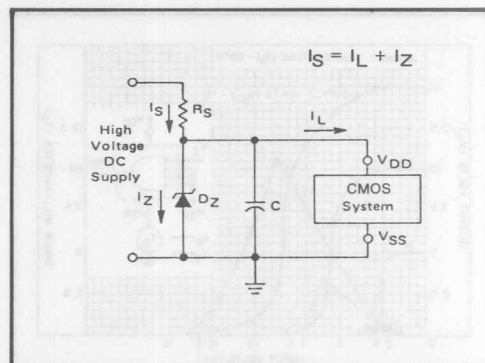


Fig. 7 — Deriving CMOS power from high voltage DC source

THERMAL FACTORS

Transfer characteristics of CMOS devices exhibit excellent stability over temperature. This feature allows the ambient temperature range of CMOS devices to be a function of package type. This section discusses techniques of thermal management and the variation of device characteristics with temperature.

THERMAL MANAGEMENT

Circuit performance and long-term reliability are maximized at low junction temperatures. Power dissipation is the common source of heat in any system; the negligible power consumed in the quiescent state in CMOS circuits is a major factor in maintaining performance and reliability. In general, operation at moderate speeds and voltages does not require consideration of the package dissipation restriction of 300 mW. In high-frequency, high-voltage, large-load, or analog applications, however, these considerations become important.

The average junction temperature is a function of device power dissipation and the ability of the packaging system to remove the generated heat. This is expressed in the following formula:

$$T_J = T_A + P_D (\Theta_{JA})$$

where T_J = junction temperature

T_A = ambient temperature

P_D = calculated power dissipation

Θ_{JA} = thermal resistance, junction-to-ambient

Worst-case and typical values of Θ_{JA} for common IC package types in still air and without heat sinking are shown in the table:

Package Type	$\Theta_{JA} (^{\circ}\text{C}/\text{watt})$	
	Typ	Max
Epoxy B Dual-in-line 14- or 16-lead	135	200
Cerdip Dual-in-line 14- or 16-lead	100	155
Epoxy B Dual-in-line 24-lead	95	140
Ceramic Dual-in-line 24-lead	70	100

These figures should be consulted in cases where there is reason to believe that device dissipation may be excessive.

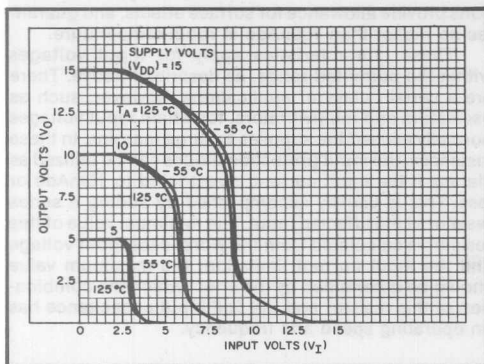


Fig. 8 — Typical inverter voltage transfer characteristics as a function of temperature

PARAMETRIC THERMAL VARIATION

All operational parameters vary to some degree with temperature. Since CMOS devices may be used over very wide temperature ranges, the designer should be familiar with the effects of these thermal variations. They fall into three categories: transfer characteristics, leakage current, and channel resistance effects.

1. Transfer Characteristics

Figure 8 illustrates the negligible variation in transfer voltage over the entire military temperature range. This results from the tendency of P-channel and N-channel transistor threshold voltages to track together. Under similar conditions, a bipolar device threshold may vary more than 40%. This feature makes threshold-dependent circuits such as oscillators and multi-vibrators feasible in systems with a wide range of operating temperature.

2. Leakage Current

As expected, since device leakage current is normally leakage across reverse-biased silicon junctions, temperature variation of this parameter follows the traditional diode leakage characteristic, i.e., approximately doubling with each 11°C rise in temperature.

3. Channel Resistance

Such parameters as output drive current (I_{OH} , I_{OL}), switching through-current (I_{TC}), propagation delays (t_{PLH} , t_{PHL}), and output transition times (t_{TLH} , t_{THL}) are direct effects of channel resistance. These parameters vary as channel resistance varies—0.3%/°C. Current characteristics decrease with increasing temperature at this rate; this factor is employed in specifying low- and high-temperature limits for these parameters on device data sheets. Switching parameters increase at this rate with temperature; this dependence must be considered by the designer in order to guarantee system dynamic performance over temperature.

INPUT RATINGS

The high impedance of a CMOS input results from the insulating oxide between the gate and the channel. This high impedance coupled with the 5pF input capacitance make CMOS inputs excellent energy storage nodes, allowing buildup of large voltages. Input diode protection networks are used, therefore, to conduct excess energy to the supply rails, thus protecting the gate regions from damage. These diodes affect certain device operations, as described in the following discussion of general input characteristics.

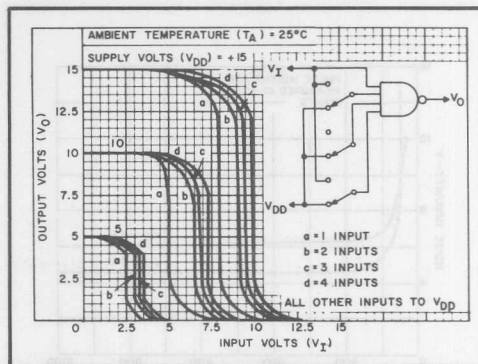


Fig. 9 — Typical multiple-input switching transfer characteristics for conventional 4-input NAND gate

INPUT VOLTAGE RANGE

Input signals should never exceed the range from 0.5 Vdc more negative than V_{SS} to 0.5 Vdc more positive than V_{DD} . This prevents forward biasing the input diodes, with the attendant possibility of entering a latch-up mode due to high-current transients. Further details may be found in the preceding discussion of "Power Supply Considerations" and later on in this section.

NOISE IMMUNITY

Noise immunity as specified in CMOS data sheets refers to the worst-case input voltage levels which will maintain guaranteed output conditions and will not produce a change in logic state. Specifically, the data sheets specify the minimum input high-level voltage (V_{IH}) and maximum input low-level voltage (V_{IL}) which guarantee an output voltage of no lower than 90% of V_{DD} or no higher than 10% of V_{DD} under no-load conditions ($|I_O| < 1\mu A$). Since the switching threshold voltage of a CMOS inverter is typically 50% of the supply and fairly sharp, and output voltages are close to the supplies, these input voltages tend to be symmetric and close to the ideal situation of 50% noise immunity. In fact, V_{IH} is typically 55% of V_{DD} , and V_{IL} is 45% of V_{DD} . (Note: the older designations of V_{NH} and V_{NL} can be related to V_{IH} and V_{IL} by the following:

$$\begin{aligned} V_{NH} &= V_{DD} - V_{IH}(\min) \\ V_{NL} &= V_{IL}(\max) - V_{SS} \end{aligned}$$

Worst-case specifications under these output voltage requirements are 20% of V_{DD} for the conventional SSI devices (Note: the older 30% noise immunity specification allowed much greater output voltage variations). This specification can be greatly improved by making the transfer voltage characteristic sharper, i.e., increasing device gain. In 1970, Solid State Scientific developed the technique of buffering gate outputs for increased gain; since that time, all CMOS gates in the SCL4000 series have been buffered. The industry began to realize the superiority of this structure for digital logic applications only with the recent agreement on "B" series CMOS.

Buffered outputs become even more important in maintaining noise immunity with the variation in transfer voltage with input pattern on multiple input gates. Figure 9 shows the typical range in switching voltage for a conventional 4-input NAND gate. Observe that $V_{IH}(\min)$ degrades as a function of the number of inputs switching. This pattern sensitivity is reversed for NOR

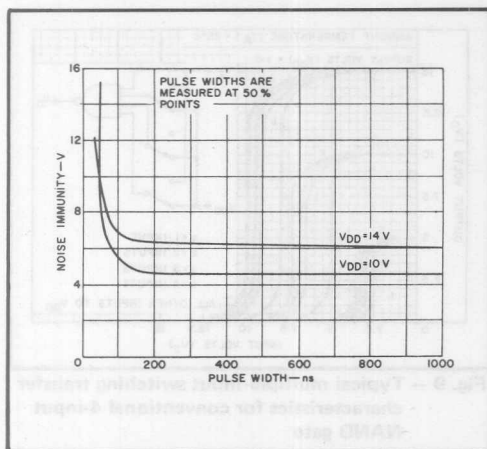


Fig. 10 — Typical signal-line noise-immunity

gate types. Buffering the device outputs, although the variations in switching voltage are unaffected, maintains greater noise immunity over all input conditions resulting from the much more nearly ideal transfer characteristic. Further improvement is attained by the requirement that CMOS gate structures consist of no more than three inputs per section; this decreases the variation in switching voltage, as compared with the 4-input gate in Figure 9. There are many other advantages to the buffered-gate concept. Each one is fully discussed in following sections.

Note that Solid State Scientific specifies and measures noise immunity under worst-case input combinations. This factor gives the designer a more realistic description of device operation, in view of the above discussion.

Noise immunity specifications refer to input signals; however, a similar discussion applies to noise introduced on power and ground lines. CMOS devices are sensitive only to negative power line transients and positive ground line transients. The magnitude of power- and ground-line noise immunity approaches that of signal-line noise immunity because of the close tracking of output voltage with supply in either state.

The relatively slow response times of CMOS devices tend to act as a noise filter: extremely short spikes of greater magnitude than the dc noise immunity limits are prevented from propagating through the device. A typical example of dc noise immunity is shown in Figure 10.

Another source of noise introduction into CMOS devices is crosstalk from high noise voltages coupled through small capacitances. Since CMOS devices have much higher output impedance than equivalent TTL types, they are much more sensitive to such capacitively-coupled noise. The designer should consult the individual device data sheets to determine the magnitude of current which will pull a CMOS output into the threshold region of the driven CMOS inputs, and use good interconnection techniques to prevent this type of crosstalk from interfering with system operation.

INPUT CURRENT

The high input impedance of CMOS results in an input current of typically 10pAdc. Worst-case specifica-

tions provide allowance for surface effects, and guarantee no higher than 100nAdc at room temperature.

These characteristics apply for input voltages within the permitted range, as described above. There are a certain class of applications, however, such as oscillators and multivibrators, for which input voltages normally exceed the supplies by large margins. In these instances, the input protection diodes can be utilized as clamps if the input current is restricted to 10mAdc or less. This is usually accomplished by adding a series resistor at the affected input. The minimum value of this resistor is calculated from the worst-case input voltage and the input current limitation; the maximum value should be determined by the effect which the combination of this resistor and the 5pF input capacitance has on operating speed and frequency.

UNUSED INPUTS

If a CMOS input is left unterminated, it can acquire unpredictable voltages through coupling with stray external capacitances and internal crosstalk. Since these voltages are normally within the supply range, the input protection diodes cannot conduct away this accumulated energy. Since both P- and N-channel transistors spend significant time in their "on" states, both power dissipation and device noise immunity degrade. Even catastrophic failure can result from these conditions. Therefore, all inputs should be connected to an appropriate supply voltage, or to another driven CMOS input. If a portion of a device is not loaded, its inputs must also be properly terminated.

INPUT WAVEFORMS

The maximum input rise and fall time specification for sequential circuits is typically in the 3 μ s to 15 μ s range, depending on supply voltage. This prevents ambiguous logic states and false clocking due to switching voltage variations and skew problems. Power dissipation also increases as logic elements spend more time in the switching region.

When sequential circuits are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the transition times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitive load. If setup and hold times are specified on device data sheets, they must also be taken into account.

Schmitt trigger constructions may be indicated to bring rise and fall times within indicated bounds.

INPUT PROTECTION NETWORKS

Because the gate oxide of a CMOS transistor has extremely high resistance, even a very-low-energy source (such as a static charge) is capable of developing the breakdown voltage of approximately 100V. This results in permanent damage to the device. Therefore, gate protection structures are employed to conduct excess energy away from the gate region. These structures, however, are only capable of protecting from overvoltages of less than 1000V. While this is normally sufficient for in-system transients, device handling can produce overvoltages of one or two orders of magnitude greater. Handling precautions are recommended when using CMOS devices. Some suggested procedures appear in the section entitled "Handling Precautions for CMOS Devices".

The input protection structure utilized on SCL4000 Series devices is shown in the diagram of a typical

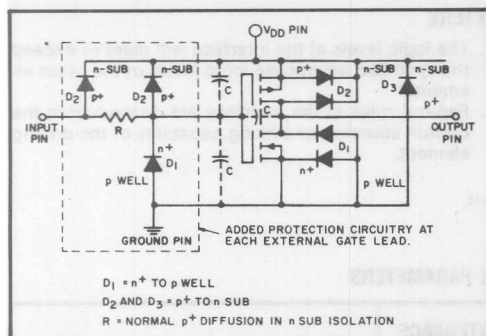


Fig. 11 — Gate-oxide protection circuit used in SCL4000 integrated circuits

CMOS device in Figure 11. The circuit consists of diodes D1 and D2, which clamp the input voltage to V_{SS} and V_{DD} , respectively, and series resistor R, whose nominal value is 1.5K Ω . Avalanche voltages of the diodes are well below the breakdown voltage of the gate oxide. The resistor provides a small delay with the 5pF input capacitance which allows excess energy to be conducted away before reaching the gate region.

When the diodes are used as clamps for oscillators, multivibrators, etc., input current must be limited to less than 10mA to protect against both possible latchup and long-term degradation due to metal migration.

In a system power-up or power-down sequence, power must be applied to the device before the introduction of low-impedance driving signals. This sequence must also be maintained while troubleshooting systems where devices or modules must be removed from or inserted into a system.

OUTPUT CHARACTERISTICS

The amount of current which a CMOS output is capable of sinking or sourcing is a function of the channel impedance of the driving structure. These characteristics vary with voltage and temperature; these variations were discussed previously. Transistor characteristics are illustrated on most device data sheets.

BUFFERED OUTPUTS

Consider the conventional CMOS 2-input NAND gate structure of Figure 12. Since the N-channel devices are in series, their on-resistance must be decreased (larger chip area) to hold the output low impedance (or sink current parameter) within specification. As the number of gate inputs increases, even larger N-channel transistors are required. Also, since the P-channel de-

vices are connected in parallel, the output high impedance (and, therefore source current) is a function of input pattern, i.e., the number of devices turned on. Solid State Scientific gates have buffered outputs: small geometry logic transistors are used to generate the required function, while only one large P-channel and one large N-channel device form the output. This technique reduces chip size; in addition, output impedance is no longer a function of input pattern. This means that dc and ac fanout are constant, and the user need not concern himself with several sets of loading requirements for each device.

OUTPUT LOADING

Since CMOS outputs driving CMOS inputs switch essentially from supply to supply while the driven inputs draw very little current (typically 10 pAdc), dc fanout can usually be ignored, except in bus-oriented systems. Of much greater importance is ac fanout, discussed below. However, several precautions are necessary to prevent damaging the output structure.

The outputs of most CMOS devices consist of a complementary pair. This structure prohibits the connection of outputs in a "wire-OR" configuration. Three-state output devices should be used to achieve this configuration. It is possible, however, to parallel inputs and outputs of devices to provide increased drive. This practice should be restricted to devices within the same package to avoid current hogging.

Note that because of the negative temperature coefficient of MOS transistors, there is built-in short-term burn-out protection. In general, devices with standard output characteristics may be shorted to the supply rails at low operating voltages. Precautions are necessary with higher voltages and/or high-current buffers, in which saturation currents can cause the maximum dissipation limitation to be exceeded.

CMOS drive capability is limited if the outputs are required to maintain a specified logic level. However, if the output is used to drive a discrete device such as a transistor or LED, large currents (within maximum ratings) can be achieved by operating the device in the saturated region.

The output impedance of a CMOS device can be employed as an effective means of providing delay and integrator functions when loaded with a capacitor. However, in any application which places a sizable capacitive load on a CMOS output, care must be taken to prevent damaging transient currents when power is removed. If the capacitive load is charged when the power supply is removed, the diode from the output to the supply (output D2 in Figure 11) forms the discharge path as it becomes forward biased. Series resistance should be added to the output in order to prevent discharge currents above 1mA.

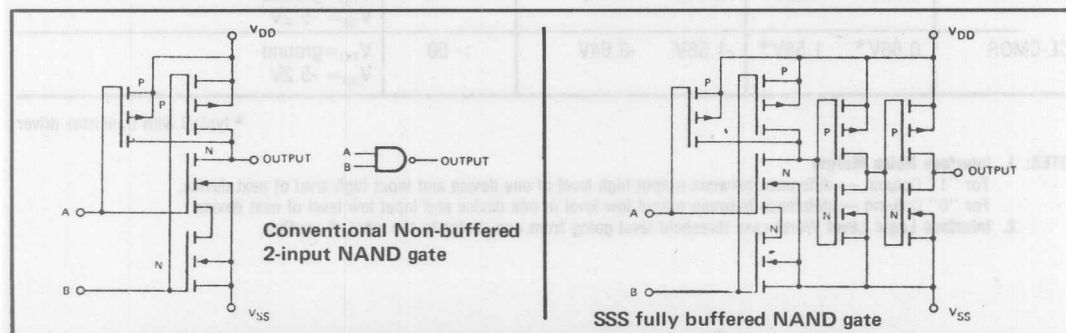


Figure 12

INTERFACE PARAMETERS

Table I provides interface parameters between CMOS and other logic families under the following conditions:

1. The power-supply voltage level and tolerances are chosen to accommodate the interfaced elements, since CMOS devices will operate over a much wider range.

2. The logic levels at the interface will meet or exceed the specified worst-case logic levels of the other elements.
3. Fan-out rules at the interface are derived from the current sourcing or sinking capability of the driving element.

TABLE I. CMOS INTERFACE PARAMETERS

INTERFACE	INTERFACE NOISE MARGIN "1" "0"		INTERFACE LOGIC LEVELS "1" "0"		INTERFACE MAXIMUM FAN OUT	REMARKS
CMOS-CMOS	1.5V	1.5V	3.5V	1.5V	> 50	5-volt system
	3.0V	3.0V	7.0V	3.0V	> 50	10-volt system
	4.0V	4.0V	11.0V	4.0V	> 50	15-volt system
CMOS-TTL/DTL	2.5V	0.4V	2.0V	0.8V	2	Buffers only
TTL/DTL-CMOS	1.1V	1.1V	3.5V	1.5V	See Remarks	2K Ω pull-up resistor for TTL or open-collector DTL. Fan-out determined by dynamic requirements
CMOS-LTTL	2.5V	0.5V	2.0V	0.7V	2	Standard "B" Series Output Drive
LTTL-CMOS	1.1V	1.2V	3.5V	1.5V	See Remarks	3K Ω pull-up resistor. Fan-out determined by dynamic requirements
CMOS-LSTTL	2.5V	0.4V	2.0V	0.8V	1	Standard "B" Series Output Drive
LSTTL-CMOS	1.1V	1.1V	3.5V	1.5V	See Remarks	3K Ω pull-up resistor. Fan-out determined by dynamic requirements.
CMOS-HTL	5.0V	5.0V	8.5V	6.5V	1	
HTL-CMOS	2.5V	2.5V	11.0V	4.0V	> 50	Active pull-up HTL
	3.5V	3.5V			> 50	Passive pull-up HTL with 2K Ω to 5K Ω pull-up resistor.
CMOS-MOS	3.0V	4.0V	-3.0V	-9.0V	> 50	High threshold PMOS: $V_{SS}-V_{DD}=13V$
	2.5V	6.0V	2.5V	1.0V	> 50	Low threshold PMOS: $V_{SS}-V_{DD}=10V$
MOS-CMOS	3.9V	3.9V	-3.9V	-9.1V	> 50	High threshold PMOS: $V_{SS}-V_{DD}=13V$
	3.0V	3.0V	2.0V	-2.0V	> 50	Low threshold PMOS: $V_{SS}-V_{DD}=10V$
CMOS-ECL	0.225V	4.325V	-1.105	-1.475	2	V_{DD} =ground V_{SS} = -5.2V
ECL-CMOS	0.66V*	1.56V*	-1.56V	-3.64V	> 50	V_{DD} =ground V_{SS} = -5.2V

* typical with transistor driver

NOTES: 1. Interface Noise Margin

For "1" Column — difference between output high level of one device and input high level of next device.

For "0" Column — difference between output low level of one device and input low level of next device.

2. Interface Logic Level Worst-case threshold level going from one device to the input of another.

DYNAMIC CONSIDERATIONS

The operating speed of a CMOS logic system is dependent upon signal propagation delays, output transition times, and associated characteristics. These parameters vary as a function of output load capacitance (ac fanout), operating voltage, and device temperature.

All device data sheets give dynamic characteristics at $V_{DD} = 5, 10, \text{ and } 15 \text{ Vdc}$, 50pF load capacitance, and 25°C ambient temperature.

CAPACITIVE LOADING

The higher output impedance of CMOS devices, in comparison to TTL, make them more sensitive to capacitive loading (ac fan-out). A linear relationship exists between dynamic parameters and load capacitance, which is to be expected: loads are charged and discharged by the resistance of the driving transistor channel.

The buffered gate output structure pioneered by Solid State Scientific in 1970 provides significantly better performance than conventional CMOS gate structures. The single stage output makes delays and transition times independent of input pattern and less sensitive to capacitive loading. In addition, the extra gain stages provide significant pulse shaping of slow transition inputs — when input rise and fall times increase, the conventional gate exhibits an increase in output transition time, while the buffered gate transition times remain unchanged. This feature eliminates progressive deterioration of pulse characteristics in a system. These buffered outputs are designed for symmetric transition times, as opposed to the conventional types.

Special considerations must be given to output transition times and propagation delays when driving synchronous systems with edge triggered inputs. Consult the section on "Input Waveforms".

It should be noted that the extra gain stages in a buffered-output gate exhibit very sharp transfer characteristics. In certain applications, notably oscillators, multivibrators, or poor input transitions, this may result in ringing or even oscillation at the switching point. For this reason, Solid State Scientific manufactures several simple unbuffered inverters (SCL4007UB, SCL4069UB, SCL4449UB) and unbuffered 2-input gates (SCL4001UB, SCL4011UB). Since these types exhibit none of the features of buffered outputs, it is recommended that some pulse shaping be employed to permit use of the buffered structures wherever possible.

VOLTAGE EFFECTS

Increasing the supply voltage from 5Vdc to 10Vdc at least doubles the operating speed of CMOS devices. Increasing to 15V results in another increase, usually far less, at a substantial penalty in power dissipation. The increase in speed is a direct effect of the lower channel resistance; the increase in power dissipation is a symptom of higher charging currents to load capacitances.

Dynamic characteristics at voltages not given on device data sheets may be interpolated from specified data.

TEMPERATURE VARIATIONS

As the temperature of a CMOS device increases, carrier mobility decreases, resulting in an increase in channel impedance. Therefore, dynamic parameters change in proportion to the factor given previously: -0.3%/°C for operating frequency, +0.3%/°C for all other parameters. Consequently, this factor must be considered in designing a system which must operate at a given frequency over a wide temperature range.

THREE STATE LOGIC

Devices such as the SCL4016 and SCL4066 provide a means for constructing bus-oriented systems. Several devices in the SCL4000 Series employ variations in this structure to provide their own high-impedance output state. Leakage currents and capacitances are specified on individual data sheets, to allow the user to determine fan-out and system speed.

ANALOG SIGNAL SWITCHING

When using the analog switch device types, care must be taken to prevent the input signal from exceeding the supply voltage. Latch-up conditions may result if this precaution is not observed.

The ON-resistance characteristics of the switch are specified on the device data sheets. This enables the user to calculate power dissipation for high-current-drive requirements.

All CMOS switches are make-before-break. Therefore, in multiplexing applications, the low-impedance path between signal drivers which occurs during the overlap must be considered when generating control-input signals.

Further information is contained on individual data sheets.

HANDLING CMOS DEVICES

Care must be exercised in handling any CMOS device. Although all SSS CMOS devices have a built-in protective diode network which protects the device against damage due to static electric discharge, additional precautions should be followed to assure trouble-free performance after assembly. The following guidelines for handling CMOS devices are suggested:

A. GENERAL

- Use a conductive, grounded work surface.
- Keep operators at ground potential (use conductive wrist bands and a 1 megohm resistor to ground)
- Don't use nylon smocks.
- Repack devices in conductive or anti-static containers; keep devices at a common potential.
- Use conductive or anti-static envelopes for storing and shipping devices — never use untreated plastic.

B. CLEANING

- Use static neutralizing ion blower when manually cleaning with brushes.

Solid State Scientific CMOS integrated circuits are provided in chip form to permit customer design of special or hybrid circuits to suit individual needs. CMOS chips are electrically identical to (temperature range -55°C to $+125^{\circ}\text{C}$) and offer the features of their packaged counterparts. For maximum ratings, electrical characteristics, schematics, and features, see the individual data sheets in this catalog.

CHIP PREPARATION

- All chips have gold backs ($4500 \text{ \AA}$ Typ.) providing ohmic contact to substrate.
- All chips are glass passivated.
- Chip thickness is typically 15 mils, and cleavage angles are 57° .
- All chips are visually inspected to MIL-STD-883A, Mtd. 2010.2, Cond. B unless otherwise specified.
- All chips have been electrically tested for all static and functional parameters.
- Chip inspection and packaging is performed under laminar flow hoods in a temperature- and humidity-controlled dust-free atmosphere.

CHIP HANDLING

- Chips should be stored in a clean, dry atmosphere preferably below 40°C and 50% relative humidity.
- The user should exercise proper care when handling chips to prevent even the slightest mechanical damage to the chip.

- Ground all automatic equipment.
- Ground cleaning baskets.

C. ASSEMBLY

- Insert CMOS devices last to avoid overhandling.
- Use conductive handling trays.
- Use conductive material between edge connections.
- Ground all automatic insertion equipment.
- Ground solder machines and metallic parts of conveyor systems.
- Ground soldering irons.

D. TESTING

- Use grounded metallic fixtures where possible.
- Use static neutralizing ion air blower when using automatic handlers.
- Use conductive handling trays.
- Don't insert or remove boards with power turned ON.

CMOS CHIPS

- Individual handling should be done with nonmetallic vacuum pick-ups.
- Proper mounting and lead bonding techniques must be used to obtain optimum electrical, mechanical and thermal performance.
- The back surface of the chip is electrically connected to the P-channel substrates which should be the most positive potential (V_{DD}). Care must be taken to keep the active substrate isolated from ground or other circuit elements in the assembly. It is recommended that the $+V_{DD}$ pad on the front of the chip be wire bonded to the chip substrate mount for optimum performance.
- After mounting and bonding, necessary procedures must be followed to insure that the chips are not subjected to mechanical abuse or to moist or contaminated atmosphere which might permit electrical conductive paths across the relatively small insulating surfaces.
- Bonders, pick-up tools, table tops, sealing and die attach equipment, and other apparatus used in chip handling should be properly grounded.
- The operator should be properly grounded.
- Assemblies or sub-assemblies of chips should be transported and stored in conductive carriers.
- All external leads of assemblies should be shorted together.

sheets and catalogs, application notes, reliability documents, and other aids which acquaint the user with CMOS technology and the SCL4000 Series product line.

Currently available Application Notes from Solid State Scientific include the following:

- AN-101 Using Complementary MOS Circuits (W.F. Kalin)
- AN-102 CMOS Expandable Gates (W.F. Kalin)
- AN-104 Interfacing with CMOS (W.F. Kalin)
- AN-105 Improved CMOS Gate Design (G.D. Miller and J.B. Tomei)
- AN-107 A Simplified Approach to Testing CMOS Inverters and Gates (J. Gaskill)
- AN-108 Applications of CMOS Integrated Circuits in Communications Equipment (W.F. Kalin)
- AN-109 CMOS Wave Shaping and Level Detection (R.S. Schamis)
- AN-110 Designing with the SCM5533 CMOS Content Addressable Memory (B.H. Benjamin)
- AN-111 Using the SCL4528 Dual Monostable Multivibrator (V. Louison and B.H. Benjamin)

JEDEC STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES

MAY 1976

Formulated by
JEDEC Solid State Products Council

NOTE: Solid State Scientific has taken part in the activities of the JEDEC Committee since its inception, and fully supports the following specifications. All part types manufactured by Solid State Scientific and marked with the designation "B" meet or exceed the industry standard CMOS specifications described herein.

1. PURPOSE AND SCOPE

1.1 Purpose

To develop a standard of "B" Series CMOS Specifications to provide for uniformity, multiplicity of sources, elimination of confusion, and ease of device specification and system design by users.

1.2 Scope

This Standard covers standard specifications for description of "B" Series CMOS devices.

2. DEFINITIONS

2.1 "B" Series

"B" Series CMOS includes both buffered and unbuffered devices.

2.2 "Buffered"

A buffered output is one that has the characteristic that the output "on" impedance is independent of any and all valid input logic conditions, both preceding and present.

3. STANDARD SPECIFICATIONS

3.1 Listing of Standard Specifications. Table 1 lists the standard specifications for "B" Series CMOS devices.

3.2 Absolute Maximum Ratings. In the maximum ratings listed below voltages are referenced to V_{SS} .

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage	V_{DD}	-0.5 to + 18	Vdc
Input Voltage	V_{IN}	-0.5 to $V_{DD} + 0.5$	Vdc
DC Input Current (any one input)	I_{IN}	± 10	mAdc
Storage Temperature Range	T_S	-65 to + 150	°C

3.3 Recommended Operating Conditions. Recommended operating conditions are listed below.

RECOMMENDED OPERATING CONDITIONS

DC Supply Voltage	V_{DD}	+3 to + 15	Vdc
Operating Temperature Range	T_A		
Military-Range Devices		-55 to + 125	°C
Commercial-Range Devices		-40 to + 85	°C

3.4 Designation of "B" Series CMOS Devices

Those parts which have analog inputs and/or outputs shall be included in the "B" Series providing those parts' maximum ratings and logical input and output parameters conform to the "B" Series, such as (including, but not limited to):

4051B	4053B
4052B	4066B

Products that meet "B" Series specifications except that the logical outputs are not buffered and the V_{IL} and V_{IH} specifications are 20% and 80% of V_{DD} , respectively, shall be marked with the UB designation, such as (including, but not limited to):

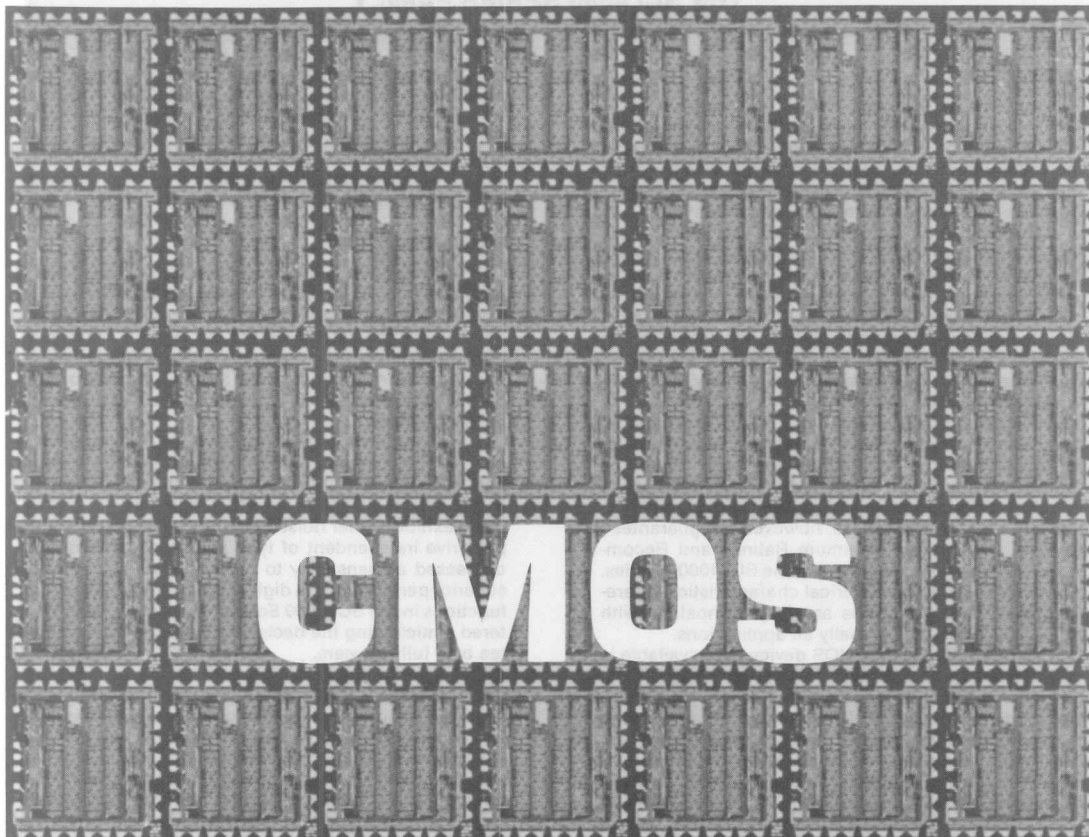
4000UB	4002UB	4011UB	4023UB	4041UB	4069UB
4001UB	4007UB	4012UB	4025UB	4049UB	

STATIC CHARACTERISTICS

PARAMETER			TEMP. RANGE	V _{DD} (Vdc)	CONDITIONS	LIMITS						UNITS	
						T _{LOW} *		+25°C			T _{HIGH} *		
						Min.	Max.	Min.	Typ.	Max.	Min.		Max.
I _{DD}	Quiescent Device Current	Mil	5	V _{IN} =V _{SS} or V _{DD}	—	0.25	—	—	0.25	—	7.5	μAdc	
			10		—	0.5	—	—	0.5	—	15		
			15		—	1.0	—	—	1.0	—	30		
		GATES	Comm	5	All valid input combinations	—	1.0	—	—	1.0	—	7.5	μAdc
				10		—	2.0	—	—	2.0	—	15	
				15		—	4.0	—	—	4.0	—	30	
	BUFFERS, FLIP-FLOPS	Mil	5	V _{IN} =V _{SS} or V _{DD}	—	1.0	—	—	1.0	—	30	μAdc	
			10		—	2.0	—	—	2.0	—	60		
			15		—	4.0	—	—	4.0	—	120		
		Comm	5	All valid input combinations	—	4.0	—	—	4.0	—	30	μAdc	
			10		—	8.0	—	—	8.0	—	60		
			15		—	16.0	—	—	16.0	—	120		
	MSI	Mil	5	V _{IN} =V _{SS} or V _{DD}	—	5	—	—	5	—	150	μAdc	
			10		—	10	—	—	10	—	300		
			15		—	20	—	—	20	—	600		
		Comm	5	All valid input combinations	—	20	—	—	20	—	150	μAdc	
			10		—	40	—	—	40	—	300		
			15		—	80	—	—	80	—	600		
V _{OL}	Low-Level Output Voltage	All	5	V _{IN} =V _{SS} or V _{DD} I _O ≤1μA	—	0.05	—	—	0.05	—	0.05	Vdc	
			10		—	0.05	—	—	0.05	—	0.05		
			15		—	0.05	—	—	0.05	—	0.05		
V _{OH}	High-Level Output Voltage	All	5	V _{IN} =V _{SS} or V _{DD} I _O ≤1μA	4.95	—	4.95	—	—	4.95	—	Vdc	
			10		9.95	—	9.95	—	—	9.95	—		
			15		14.95	—	14.95	—	—	14.95	—		
V _{IL}	Input Low Voltage	All	5	V _O = 0.5V or 4.5V 1.0V or 9.0V 1.5V or 13.5V I _O ≤1μA	—	1.5	—	—	1.5	—	1.5	Vdc	
			10		—	3.0	—	—	3.0	—	3.0		
			15		—	4.0	—	—	4.0	—	4.0		
V _{IH}	Input High Voltage	All	5	V _O = 0.5V or 4.5V 1.0V or 9.0V 1.5V or 13.5V I _O ≤1μA	3.5	—	3.5	—	—	3.5	—	Vdc	
			10		7.0	—	7.0	—	—	7.0	—		
			15		11.0	—	11.0	—	—	11.0	—		
I _{OL}	Output Low (Sink) Current	Mil	5	V _O =0.4V, V _{IN} =0 or 5V V _O =0.5V, V _{IN} =0 or 10V V _O =1.5V, V _{IN} =0 or 15V	0.64	—	0.51	—	—	0.36	—	mAdc	
			10		1.6	—	1.3	—	—	0.9	—		
			15		4.2	—	3.4	—	—	2.4	—		
		Comm	5	V _O =0.4V, V _{IN} =0 or 5V V _O =0.5V, V _{IN} =0 or 10V V _O =1.5V, V _{IN} =0 or 15V	0.52	—	0.44	—	—	0.36	—	mAdc	
			10		1.3	—	1.1	—	—	0.9	—		
			15		3.6	—	3.0	—	—	2.4	—		
I _{OH}	Output High (Source) Current	Mil	5	V _O =4.6V, V _{IN} =0 or 5V V _O =9.5V, V _{IN} =0 or 10V V _O =13.5V, V _{IN} =0 or 15V	-0.25	—	-0.2	—	—	-0.14	—	mAdc	
			10		-0.62	—	-0.5	—	—	-0.35	—		
			15		-1.8	—	-1.5	—	—	-1.1	—		
		Comm	5	V _O =4.6V, V _{IN} =0 or 5V V _O =9.5V, V _{IN} =0 or 10V V _O =13.5V, V _{IN} =0 or 15V	-0.2	—	-0.16	—	—	-0.12	—	mAdc	
			10		-0.5	—	-0.4	—	—	-0.3	—		
			15		-1.4	—	-1.2	—	—	-1.0	—		
I _{IN}	Input Current	Mil	15	V _{IN} =0 or 15V	—	±0.1	—	—	±0.1	—	±1.0	μAdc	
		Comm	15	V _{IN} =0 or 15V	—	±0.3	—	—	±0.3	—	±1.0	μAdc	
C _{IN}	Input Capacitance per Unit Load	All	—	Any Input	—	—	—	—	7.5	—	—	pF	

* T_{LOW} = -55°C for Military Temp. Range device, -40°C for Commercial Temp. Range device.

* T_{HIGH} = +125°C for Military Temp. Range device, +85°C for Commercial Temp. Range device.



THE SCL4000 SERIES FAMILY

THE SCL4000 SERIES FAMILY

INTRODUCTION

Solid State Scientific CMOS devices comprise a family of medium-speed integrated circuits with a superior combination of high noise immunity, wide operating voltage range, low power dissipation, and high fan-out. These characteristics greatly minimize power supply costs and simplify system design and layout.

The great majority of the devices in the SCL4000 Series exceed the JEDEC Standard Specifications for "B" Series CMOS Devices given in the previous section. For this reason, Solid State Scientific guarantees that all devices designated SCL4xxxB or SCL4xxxUB¹ will meet the electrical specifications given in the tables in this section. These standards are tighter than the JEDEC Specifications in several key areas, notably gate leakage currents (I_{DD}), output voltage (V_{OH} , V_{OL}) and, in several cases, output drive current (I_{OH} , I_{OL}). In addition, Solid State Scientific does not degrade any parameter for any commercial-temperature-range part type. The few device types which fail to meet the SCL4000B Series Family Specifications for any reason are designated by the suffix AB. These devices, however, are guaranteed to meet all Absolute Maximum Ratings and Recommended Operating Conditions of the SCL4000B Series, as well as most of the electrical characteristics. Therefore, these few part types are fully compatible with SCL4000B devices in virtually all applications.

All SCL4000 Series CMOS devices are available in military temperature range (-55°C to $+125^{\circ}\text{C}$) and commercial temperature range (-40°C to $+85^{\circ}\text{C}$) versions, and a variety of package configurations. Military temperature range devices are available in Frit-seal ceramic or Cerdip dual-in-line packages (C suffix — 14- and 16-lead types), welded-seal or side-brazed ceramic dual-in-line packages (D suffix — 14-, 16-, and 24-lead types), ceramic flat packs (F suffix — 14- and 16-lead types), and bare chip form (H suffix) for those users manufacturing hybrid microcircuits. Commercial tem-

perature range devices are available in the Epoxy B or plastic dual-in-line package (E suffix — 14-, 16- and 24-lead types). Since electrical parameters are never degraded for devices in this package, any mix of packages may be used in a system with confidence that they will be fully compatible throughout the entire range of valid operating conditions.

THE SCL4000B SERIES

Solid State Scientific anticipated the JEDEC Standard Specifications for "B" Series CMOS Devices by several years in several important areas. All part types have been consistently rated at 18 Vdc maximum operating voltage. This upgrading did not entail a process alteration; performance specifications for the higher voltages were simply added to the test programs for each device.

In addition, the decision of the JEDEC Committee to consider devices with buffered outputs as the standard part types in the "B" Series supports the position taken by Solid State Scientific in 1970. Since buffered-output gates exhibit higher noise immunity, standardized output drive independent of type and input pattern, and decreased ac sensitivity to output loading, they offer superior performance in digital logic applications. Gate functions in the SCL4000 Series have always been buffered, anticipating the decision of the JEDEC Committee by a full six years.

The following Family Specifications apply to all SCL4xxxB and SCL4xxxUB part types, unless otherwise specified on individual data sheets. Note that there are two distinct categories of output drive current (I_{OH} , I_{OL}) — standard and balanced. This second category applies to devices with equal source and sink current specifications at the conditions indicated. All SSI types (gates, flip-flops) and many MSI types fall into this category. Devices with balanced output drive current are plainly identified on individual data sheets.

¹As defined in JEDEC Standard Specification

SCL4000B SERIES FAMILY SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS¹

DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage	V_{IN}	-0.5 to $V_{DD} + 0.5$	Vdc
DC Input Current (any one input)	I_{IN}	± 10	mAdc
Power Dissipation	P_T	300	mW
Storage Temperature Range	T_S	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS¹

DC Supply Voltage	V_{DD}	3 to 15	Vdc
Operating Temperature Range	T_A		
Military Range Device (C,D,F packages, chips)		-55 to +125	°C
Commercial Range Device (E package)		-40 to +85	°C

¹Voltage referenced to V_{SS}

Parametric limits are guaranteed for $V_{DD} = 5, 10, \text{ and } 15 \text{ Vdc}$. Where low power is required, the lowest supply voltage, consistent with required speed, should be used. For larger noise immunity and higher speed, higher supply voltages should be specified. The lower limit of supply regulation is 3 Vdc or as determined by required system speed, noise immunity, or interface to other logic. The recommended upper limit is 15 Vdc or as determined by power dissipation restrictions or interface to other logic.

Unused inputs must be connected to V_{DD} , V_{SS} , or another input.

Care should be used in handling CMOS devices; static charges may damage the device.

ELECTRICAL SPECIFICATIONS

Parametric limits listed here are guaranteed for the entire SCL4000B Series Family unless otherwise specified on the individual data sheets.

STATIC CHARACTERISTICS ($V_{SS} = 0V$)

PARAMETER	V_{DD} (Vdc)	CONDITIONS	T_{LOW}^1		+25°C			T_{HIGH}^1		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT Gates	I_{DD}	$V_{IN} = V_{SS} \text{ or } V_{DD}$	—	0.05	—	0.0005	0.05	—	1.5	μAdc
			—	0.1	—	0.001	0.1	—	3.0	
			—	0.2	—	0.002	0.2	—	6.0	
Buffers, Flip-Flops		All valid input combinations	—	1.0	—	0.005	1.0	—	30	μAdc
			—	2.0	—	0.01	2.0	—	60	
			—	4.0	—	0.02	4.0	—	120	
MSI			—	5	—	0.05	5	—	150	μAdc
			—	10	—	0.1	10	—	300	
			—	20	—	0.2	20	—	600	
HIGH-LEVEL OUTPUT VOLTAGE	V_{OH}	$V_{IN} = V_{SS} \text{ or } V_{DD}$ $ I_O \leq 1\mu\text{A}$	4.99	—	4.99	5	—	4.95	—	Vdc
			9.99	—	9.99	10	—	9.95	—	
			14.99	—	14.99	15	—	14.95	—	
LOW-LEVEL OUTPUT VOLTAGE	V_{OL}	$V_{IN} = V_{SS} \text{ or } V_{DD}$ $ I_O \leq 1\mu\text{A}$	—	0.01	—	0	0.01	—	0.05	Vdc
			—	0.01	—	0	0.01	—	0.05	
			—	0.01	—	0	0.01	—	0.05	
MINIMUM INPUT HIGH VOLTAGE	V_{IH}	$V_O = 0.5V \text{ or } 4.5V$ $V_O = 1.0V \text{ or } 9.0V$ $V_O = 1.5V \text{ or } 13.5V$ $ I_O \leq 1\mu\text{A}$	—	3.5	—	2.75	3.5	—	3.5	Vdc
			—	7.0	—	5.5	7.0	—	7.0	
			—	11.0	—	8.25	11.0	—	11.0	

¹ T_{LOW} = -55°C for C, D, F, and H devices (Military Temperature Range)

= -40°C for E device (Commercial Temperature Range)

T_{HIGH} = +125°C for C, D, F, and H devices (Military Temperature Range)

= +85°C for E device (Commercial Temperature Range)

STATIC CHARACTERISTICS ($V_{SS} = 0V$) Continued

PARAMETER	V_{DD} (Vdc)	CONDITIONS	T_{LOW}^1		+25°C			T_{HIGH}^1		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
MAXIMUM INPUT LOW VOLTAGE	V_{IL}	5 $V_O=0.5V$ or $4.5V$	1.5	—	1.5	2.25	—	1.5	—	Vdc
		10 $V_O=1.0V$ or $9.0V$	3.0	—	3.0	4.5	—	3.0	—	
		15 $V_O=1.5V$ or $13.5V$	4.0	—	4.0	6.75	—	4.0	—	
		$ I_O \leq 1\mu A$								
OUTPUT HIGH (SOURCE) CURRENT Standard: C, D, F, H device	I_{OH}	5 $V_{OH}=4.6V$	-0.25	—	-0.2	-0.5	—	-0.14	—	mAdc
		10 $V_{OH}=9.5V$	-0.62	—	-0.5	-1.3	—	-0.35	—	
		15 $V_{OH}=13.5V$	-1.9	—	-1.5	-5.0	—	-1.1	—	
		$V_{IN}=V_{SS}$ or V_{DD}								
		5 $V_{OH}=4.6V$	-0.24	—	-0.2	-0.5	—	-0.16	—	mAdc
		10 $V_{OH}=9.5V$	-0.6	—	-0.5	-1.3	—	-0.4	—	
		15 $V_{OH}=13.5V$	-1.8	—	-1.5	-5.0	—	-1.2	—	
		$V_{IN}=V_{SS}$ or V_{DD}								
		5 $V_{OH}=4.6V$	-0.64	—	-0.51	-1.25	—	-0.36	—	mAdc
		10 $V_{OH}=9.5V$	-1.6	—	-1.3	-3.25	—	-0.9	—	
		15 $V_{OH}=13.5V$	-4.2	—	-3.4	-10	—	-2.4	—	
		$V_{IN}=V_{SS}$ or V_{DD}								
		5 $V_{OH}=4.6V$	-0.61	—	-0.51	-1.25	—	-0.41	—	mAdc
		10 $V_{OH}=9.5V$	-1.5	—	-1.3	-3.25	—	-1.1	—	
		15 $V_{OH}=13.5V$	-4.0	—	-3.4	-10	—	-2.8	—	
		$V_{IN}=V_{SS}$ or V_{DD}								
OUTPUT LOW (SINK) CURRENT Standard: C, D, F, H device	I_{OL}	5 $V_{OL}=0.4V$	0.64	—	0.51	0.78	—	0.36	—	mAdc
		10 $V_{OL}=0.5V$	1.6	—	1.3	2.0	—	0.9	—	
		15 $V_{OL}=1.5V$	4.2	—	3.4	7.8	—	2.4	—	
		$V_{IN}=V_{SS}$ or V_{DD}								
		5 $V_{OL}=0.4V$	0.61	—	0.51	0.78	—	0.41	—	mAdc
		10 $V_{OL}=0.5V$	1.5	—	1.3	2.0	—	1.1	—	
		15 $V_{OL}=1.5V$	4.0	—	3.4	7.8	—	2.8	—	
		$V_{IN}=V_{SS}$ or V_{DD}								
		5 $V_{OL}=0.4V$	0.64	—	0.51	1.25	—	0.36	—	mAdc
		10 $V_{OL}=0.5V$	1.6	—	1.3	3.25	—	0.9	—	
		15 $V_{OL}=1.5V$	4.2	—	3.4	10	—	2.4	—	
		$V_{IN}=V_{SS}$ or V_{DD}								
		5 $V_{OL}=0.4V$	0.61	—	0.51	1.25	—	0.41	—	mAdc
		10 $V_{OL}=0.5V$	1.5	—	1.3	3.25	—	1.1	—	
		15 $V_{OL}=1.5V$	4.0	—	3.4	10	—	2.8	—	
		$V_{IN}=V_{SS}$ or V_{DD}								
INPUT CURRENT	I_{IN}	15 $V_{IN}=0$ or $15V$	—	± 0.1	—	$\pm 10^{-5}$	± 0.1	—	± 1.0	μAdc

¹ T_{LOW} = -55°C for C, D, F, and H devices (Military Temperature Range)

= -40°C for E device (Commercial Temperature Range)

T_{HIGH} = +125°C for C, D, F, and H devices (Military Temperature Range)

= +85°C for E device (Commercial Temperature Range)

DYNAMIC CHARACTERISTICS ($T_A = 25^\circ C$)

PARAMETER	V_{DD} (Vdc)	Min.	Typ.	Max.	Units
INPUT CAPACITANCE	C_{IN}	—	5	7.5	pF

Part types designated "UB" meet the above parametric specifications with the following exception, unless otherwise specified on the individual data sheets.

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ¹		+25°C			T _{HIGH} ¹		Unit
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
MINIMUM INPUT HIGH VOLTAGE	V _{IH}	5 V _O =0.5V or 4.5V	—	4.0	—	2.75	4.0	—	4.0	Vdc
		10 V _O =1.0V or 9.0V	—	8.0	—	5.5	8.0	—	8.0	
		15 V _O =1.5V or 13.5V I _O ≤ 1μA	—	12.0	—	8.25	12.0	—	12.0	
MAXIMUM INPUT LOW VOLTAGE	V _{IL}	5 V _O =0.5V or 4.5V	1.0	—	1.0	2.25	—	1.0	—	Vdc
		10 V _O =1.0V or 9.0V	2.0	—	2.0	4.5	—	2.0	—	
		15 V _O =1.5V or 13.5V I _O ≤ 1μA	3.0	—	3.0	6.75	—	3.0	—	

¹ T_{LOW} = -55°C for C, D, F, and H devices (Military Temperature Range)

= -40°C for E device (Commercial Temperature Range)

T_{HIGH} = +125°C for C, D, F, and H devices (Military Temperature Range)

= +85°C for E device (Commercial Temperature Range)

The user should consult the section of this book entitled "CMOS Design Considerations" in conjunction with the Family Specifications given here to assure proper system performance.

¹As defined in JEDEC Standard Specification

PARAMETER DEFINITIONS AND WAVEFORMS

DEFINITIONS

The following information provides detailed explanations of the electrical parameters specified on SCL4000 Series data sheets. These parameters are categorized into Absolute Maximum Ratings, Recommended Operating Conditions, Static Electrical Characteristics, and Dynamic Electrical Characteristics. Virtually all devices in the SCL4000 Series are fully described by a combination of the parameters identified in this section; in a few special cases, however, parameters unique to a device are defined on the individual data sheet.

While all parameters exhibit a statistical distribution about a mean value, only the mean value and one worst-case limit — either the minimum or the maximum value — appears on the data sheet. Following the EIA standard guidelines, the minimum limit value is always less than the mean or typical value, and the maximum

limit value is always greater than the typical value. Several parameters, therefore, require the prefix "minimum" or "maximum" in order to maintain the proper convention on the data sheet. These prefixes should not be confused with the minimum and maximum designations applied to limit values. Thus, "maximum clock frequency" has minimum limit values specified, while "minimum clock pulse width" has maximum limit values specified.

Each parameter is measured under a specified set of conditions: supply voltage, input voltages and currents, output voltages and currents, input signal switching characteristics, etc. To assist the designer in constructing his system, any given parameter is measured under the same test conditions for all devices in the SCL4000 Series, whether they fall into the B, UB, or AB designation.

ABSOLUTE MAXIMUM RATINGS

These ratings are absolute limits within which safe operation occurs. The presence of conditions outside these limits may cause severe device degradation, and possibly catastrophic failure. These ratings apply across the entire temperature range.

DC Supply Voltage Range

To prevent forward biasing and possibly damaging the structural and protective diode junctions present in CMOS construction, V_{DD} must never be more than 0.5Vdc negative with respect to V_{SS} .

The maximum limit of 18Vdc prevents primary breakdown of any internal device junction.

Input Voltage Range

The voltage at any device input must not exceed either the V_{SS} or V_{DD} supply voltages by more than 0.5Vdc. Unrestricted operation outside this range may damage the input protection diodes, or cause internal latch-up.

RECOMMENDED OPERATING CONDITIONS

These conditions specify ranges within which reliable operations may be maintained. Systems utilizing CMOS should be designed to operate within these ranges.

DC Supply Voltage Range

The lower limit of 3Vdc is based upon transistor threshold levels. The recommended maximum limit of 15V is substantially below the primary breakdown limit for the devices to allow for limited power-supply transient and regulation limits.

STATIC ELECTRICAL CHARACTERISTICS

These parameters apply to devices in the steady-state condition. They are specified at the low temperature limits (-55°C or -40°C), $+25^{\circ}\text{C}$, and the high temperature limits ($+125^{\circ}\text{C}$ or $+85^{\circ}\text{C}$), with typical values given at $+25^{\circ}\text{C}$.

Quiescent Device Current (I_{DD})

Quiescent current is defined as the current flowing

DC Input Current

To prevent excessive dissipation in the junctions of the protection diodes, input current must be limited to less than 10mAdc.

Maximum Package Power Dissipation

This requirement prevents excessive junction or package temperatures from developing. The maximum rating of 300mW includes both quiescent (dc) and dynamic (ac) dissipation, and should be calculated from the discussion of Power Dissipation in the section entitled "Design Considerations."

Storage Temperature Range

The temperature range within which devices may be stored without electrical connection is -65°C to $+150^{\circ}\text{C}$. Device reliability may be degraded when stored outside this range.

Operating Temperature Range

The maximum ambient temperature range within which the device may be reliably operated is -55°C to $+125^{\circ}\text{C}$ (the standard military temperature range) for the C, D, and F packages, and -40°C to $+85^{\circ}\text{C}$ (an extended commercial range) for the E package. Chips (H suffix) may be operated over the full military temperature range, -55°C to $+125^{\circ}\text{C}$.

into the V_{DD} terminal of the device with no load on the outputs. This current is measured under all valid input combinations (inputs tied in all valid combinations to V_{SS} or V_{DD}). The maximum limit reflects domination by surface leakage effects. Most devices exhibiting typical leakage currents are dominated by junction leakage which doubles with every 11°C increase in temperature.

These values have been standardized into three

categories: gates, buffers and flip-flops, and MSI devices. Solid State Scientific does not degrade this parameter for commercial temperature range devices (E package).

Output Voltage (V_{OH} , V_{OL})

V_{OH} is defined as the high-level output voltage under no-load conditions ($|I_O| < 1\mu A$), with inputs tied to V_{SS} or V_{DD} . Similarly, V_{OL} is the low-level output voltage measured under the same conditions. Both parameters are guaranteed to be no more than 0.01Vdc from the supply voltage at low temperature and +25°C, and no more than 0.05Vdc from the supply voltage at high temperature.

Input Voltage (V_{IH} , V_{IL})

V_{IH} and V_{IL} are defined as the minimum input high voltage and the maximum input low voltage, respectively, which produce no more than a 10% V_{DD} change in output voltage under no-load conditions ($|I_O| < 1\mu A$). This parameter differentiates device designations "B" and "UB".

In general, "B" devices have greater noise immunity, i.e., lower V_{IH} and higher V_{IL} , than "UB" devices because output buffering more effectively isolates outputs from input voltage variations.

Output Drive Currents (I_{OH} , I_{OL})

Output drive current is the source current (I_{OH}) with the output high, or the sink current (I_{OL}) with the output low, that flows out of or into the device from a load of specific voltage. Polarity is defined as positive when flowing into the output. Inputs are tied directly to V_{SS} or V_{DD} ; output voltages are specified at equal voltage drops for both parameters at given supply voltage.

At $V_{DD} = 5Vdc$, I_{OH} and I_{OL} are specified at $V_{OH} = 4.6Vdc$ and $V_{OL} = 0.4Vdc$, respectively. Logic outputs of "B" and "UB" devices are capable of driving one low-power TTL load across temperature. Although the source current (I_{OH}) specification for these devices is lower than the sink current (I_{OL}) specification (I_{IL} (TTL) $>> I_{IH}$), many devices in the SCL 4000 Series Family are designed for balanced drives at these output voltages.

DYNAMIC ELECTRICAL CHARACTERISTICS

Switching characteristics are specified at a total output load capacitance per output $C_L = 50pF$, ambient temperature $T_A = 25^\circ C$, and input rise and fall times t_r , $t_f = 20nS$ (except for maximum input rise and fall time specifications). Typical temperature coefficient for dynamic characteristics is $|0.3\%/^\circ C|$ (negative for maximum clock frequency (f_{CL}) and positive for other parameters). Solid State Scientific does not degrade dynamic parameters for commercial temperature range devices (E package).

Propagation Delay Time (t_{PLH} , t_{PHL})

These parameters are specified on all data sheets. For non-synchronous circuits and inputs, the delay time is measured from the 50% point of the input signal edge to the 50% point of the resulting output signal edge. For synchronous inputs (having a clock signal), the delay time is measured from the 50% of the clock signal edge associated with the input level to the 50% point of the resulting output signal edge. The designation "LH" refers to the low-to-high output transition; "HL" refers to the high-to-low output transition. Propagation delays increase linearly with load capacitance.

All gates and flip-flops, and a number of MSI parts, fall into this category; this is noted on the individual data sheets.

At $V_{DD} = 10Vdc$, an output voltage drop of 0.5Vdc from either supply is used as the standard condition for specifying I_{OH} and I_{OL} .

At $V_{DD} = 15Vdc$, 1.5Vdc is used as the standard output voltage drop. Current values are designed to drive two standard HTL loads over temperature.

The limits at the temperature extremes reflect the $0.3\%/^\circ C$ current decrease with increasing temperature at $25^\circ C$ characteristic of CMOS. Most device data sheets supply transistor characteristic curves for determination of output drive current under other operating conditions.

Solid State Scientific does not degrade these parameters for commercial temperature range devices (E package).

3-State Output Leakage Current (I_{ZL})

Leakage current at the output terminal of a 3-state device when disabled (high-impedance state) is measured under the two worst-case conditions: V_{DD} is applied at the output along with input combinations which would normally force the output low; V_{SS} is applied at the output along with input combinations which would normally force the output high.

Solid State Scientific does not degrade this parameter for commercial temperature range devices (E package).

Input Current

Input current is defined as the current that flows into or out of an input terminal when V_{SS} or V_{DD} is applied to that terminal. Input current consists of junction leakages in the diode protection circuit, and is typically $\pm 10pAdc$. Worst-case input current is specified at $V_{DD} = 15Vdc$ across temperature, with a maximum of $\pm 1.0uAdc$ at $+125^\circ C$ ($+85^\circ C$ for commercial temperature range devices).

Solid State Scientific does not degrade this parameter for commercial temperature range devices.

3-State Propagation Delay (t_{PHZ} , t_{PLZ} , t_{PZH} , t_{PZL})

The t_{PHZ} (high-level to 3-state) and t_{PLZ} (low-level to 3-state) propagation delays are measured from the 50% point of the disable input leading edge to the 90% point of the output signal falling edge (t_{PHZ}) or to the 10% point of the output signal rising edge (t_{PLZ}). The t_{PZH} (3-state to high-level) and t_{PZL} (3-state to low-level) propagation delays are measured from the 50% point of the disable input trailing edge to the 10% point of the output signal rising edge (t_{PZH}) or to the 90% point of the output signal falling edge (t_{PZL}). In addition to the 50pF load capacitance, a 1K Ω load resistor is tied to V_{SS} (t_{PHZ} and t_{PZH}) or V_{DD} (t_{PLZ} and t_{PZL}).

Output Transition Time (t_{TLH} , t_{THL})

These parameters refer to the rise (t_{TLH}) and fall (t_{THL}) times at device outputs. They are measured from the 10% to the 90% points of the output waveform. Both parameters are functions of output transistor sizes, and fall into standard categories in the same way as output drive current. Output transition times vary linearly with load capacitance C_L .

Minimum (Clock) Pulse Width (PW)

Minimum pulse width refers to that portion of the input signal between the active (leading) edge and the opposite (trailing) edge. It is defined as the interval between the 50% points of each edge. When applied to clock signals, this parameter also refers to the remaining portion of the signal, i.e., 50% duty cycle.

Maximum Clock Frequency (f_{CL})

The maximum clock frequency is the rate at which information can transfer through a synchronous circuit without developing system problems due to excessive propagation delays across internal stages.

Maximum Clock Rise and Fall Times (t_{rCL} , t_{fCL})

These limits refer to the maximum allowable input transition times which prevent interactions between internal stages from interfering with proper clocking. These parameters are measured from the 10% point to the 90% point of the input signal, and usually decrease with increasing operating voltage.

When synchronous stages are cascaded, however, maximum rise and fall times of the clock input should be equal to or less than the transition times of data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitive load. This prevents improper operation resulting from logic state interaction between adjoining stages.

Minimum Setup Time (t_{setup})

Setup time refers to the minimum interval between the data or control input signal and the clock or strobe signal which guarantees proper entry of that information into the device. It is measured between the 50% points of the two appropriate edges.

Minimum Hold Time (t_{hold})

Hold time refers to the interval after the clock or strobe edge during which data or control information must remain valid. It is measured between the 50% points of the two appropriate edges.

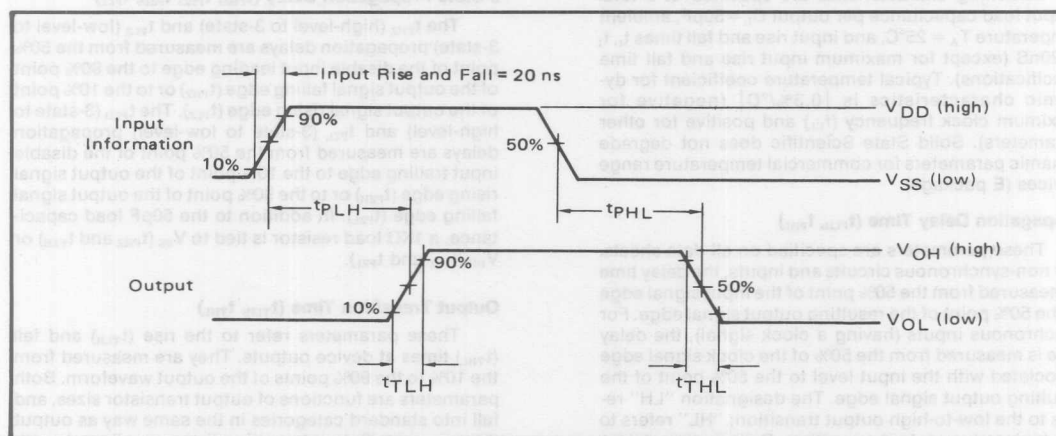
Removal Time (t_{rem})

Removal time is defined as the interval after removing an asynchronous control input during which a clock or strobe signal edge may not be recognized. This parameter is similar to minimum setup time, and is measured from the 50% point of the control input trailing edge to the 50% point of the clock or strobe signal leading edge.

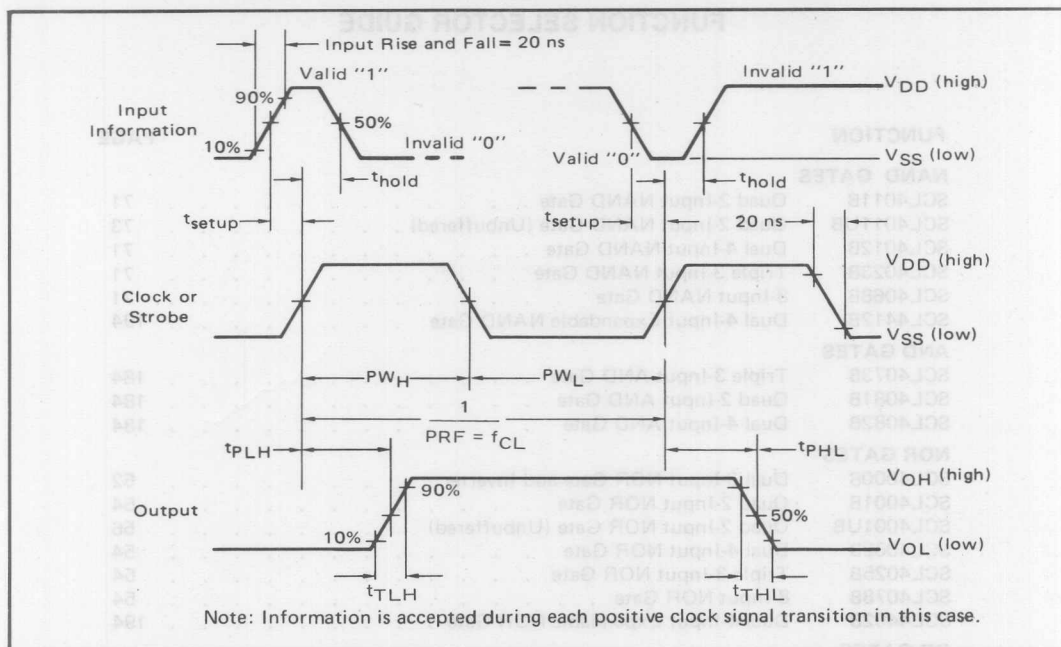
Input Capacitance (C_{IN})

The input capacitance is defined as the ac capacitance under zero bias conditions as applied to any input. This capacitance is typically 5pF for most devices; it is somewhat higher for inputs to high-current buffers.

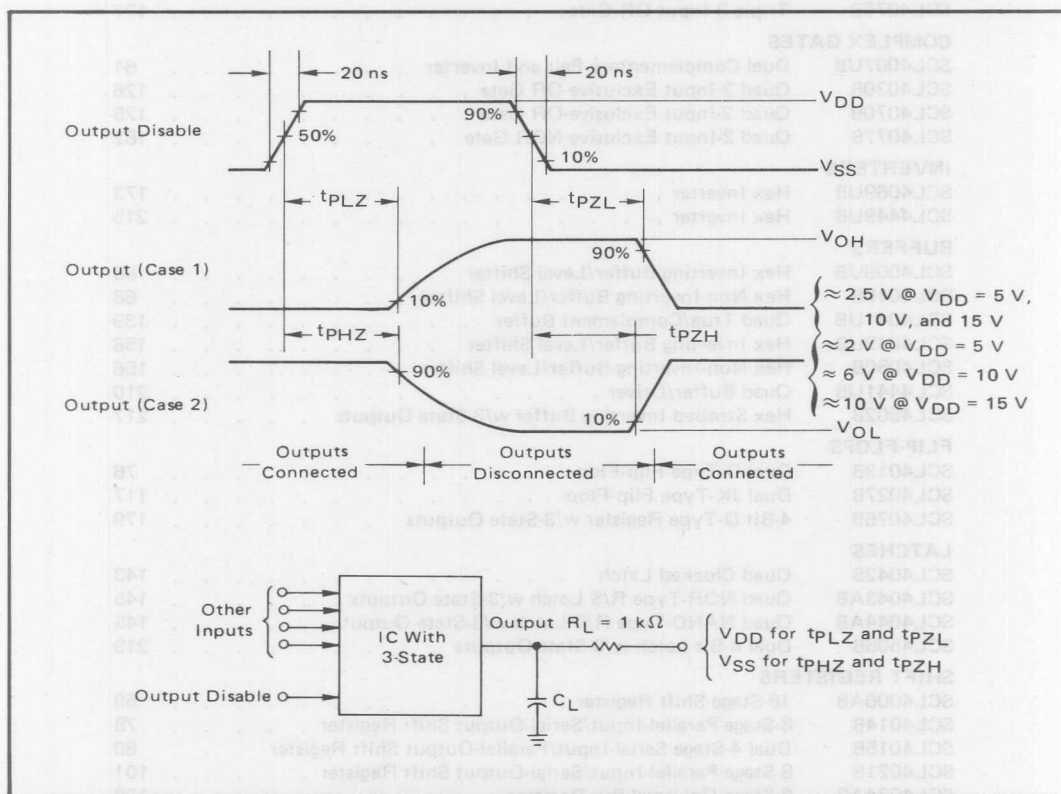
DYNAMIC ELECTRICAL CHARACTERISTICS



Non-Synchronous Circuit Waveshapes and Timing Parameters



Synchronous Circuit Waveshapes and Timing Parameters



Three-State Propagation Delay Waveshape and Test Circuit

FUNCTION SELECTOR GUIDE

FUNCTION	PAGE
NAND GATES	
SCL4011B Quad 2-Input NAND Gate	71
SCL4011UB Quad 2-Input NAND Gate (Unbuffered)	73
SCL4012B Dual 4-Input NAND Gate	71
SCL4023B Triple 3-Input NAND Gate	71
SCL4068B 8-Input NAND Gate	71
SCL4412B Dual 4-Input Expandable NAND Gate	194
AND GATES	
SCL4073B Triple 3-Input AND Gate	184
SCL4081B Quad 2-Input AND Gate	184
SCL4082B Dual 4-Input AND Gate	184
NOR GATES	
SCL4000B Dual 3-Input NOR Gate and Inverter	52
SCL4001B Quad 2-Input NOR Gate	54
SCL4001UB Quad 2-Input NOR Gate (Unbuffered)	56
SCL4002B Dual 4-Input NOR Gate	54
SCL4025B Triple 3-Input NOR Gate	54
SCL4078B 8-Input NOR Gate	54
SCL4402B Dual 4-Input Expandable NOR Gate	194
OR GATES	
SCL4071B Quad 2-Input OR Gate	177
SCL4072B Dual 4-Input OR Gate	177
SCL4075B Triple 3-Input OR Gate	177
COMPLEX GATES	
SCL4007UB Dual Complementary Pair and Inverter	61
SCL4030B Quad 2-Input Exclusive-OR Gate	126
SCL4070B Quad 2-Input Exclusive-OR Gate	175
SCL4077B Quad 2-Input Exclusive-NOR Gate	182
INVERTERS	
SCL4069UB Hex Inverter	173
SCL4449UB Hex Inverter	215
BUFFERS	
SCL4009UB Hex Inverting Buffer/Level Shifter	68
SCL4010B Hex Non-Inverting Buffer/Level Shifter	68
SCL4041UB Quad True/Complement Buffer	139
SCL4049UB Hex Inverting Buffer/Level Shifter	156
SCL4050B Hex Non-Inverting Buffer/Level Shifter	156
SCL4441UB Quad Buffer/Driver	210
SCL4502B Hex Strobed Inverting Buffer w/3-State Outputs	217
FLIP-FLOPS	
SCL4013B Dual D-Type Flip-Flop	76
SCL4027B Dual JK-Type Flip-Flop	117
SCL4076B 4-Bit D-Type Register w/3-State Outputs	179
LATCHES	
SCL4042B Quad Clocked Latch	143
SCL4043AB Quad NOR-Type R/S Latch w/3-State Outputs	145
SCL4044AB Quad NAND-Type R/S Latch w/3-State Outputs	145
SCL4508B Dual 4-Bit Latch w/3-State Outputs	219
SHIFT REGISTERS	
SCL4006AB 18-Stage Shift Register	59
SCL4014B 8-Stage Parallel-Input/Serial-Output Shift Register	78
SCL4015B Dual 4-Stage Serial-Input/Parallel-Output Shift Register	80
SCL4021B 8-Stage Parallel-Input/Serial-Output Shift Register	101
SCL4034AB 8-Stage Universal Bus Register	128
SCL4035B 4-Stage Parallel-Input/Parallel-Output Shift Register	133

FUNCTION SELECTOR GUIDE (Continued)

FUNCTION	PAGE
COUNTERS	
SCL4017AB	Decade Counter w/10 Decoded Outputs 88
SCL4018B	Presetable Divide-by-N Counter 93
SCL4020AB	14-Stage Binary Counter 98
SCL4022AB	Binary Counter w/8 Decoded Outputs 104
SCL4024B	7-Stage Binary Counter 109
SCL4029B	Presetable Up/Down Binary/Decade Counter 122
SCL4040AB	12-Stage Binary Counter 136
SCL4060AB	14-Stage Binary Counter and Oscillator 164
SCL4160B	BCD Decade Counter w/Asynchronous Clear 189
SCL4161B	4-Stage Binary Counter w/Asynchronous Clear 189
SCL4162B	BCD Decade Counter w/Synchronous Clear 189
SCL4163B	4-Stage Binary Counter w/Synchronous Clear 189
SCL4404B	8-Stage Binary Counter 196
SCL4510B	BCD Decade Programmable Up/Down Counter 222
SCL4516B	4-Stage Binary Programmable Up/Down Counter 236
SCL4518B	Dual BCD Decade Up Counter 240
SCL4520B	Dual 4-Stage Binary Up Counter 240
SCL4522B	BCD Decade Programmable Down Counter 243
SCL4526B	4-Stage Binary Programmable Down Counter 243
DECODERS	
SCL4026AB	Decade Counter w/7-Segment Outputs 112
SCL4028B	BCD-to-Decimal Decoder 119
SCL4033AB	Decade Counter w/7-Segment Outputs 112
SCL4426AB	Decade Counter w/7-Segment Driver Outputs 202
SCL4428B	Binary-to-Octal Decoder 207
SCL4433AB	Decade Counter w/7-Segment Driver Outputs 202
SCL4511B	BCD-to-7 Segment Latch/Decoder/Driver 226
SCL4514B	4-to-16 Line Decoder with Latch (Active High Outputs) 233
SCL4515B	4-to-16 Line Decoder with Latch (Active Low Outputs) 233
SCL4543B	BCD-to-7 Segment Latch/Decoder/Driver 257
SCL4555B	Dual 2-to-4 Line Decoder (Active High Outputs) 260
SCL4556B	Dual 2-to-4 Line Decoder (Active Low Outputs) 260
DIGITAL MULTIPLEXERS	
SCL4019B	Quad AND-OR Select Gate 96
SCL4512B	8-Channel Data Selector 229
ANALOG SWITCHES/MULTIPLEXERS/DEMULTIPLEXERS	
SCL4016AB	Quad Analog Switch 82
SCL4051B	8-Channel Analog Multiplexer/Demultiplexer 159
SCL4052B	Differential 4-Channel Analog Multiplexer/Demultiplexer 159
SCL4053B	Triple 2-Channel Analog Multiplexer/Demultiplexer 159
SCL4066B	Quad Analog Switch 168
SCL4416AB	Quad Analog Switch 198
ARITHMETIC OPERATORS	
SCL4008B	Four-Bit Full Adder 64
SCL4531B	12-Bit Parity Tree 255
SCL4581B	4-Bit Arithmetic Logic Unit 263
SCL4582B	Look-Ahead Carry Block 267
SCL4585B	4-Bit Magnitude Comparator 269
FREQUENCY DIVIDERS/RATE MULTIPLIERS	
SCL4445B	21-Stage Frequency Divider and Oscillator 212
SCL4527B	BCD Rate Multiplier 247
MULTIVIBRATORS/PHASE-LOCKED LOOPS	
SCL4046B	Phase-Locked Loop 148
SCL4446B	Phase-Locked Loop 148
SCL4528B	Dual Monostable Multivibrator 251
SCHMITT TRIGGERS	
SCL4093B	Quad 2-Input NAND Schmitt Trigger 186

INDEX TO PRODUCT DATA SHEETS

To simplify data reference, data sheets are arranged as nearly as possible in numerical sequence of device type numbers. Because some data sheets include more than one part type, however, some types may be out of sequence.

NUMERICAL DEVICE INDEX

DEVICE		PAGE
SCL4000B	Dual 3-Input NOR Gate and Inverter	52
SCL4001B	Quad 2-Input NOR Gate	54
SCL4001UB	Quad 2-Input NOR Gate (Unbuffered)	56
SCL4002B	Dual 4-Input NOR Gate	54
SCL4006AB	18-Stage Shift Register	59
SCL4007UB	Dual Complementary Pair and Inverter	61
SCL4008B	Four-Bit Full Adder	64
SCL4009UB	Hex Inverting Buffer/Level Shifter	68
SCL4010B	Hex Non-Inverting Buffer/Level Shifter	68
SCL4011B	Quad 2-Input NAND Gate	71
SCL4011UB	Quad 2-Input NAND Gate (Unbuffered)	73
SCL4012B	Dual 4-Input NAND Gate	71
SCL4013B	Dual D-Type Flip-Flop	76
SCL4014B	8-Stage Parallel-Input/Serial-Output Shift Register	78
SCL4015B	Dual 4-Stage Serial-Input/Parallel-Output Shift Register	80
SCL4016AB	Quad Analog Switch	82
SCL4017AB	Decade Counter w/10 Decoded Outputs	88
SCL4018B	Presettable Divide-by-N Counter	93
SCL4019B	Quad AND-OR Select Gate	96
SCL4020AB	14-Stage Binary Counter	98
SCL4021B	8-Stage Parallel-Input/Serial-Output Shift Register	101
SCL4022AB	Binary Counter w/8 Decoded Outputs	104
SCL4023B	Triple 3-Input NAND Gate	71
SCL4024B	7-Stage Binary Counter	109
SCL4025B	Triple 3-Input NOR Gate	54
SCL4026AB	Decade Counter w/7-Segment Outputs	112
SCL4027B	Dual JK-Type Flip-Flop	117
SCL4028B	BCD-to-Decimal Decoder	119
SCL4029B	Presettable Up/Down Binary/Decade Counter	122
SCL4030B	Quad 2-Input Exclusive-OR Gate	126
SCL4033AB	Decade Counter w/7-Segment Outputs	112
SCL4034AB	8-Stage Universal Bus Register	128
SCL4035B	4-Stage Parallel-Input/Parallel-Output Shift Register	133
SCL4040AB	12-Stage Binary Counter	136
SCL4041UB	Quad True/Complement Buffer	139
SCL4042B	Quad Clocked Latch	143
SCL4043AB	Quad NOR-Type R/S Latch w/3-State Outputs	145
SCL4044AB	Quad NAND-Type R/S Latch w/3-State Outputs	145
SCL4046B	Phase-Locked Loop	148
SCL4049UB	Hex Inverting Buffer/Level Shifter	156
SCL4050B	Hex Non-Inverting Buffer/Level Shifter	156
SCL4051B	8-Channel Analog Multiplexer/Demultiplexer	159
SCL4052B	Differential 4-Channel Analog Multiplexer/Demultiplexer	159
SCL4053B	Triple 2-Channel Analog Multiplexer/Demultiplexer	159
SCL4060AB	14-Stage Binary Counter and Oscillator	164
SCL4066B	Quad Analog Switch	168
SCL4068B	8-Input NAND Gate	71
SCL4069UB	Hex Inverter	173
SCL4070B	Quad 2-Input Exclusive-OR Gate	175
SCL4071B	Quad 2-Input OR Gate	177

NUMERICAL DEVICE INDEX (Continued)

DEVICE		PAGE
SCL4072B	Dual 4-Input OR Gate	177
SCL4073B	Triple 3-Input AND Gate	184
SCL4075B	Triple 3-Input OR Gate	177
SCL4076B	4-Bit D-Type Register w/3-State Outputs	179
SCL4077B	Quad 2-Input Exclusive-NOR Gate	182
SCL4078B	8-Input NOR Gate	54
SCL4081B	Quad 2-Input AND Gate	184
SCL4082B	Dual 4-Input AND Gate	184
SCL4093B	Quad 2-Input NAND Schmitt Trigger	186
SCL4160B	BCD Decade Counter w/Asynchronous Clear	189
SCL4161B	4-Stage Binary Counter w/Asynchronous Clear	189
SCL4162B	BCD Decade Counter w/Synchronous Clear	189
SCL4163B	4-Stage Binary Counter w/Synchronous Clear	189
SCL4402B	Dual 4-Input Expandable NOR Gate	194
SCL4404B	8-Stage Binary Counter	196
SCL4412B	Dual 4-Input Expandable NAND Gate	194
SCL4416AB	Quad Analog Switch	198
SCL4426AB	Decade Counter w/7-Segment Driver Outputs	202
SCL4428B	Binary-to-Octal Decoder	207
SCL4433AB	Decade Counter w/7-Segment Driver Outputs	202
SCL4441UB	Quad Buffer/Driver	210
SCL4445B	21-Stage Frequency Divider and Oscillator	212
SCL4446B	Phase-Locked Loop	148
SCL4449UB	Hex Inverter	215
SCL4502B	Hex Strobed Inverting Buffer w/3-State Outputs	217
SCL4508B	Dual 4-Bit Latch w/3-State Outputs	219
SCL4510B	BCD Decade Programmable Up/Down Counter	222
SCL4511B	BCD-to-7 Segment Latch/Decoder/Driver	226
SCL4512B	8-Channel Data Selector	229
SCL4514B	4-to-16 Line Decoder with Latch (Active High Outputs)	233
SCL4515B	4-to-16 Line Decoder with Latch (Active Low Outputs)	233
SCL4516B	4-Stage Binary Programmable Up/Down Counter	236
SCL4518B	Dual BCD Decade Up Counter	240
SCL4520B	Dual 4-Stage Binary Up Counter	240
SCL4522B	BCD Decade Programmable Down Counter	243
SCL4526B	4-Stage Binary Programmable Down Counter	243
SCL4527B	BCD Rate Multiplier	247
SCL4528B	Dual Monostable Multivibrator	251
SCL4531B	12-Bit Parity Tree	255
SCL4543B	BCD-to-7 Segment Latch/Decoder/Driver	257
SCL4555B	Dual 2-to-4 Line Decoder (Active High Outputs)	260
SCL4556B	Dual 2-to-4 Line Decoder (Active Low Outputs)	260
SCL4581B	4-Bit Arithmetic Logic Unit	263
SCL4582B	Look-Ahead Carry Block	267
SCL4585B	4-Bit Magnitude Comparator	269

CROSS REFERENCE GUIDE

SSS	RCA	MOTOROLA	NATIONAL*	FAIRCHILD	HARRIS*	TEXAS INSTRUMENTS	SOLITRON
SCL4000B	CD4000A ¹	MC14000 ¹				TP4000A ¹	
SCL4001B		MC14001B		F4001			
SCL4001UB	CD4001A	MC14001	CD4001A		HD4001A	TP4001A	CM4001A
SCL4002B	CD4002A ¹	MC14002B	CD4002A ¹	F4002	HD4002A ¹	TP4002A ¹	CM4002A ¹
SCL4006AB	CD4006A	MC14006	CD4006A	F4006	HD4006A		CM4006A
SCL4007UB	CD4007A	MC14007	CD4007A	F4007	HD4007A	TP4007A	CM4007A
SCL4008B	CD4008A	MC14008		F4008	HD4008A	TP4008A	CM4008A
SCL4009UB	CD4009A		CD4009A			TP4009A	
SCL4010B	CD4010A		CD4010A			TP4010A	
SCL4011B		MC14011B		F4011			
SCL4011UB	CD4011A	MC14011	CD4011A		HD4011A	TP4011A	CM4011A
SCL4012B	CD4012A ¹	MC14012B	CD4012A ¹	F4012	HD4012A ¹	TP4012A ¹	CM4012A ¹
SCL4013B	CD4013A	MC14013	CD4013A	F4013	HD4013A	TP4013A	CM4013A
SCL4014B	CD4014A	MC14014	CD4014A	F4014	HD4014A	TP4014A	CM4014A
SCL4015B	CD4015A	MC14015	CD4015A	F4015	HD4015A	TP4015A	
SCL4016AB	CD4016A	MC14016	CD4016A	F4016		TP4016A	CM4016A
SCL4017AB	CD4017A	MC14017	CD4017A	F4017	HD4017A	TP4017A	CM4017A
SCL4018B	CD4018A	MC14018	CD4018A	F4018	HD4018A	TP4018A	CM4018A
SCL4019B	CD4019A		CD4019A	F4019	HD4019A	TP4019A	CM4019A
SCL4020AB	CD4020A	MC14020	CD4020A	F4020	HD4020A	TP4020A	CM4020A
SCL4021B	CD4021A	MC14021	CD4021A	F4021	HD4021A	TP4021A	CM4021A
SCL4022AB	CD4022A	MC14022	CD4022A	F4022	HD4022A	TP4022A	CM4022A
SCL4023B	CD4023A ¹	MC14023B	CD4023A ¹	F4023	HD4023A ¹	TP4023A ¹	CM4023A ¹
SCL4024B	CD4024A	MC14024	CD4024A	F4024	HD4024A	TP4024A	CM4024A
SCL4025B	CD4025A ¹	MC14025B	CD4025A ¹	F4025	HD4025A ¹	TP4025A ¹	CM4025A ¹
SCL4026AB	CD4026A						
SCL4027B	CD4027A	MC14027	CD4027A	F4027	HD4027A	TP4027A	
SCL4028B	CD4028A	MC14028	CD4028A	F4028	HD4028A	TP4028A	
SCL4029B	CD4029A		CD4029A	F4029	HD4029A	TP4029A	
SCL4030B	CD4030A		CD4030A	F4030	HD4030A	TP4030A	
SCL4033AB	CD4033A						
SCL4034AB	CD4034A	MC14034					
SCL4035B	CD4035A	MC14035	CD4035A	F4035	HD4035A	TP4035A	
SCL4040AB	CD4040A	MC14040	CD4040A	F4040	HD4040A	TP4040A	
SCL4041UB	CD4041A			F4041		TP4041A	CM4041A

*74C types are listed only if pin-compatible

CROSS REFERENCE GUIDE (continued)

SSS	RCA	MOTOROLA	NATIONAL*	FAIRCHILD	HARRIS*	TEXAS INSTRUMENTS	SOLITRON
SCL4042B	CD4042A	MC14042	CD4042A	F4042	HD4042A	TP4042A	CM4043A CM4044A
SCL4043AB	CD4043A	MC14043	CD4043A	F4043	HD4043A	TP4043A	
SCL4044AB	CD4044A	MC14044	CD4044A	F4044	HD4044A	TP4044A	
SCL4046B	CD4046A	MC14046	CD4046A	F4046			
SCL4049UB	CD4049A	MC14049	CD4049A	F4049	HD4049A	TP4049A	
SCL4050B	CD4050A	MC14050	CD4050A	F4050	HD4050A	TP4050A	
SCL4051B	CD4051A	MC14051	CD4051A	F4051		TP4051A	
SCL4052B	CD4052A	MC14052	CD4052A	F4052		TP4052A	
SCL4053B	CD4053A	MC14053	CD4053A	F4053		TP4053A	
SCL4060AB	CD4060A						
SCL4066B	CD4066B	MC14066	CD4066A	F4066	HD4066A		
SCL4068B	CD4068B	MC14068B		F4068			
SCL4069UB	CD4069B	MC14069	CD4069A	F4069	HD74C04		
SCL4070B	CD4070B	MC14070	CD4070A	F4070	HD74C86		
SCL4071B	CD4071B	MC14071B		F4071			
SCL4072B	CD4072B	MC14072B		F4072			
SCL4073B	CD4073B	MC14073B		F4073			
SCL4075B	CD4075B	MC14075B		F4075			
SCL4076B	CD4076B	MC14076	CD4076A	F4076	HD74C173		
SCL4077B	CD4077B	MC14077		F4077			
SCL4078B	CD4078B	MC14078B		F4078			
SCL4081B	CD4081B	MC14081B		F4081			
SCL4082B	CD4082B	MC14082B		F4082			
SCL4093B	CD4093B	MC14093					
SCL4160B		MC14160B	MM74C160	F40160	HD74C160	TP4360	
SCL4161B		MC14161B	MM74C161	F40161	HD74C161	TP4361	
SCL4162B		MC14162B	MM74C162	F40162	HD74C162	TP4362	
SCL4163B		MC14163B	MM74C163	F40163	HD74C163	TP4363	
SCL4402B							
SCL4404B							
SCL4412B							
SCL4416AB							
SCL4426AB							
SCL4428B							
SCL4433AB							

*74C types are listed only if pin-compatible

CROSS REFERENCE GUIDE (continued)

CROSS REFERENCE GUIDE (Continued)

SSS	RCA	MOTOROLA	NATIONAL*	FAIRCHILD	HARRIS*	TEXAS INSTRUMENTS	SOLITRON
SCL4441UB							
SCL4445B	CD4045A ²						
SCL4446B							
SCL4449UB							
SCL4502B	CD4502B	MC14502					
SCL4508B	CD4508B	MC14508					
SCL4510B	CD4510B	MC14510	CD14510	F4510			
SCL4511B	CD4511B	MC14511	CD14511	F4511			
SCL4512B		MC14512		F4512		TP4512A	
SCL4514B	CD4514B	MC14514		F4514		TP4514A	
SCL4515B	CD4515B	MC14515		F4515		TP4515A	
SCL4516B	CD4516B	MC14516	CD14516	F4516			
SCL4518B	CD4518B	MC14518		F4518		TP4518A	
SCL4520B	CD4520B	MC14520		F4520		TP4520A	
SCL4522B		MC14522		F4522		TP4522A	
SCL4526B		MC14526		F4526		TP4526A	
SCL4527B	CD4527B	MC14527					
SCL4528B	CD4098B ³	MC14528		F4528			
SCL4531B		MC14531		F4531		TP4531A	
SCL4543B	CD4056A ⁴	MC14543					
SCL4555B	CD4555B	MC14555		F4555			
SCL4556B	CD4556B	MC14556		F4556			
SCL4581B	CD40181B	MC14581	MM74C181			TP4581A	
SCL4582B	CD40182B	MC14582	MM74C182	F4582		TP4582A	
SCL4585B		MC14585					

NOTES: *Unbuffered versions

²Functional equivalent; CD4045A lacks f_o/4 output and internal resistors

³Functional equivalent; CD4098B has different output pulse width characteristics

⁴Pin-for-pin compatible if leads 7 and 8 are tied together

*74C types are listed only if pin-compatible

CROSS REFERENCE GUIDE (continued)

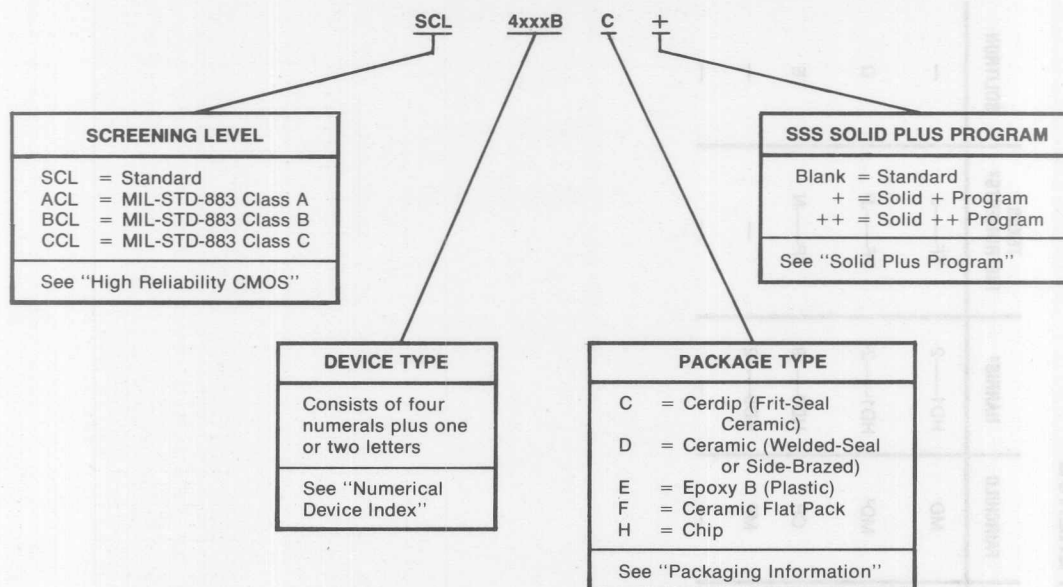
PACKAGE CODE CROSS REFERENCE

PACKAGE	TEMP RANGE ¹	SSS	RCA	MOTOROLA	NATIONAL	FAIRCHILD	HARRIS ²	TEXAS INSTRUMENTS ²	SOLITRON
Frit-Seal Ceramic (Cerdip)	Mil	C	F	AL	MJ	MD	HD1—2	TF—J	—
Welded-Seal or Side-Brazed Ceramic	Mil	D	D	AL	MD	MD ³	HD1—2 ³	TF—J ³	D
Epoxy B (Plastic)	Comm	E	E	CP	CN	CP	HD3—9	TP—N	E
Ceramic Flat Pack	Mil	F	K	—	MF	MF	HD9—2	—	—
Chip	Mil	H	H	—	—	—	—	—	—

NOTES: ¹Mil: -55° C to +125° C
Comm: -40° C to +85° C

2. Prefix—Suffix
3. 24-lead devices only

ORDERING INFORMATION



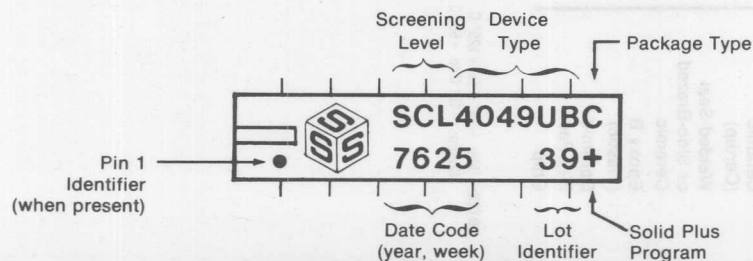
PACKAGING INFORMATION

Devices in the SCL4000 Series are available in a variety of package types and temperature ranges. The single-letter package designator appears as a suffix to the device type.

Designator ¹	Type	Style	No. of Pins	Temperature Range
C	Cerdip (Frit-Seal)	Dual-in-Line (DIP)	14, 16	-55° C to +125° C
D	Ceramic (Welded-Seal or Side-Brazed)	Dual-in-Line (DIP)	14, 16, 24	-55° C to +125° C
E	Epoxy B (Plastic)	Dual-in-Line (DIP)	14, 16, 24	-40° C to +85° C
F	Ceramic	Flat Pack	14, 16	-55° C to +125° C
H	Chip	—	—	-55° C to +125° C

Note: 1. For physical dimensions, see "Mechanical Specifications"

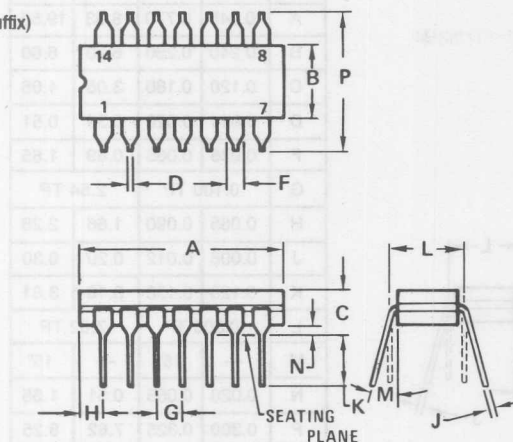
DEVICE MARKING



MECHANICAL SPECIFICATIONS

Cerdip Dual-in-Line Packages (C Suffix)

14-Lead
Frit Seal
(Cerdip)
DIP
(C suffix)



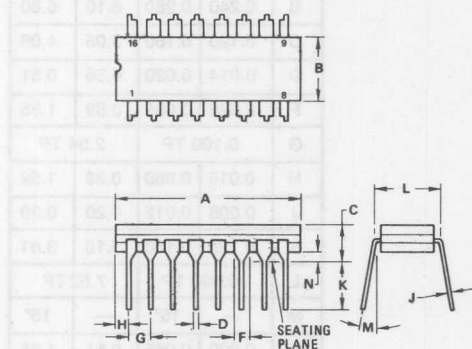
Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	0.660	0.785	16.8	19.9
B	0.220	0.280	5.59	7.11
C	0.155	0.200	3.94	5.08
D	0.014	0.023	0.36	0.58
F	0.030	0.070	0.77	1.77
G	0.100 TP		2.54 TP	
H	0.065	0.090	1.66	2.28
J	0.008	0.015	0.20	0.38
K	0.100	0.150	2.54	3.81
L	0.300 TP		7.62 TP	
M	—	15°	—	15°
N	0.020	0.050	0.51	1.27
P	0.300	0.325	7.62	8.25

All JEDEC dimensions and notes apply.

Notes:

1. Leads within 0.005" (0.13 mm) radius of true position at seating plane at maximum material condition.
2. Pkg. index: notch in lead, notch in ceramic, or ink dot.
3. Dim. "A" and "B" do not include glass run-out.
4. Dim. "L" to center of leads when formed parallel.

16-Lead
Frit-Seal
(Cerdip)
DIP
(C suffix)



Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	0.745	0.785	18.93	19.93
B	0.240	0.275	6.10	6.98
C	0.155	0.200	3.94	5.08
D	0.014	0.020	0.36	0.51
F	0.035	0.065	0.89	1.65
G	0.100 TP		2.54 TP	
H	0.015	0.060	0.39	1.52
J	0.008	0.012	0.20	0.30
K	0.100	0.160	2.54	4.06
L	0.300 TP		7.62 TP	
M	—	15°	—	15°
N	0.020	0.050	0.51	1.27

All JEDEC dimensions and notes apply.

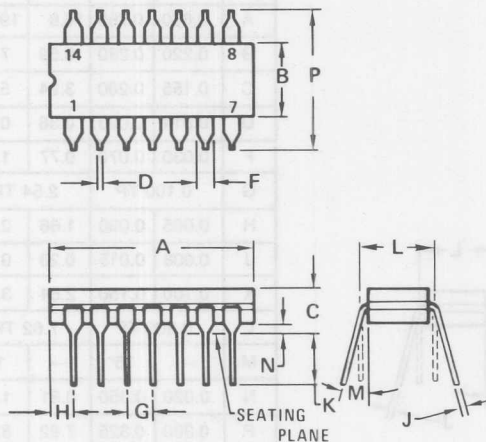
Notes:

1. Leads within 0.005" (0.13 mm) radius of true position at seating plane at maximum material condition.
2. Pkg. index: notch in lead, notch in ceramic, or ink dot.
3. Dim. "A" and "B" do not include glass run-out.
4. Dim. "F" applies to all leads except the four end leads, which have Dim. "F" = 0.025" (0.64 mm) min.
5. Dim. "L" to center of leads when formed parallel.

MECHANICAL SPECIFICATIONS (Continued)

Ceramic Dual-in-Line Packages (D Suffix)

14-Lead
Welded-Seal
Ceramic DIP
(D suffix)



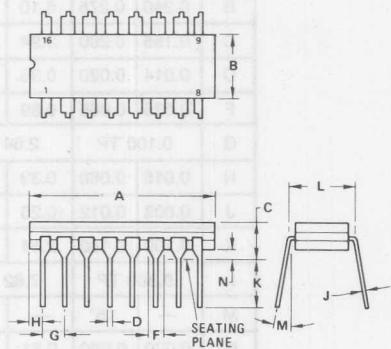
Notes:

1. Leads within 0.005" (0.13 mm) radius of true position at seating plane at maximum material condition.
2. Pkg. index: notch in lead, notch in lid, or ink dot.
3. Dim. "L" to center of leads when formed parallel.

Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	0.745	0.770	18.93	19.55
B	0.240	0.260	6.10	6.60
C	0.120	0.160	3.05	4.06
D	0.014	0.020	0.36	0.51
F	0.035	0.065	0.89	1.65
G	0.100 TP		2.54 TP	
H	0.065	0.090	1.66	2.28
J	0.008	0.012	0.20	0.30
K	0.125	0.150	3.18	3.81
L	0.300 TP		7.62 TP	
M	—	15°	—	15°
N	0.020	0.065	0.51	1.65
P	0.300	0.325	7.62	8.25

All JEDEC dimensions and notes apply.

16-Lead
Welded-Seal
Ceramic DIP
(D suffix)



Notes:

1. Leads within 0.005" (0.13 mm) radius of true position at seating plane at maximum material condition.
2. Pkg. index: notch in lead, notch in lid, or ink dot.
3. Dim. "L" to center of leads when formed parallel.

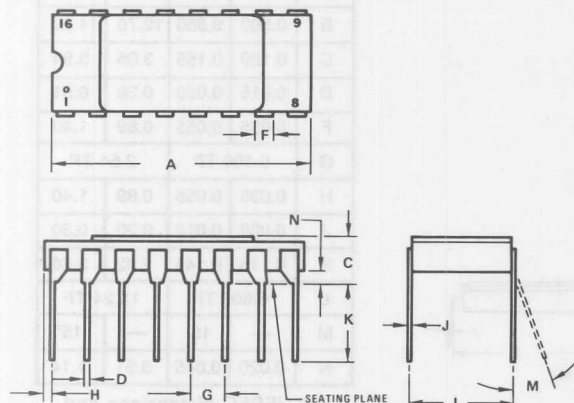
Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	0.745	0.785	18.93	19.93
B	0.240	0.260	6.10	6.60
C	0.120	0.160	3.05	4.06
D	0.014	0.020	0.36	0.51
F	0.035	0.065	0.89	1.65
G	0.100 TP		2.54 TP	
H	0.015	0.060	0.39	1.52
J	0.008	0.012	0.20	0.30
K	0.125	0.150	3.18	3.81
L	0.300 TP		7.62 TP	
M	—	15°	—	15°
N	0.020	0.065	0.51	1.65

All JEDEC dimensions and notes apply.

MECHANICAL SPECIFICATIONS (Continued)

Ceramic Dual-in-Line Packages (D Suffix)

16-Lead
Side-Brazed
Ceramic DIP
(D suffix)



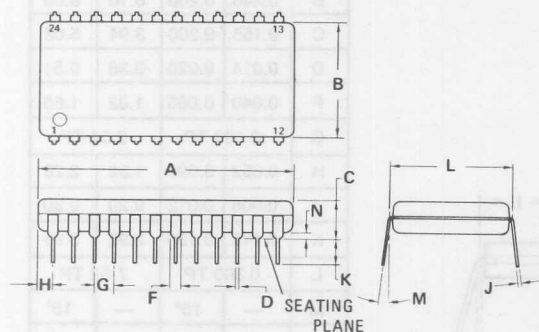
Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	0.740	0.830	18.80	21.08
C	0.105	0.200	2.67	5.08
D	0.015	0.023	0.38	0.58
F	0.045	0.055	1.14	1.40
G	0.100 TP		2.54 TP	
H	0.015	0.090	0.39	2.28
J	0.008	0.012	0.20	0.30
K	0.125	0.190	3.18	4.83
L	0.300 TP		7.62 TP	
M	—	15°	—	15°
N	0.020	0.045	0.51	1.14

All JEDEC dimensions and notes apply.

Notes:

1. Leads within 0.005" (0.13 mm) radius of true position at seating plane at maximum material condition.
2. Pkg. index: notch in lead, notch in ceramic, or ink dot.
3. Dim. "F" on four end leads = 0.025" (0.64 mm) min.
4. Dim. "L" to center of leads when formed parallel.

24-Lead
Welded-Seal
Ceramic DIP
(D suffix)



Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	1.15	1.22	29.21	30.98
B	0.480	0.520	12.20	13.20
C	0.090	0.150	2.29	3.81
D	0.015	0.020	0.38	0.51
F	0.045	0.055	1.14	1.40
G	0.100 TP		2.54 TP	
H	0.020	0.060	0.51	1.52
J	0.008	0.012	0.20	0.30
K	0.100	0.180	2.54	4.57
L	0.600 TP		15.24 TP	
M	—	15°	—	15°
N	0.020	0.065	0.51	1.65

All JEDEC dimensions and notes apply.

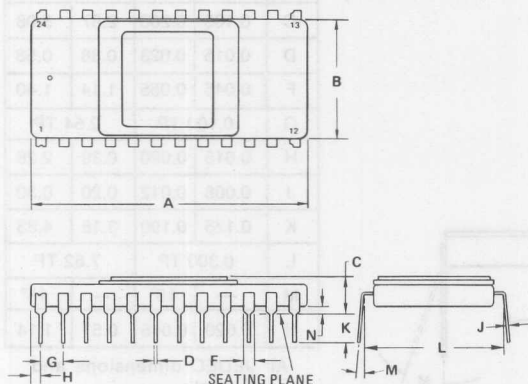
Notes:

1. Leads within 0.005" (0.13 mm) radius of true position at seating plane at maximum material condition.
2. Pkg. index: notch in lead, notch in lid, or ink dot.
3. Dim. "L" to center of leads when formed parallel.

MECHANICAL SPECIFICATIONS (Continued)

Ceramic Dual-in-Line Packages (D Suffix)

24-Lead
Side-Brazed
Ceramic DIP
(D suffix)



Notes:

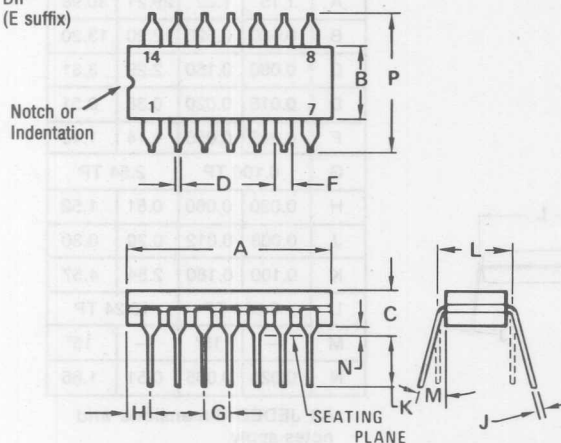
1. Leads within 0.005" (0.13 mm) radius of true position at seating plane at maximum material condition.
2. Pkg. index: notch in lead, notch in ceramic, or ink dot.
3. Dim. "L" to center of leads when formed parallel.

Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	1.15	1.22	29.21	30.98
B	0.500	0.560	12.70	14.22
C	0.120	0.155	3.05	3.94
D	0.015	0.020	0.38	0.51
F	0.035	0.055	0.89	1.40
G	0.100 TP		2.54 TP	
H	0.035	0.055	0.89	1.40
J	0.008	0.012	0.20	0.30
K	0.115	0.145	2.92	3.68
L	0.600 TP		15.24 TP	
M	—	15°	—	15°
N	0.020	0.045	0.51	1.14

All JEDEC dimensions and notes apply.

Epoxy B (Plastic) Dual-in-Line Packages (E Suffix)

14-Lead
Epoxy B
(Plastic)
DIP
(E suffix)



Notes:

1. Leads within 0.005" (0.13 mm) radius of true position at seating plane at maximum material condition.
2. Pkg. index: notch or indentation as shown.
3. Dim. "L" to center of leads when formed parallel.

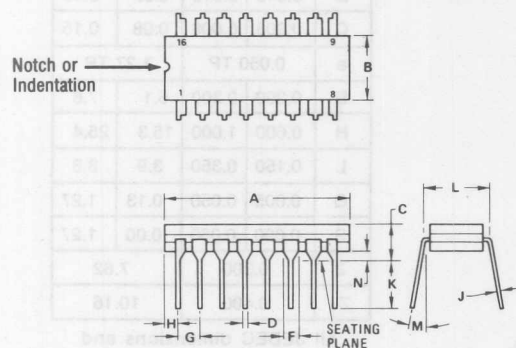
Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	0.715	0.770	18.16	19.55
B	0.240	0.260	6.10	6.60
C	0.155	0.200	3.94	5.08
D	0.014	0.020	0.36	0.51
F	0.040	0.065	1.02	1.65
G	0.100 TP		2.54 TP	
H	0.052	0.090	1.32	2.28
J	0.008	0.012	0.20	0.30
K	0.115	0.150	2.92	3.81
L	0.300 TP		7.62 TP	
M	—	15°	—	15°
N	0.020	0.050	0.51	1.27
P	0.300	0.325	7.62	8.25

All JEDEC dimensions and notes apply.

MECHANICAL SPECIFICATIONS (Continued)

Epoxy B (Plastic) Dual-in-Line Packages (E Suffix)

16-Lead
Epoxy B
(Plastic)
DIP
(E suffix)



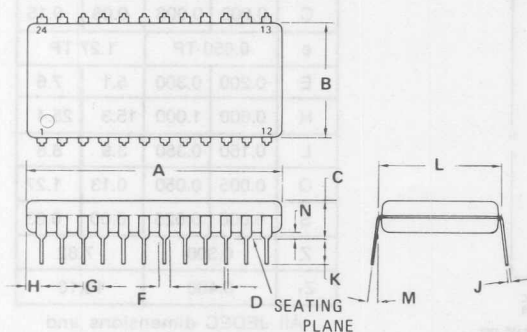
Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	0.745	0.840	18.93	21.94
B	0.240	0.260	6.10	6.60
C	0.155	0.200	3.94	5.08
D	0.014	0.020	0.36	0.51
F	0.035	0.065	0.89	1.65
G	0.100 TP		2.54 TP	
H	0.015	0.072	0.39	1.83
J	0.008	0.012	0.20	0.30
K	0.115	0.150	2.92	3.81
L	0.300 TP		7.62 TP	
M	—	15°	—	15°
N	0.020	0.050	0.51	1.27

All JEDEC dimensions and notes apply.

Notes:

1. Leads within 0.005" (0.13 mm) radius of true position at seating plane at maximum material condition.
2. Pkg. index: notch or indentation as shown.
3. Dim. "F" on four end leads = 0.025" (0.64 mm) min.
4. Dim. "L" to center of leads when formed parallel.

24-Lead
Epoxy B
(Plastic)
DIP
(E suffix)



Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	1.235	1.265	31.37	32.13
B	0.540	0.560	13.72	14.22
C	0.165	0.200	4.19	5.08
D	0.014	0.020	0.36	0.51
F	0.040	0.065	1.02	1.66
G	0.100 TP		2.54 TP	
H	0.065	0.090	1.66	2.28
J	0.008	0.012	0.20	0.30
K	0.115	0.140	2.93	3.56
L	0.600 TP		15.24 TP	
M	—	15°	—	15°
N	0.020	0.040	0.51	1.02

All JEDEC dimensions and notes apply.

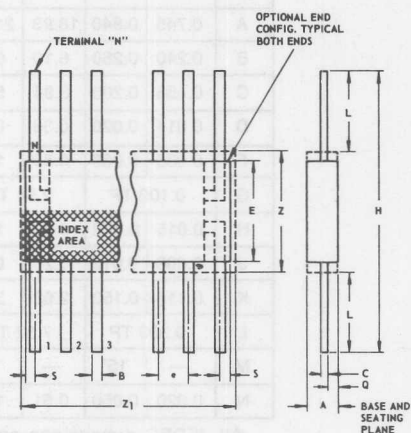
Notes:

1. Leads within 0.005" (0.13 mm) radius of true position at seating plane at maximum material condition.
2. Pkg. index: notch or indentation.
3. Dim. "F" on four end leads = 0.025" (0.64 mm) min.
4. Dim. "L" to center of leads when formed parallel.

MECHANICAL SPECIFICATIONS (Continued)

Ceramic Flat Packs (F Suffix)

14-Lead
Ceramic
Flat Pack
(F suffix)



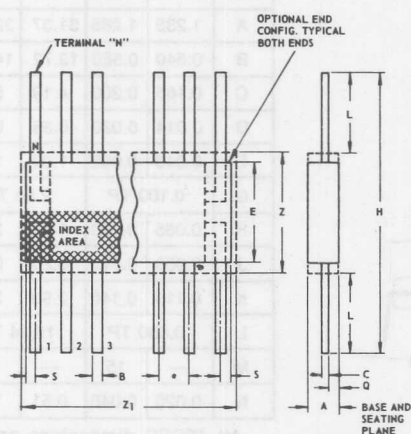
Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	0.008	0.100	0.21	2.54
B	0.015	0.019	0.38	0.48
C	0.003	0.006	0.08	0.15
e	0.050 TP		1.27 TP	
E	0.200	0.300	5.1	7.6
H	0.600	1.000	15.3	25.4
L	0.150	0.350	3.9	8.8
Q	0.005	0.050	0.13	1.27
S	0.000	0.050	0.00	1.27
Z	0.300		7.62	
Z ₁	0.400		10.16	

All JEDEC dimensions and notes apply.

Notes:

1. Leads within 0.005" (0.13 mm) radius of true position at seating plane at maximum material condition.
2. Pkg. index: tab on lead, notch in package, or ink dot.
3. Dim. "Z" and "Z₁" determine a zone within which all body and lead irregularities lie.

16-Lead
Ceramic
Flat Pack
(F suffix)

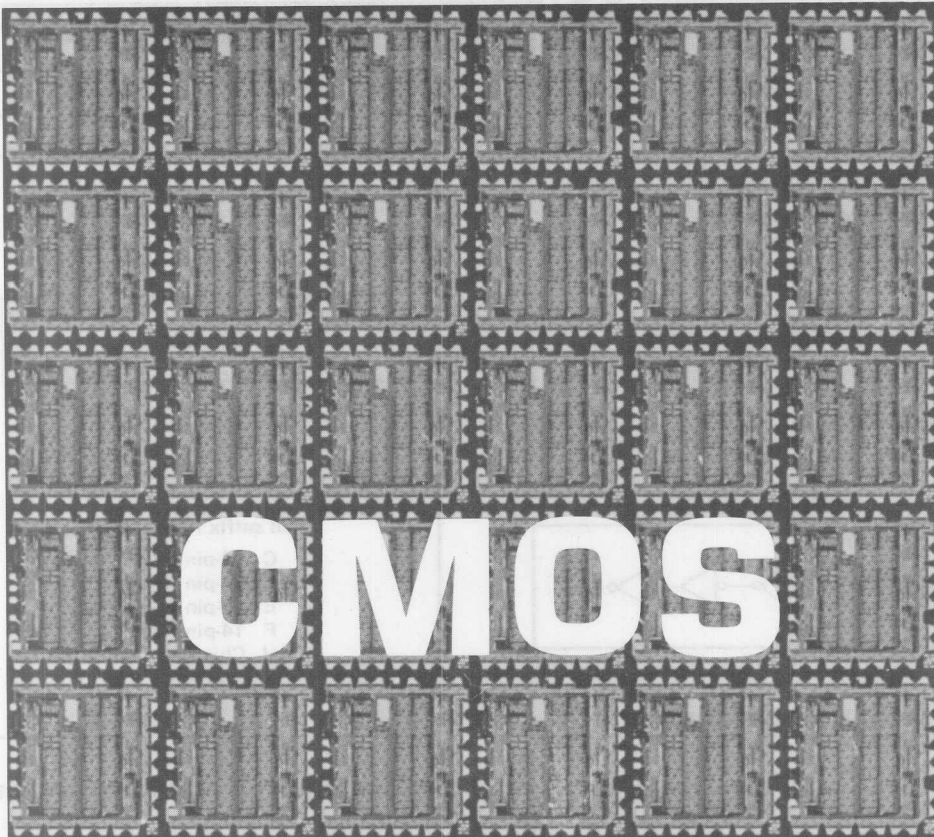


Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	0.008	0.100	0.21	2.54
B	0.015	0.019	0.38	0.48
C	0.003	0.006	0.08	0.15
e	0.050 TP		1.27 TP	
E	0.200	0.300	5.1	7.6
H	0.600	1.000	15.3	25.4
L	0.150	0.350	3.9	8.8
Q	0.005	0.050	0.13	1.27
S	0.000	0.025	0.00	0.63
Z	0.300		7.62	
Z ₁	0.400		10.16	

All JEDEC dimensions and notes apply.

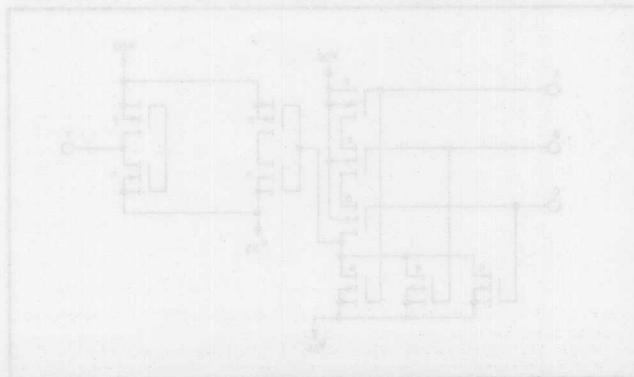
Notes:

1. Leads within 0.005" (0.13 mm) radius of true position at seating plane at maximum material condition.
2. Pkg. index: tab on lead, notch in package, or ink dot.
3. Dim. "Z" and "Z₁" determine a zone within which all body and lead irregularities lie.



CMOS

PRODUCT DATA SHEETS



SCL4000B



CMOS DUAL 3-INPUT NOR GATE PLUS INVERTER

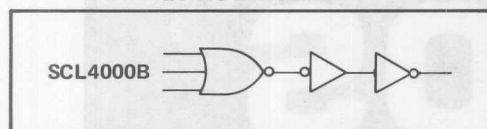
FEATURES

- ◆ Buffered Gate Outputs
- ◆ Diode Protection on all Inputs
- ◆ Fully "B" Series Compatible
- ◆ Balanced Output Drive Current Specifications

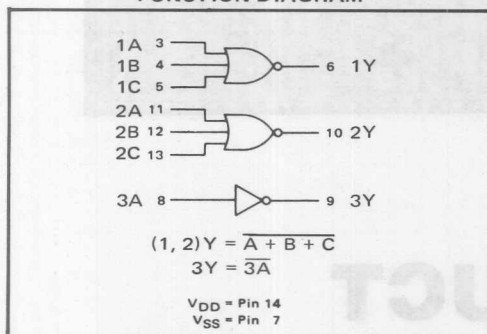
TRUTH TABLE (NOR GATE)

INPUTS	OUTPUT
0 0 0	1
All other combinations	0

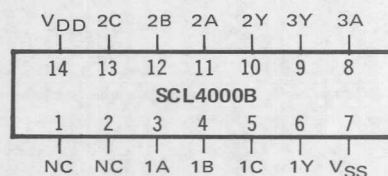
LOGIC DIAGRAM



FUNCTION DIAGRAM



CONNECTION DIAGRAM (all packages)



Add suffix for package:

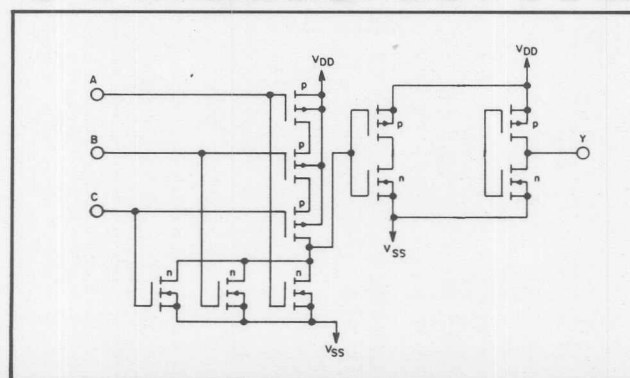
- C 14-pin Cerdip
- D 14-pin Ceramic
- E 14-pin Epoxy
- F 14-pin Flat
- H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A	-55 to +125	°C
C, D, F, H Device		-40 to +85	°C

SCHEMATIC DIAGRAM (One of two NOR Gates)



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS^{1,3}

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	V _{IN} =V _{SS} or V _{DD} All valid input combinations	—	0.05	—	0.0005	0.05	—	1.5	μAdc
			—	0.10	—	0.001	0.10	—	3.0	
			—	0.20	—	0.002	0.20	—	6.0	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

² T_{LOW} = -55°C for C, D, F, H device.

= -40°C for E device.

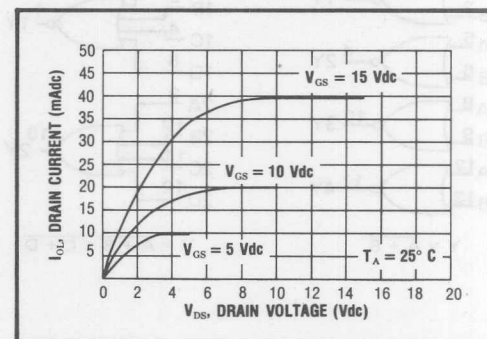
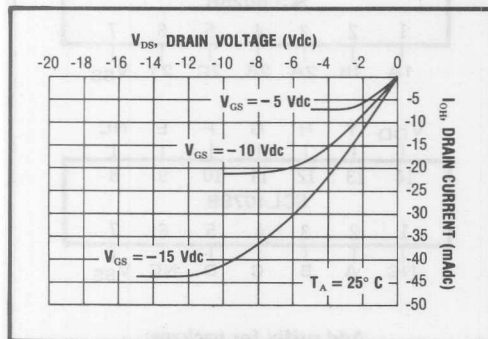
T_{HIGH} = +125°C for C, D, F, H device.

= + 85°C for E device.

³ This device has been designed for balanced output drive current specifications. Consult Family Specifications.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V _{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME	t _{PLH} , t _{PHL}	5	—	125	250	ns
		10	—	60	120	
		15	—	45	90	
OUTPUT TRANSITION TIME	t _{TLH} , t _{THL}	5	—	100	200	ns
		10	—	50	100	
		15	—	40	80	



**SCL4001B, SCL4002B
SCL4025B, SCL4078B**



CMOS NOR GATES

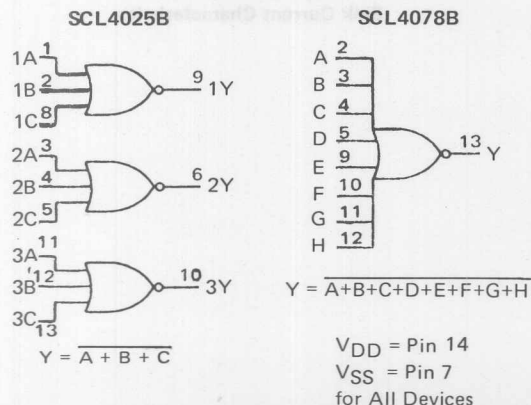
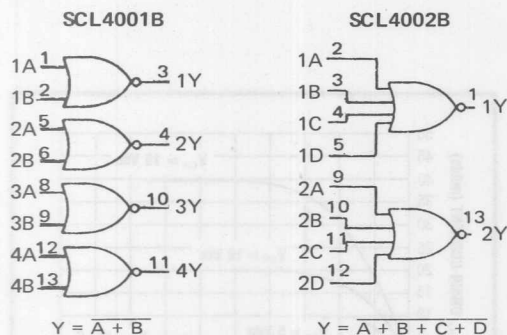
SCL4001B – Quad 2-Input NOR
SCL4002B – Dual 4-Input NOR
SCL4025B – Triple 3-Input NOR
SCL4078B – 8-Input NOR

FEATURES

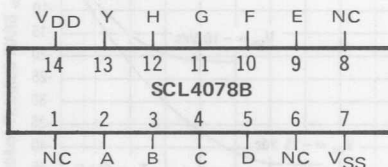
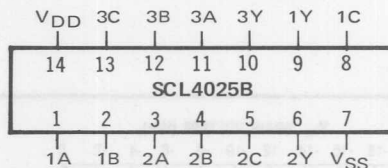
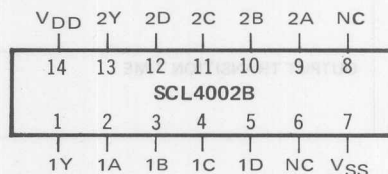
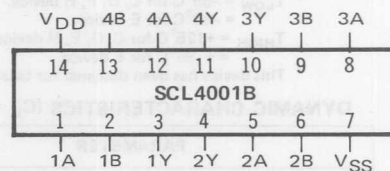
- ◆ Buffered Outputs
- ◆ Diode Protection on all Inputs
- ◆ Fully "B" - Series Compatible
- ◆ Balanced Output Drive Current Specifications

Inputs	Output
0 0 . . . 0	1
All other combinations	0

FUNCTION DIAGRAMS



CONNECTION DIAGRAMS (all packages)



Add suffix for package:

- C 14-pin Cerdip
- D 14-pin Ceramic
- E 14-pin Epoxy
- F 14-pin Flat
- H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	V_{dc}
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	$^{\circ}C$
E Device		-40 to +85	$^{\circ}C$

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS^{1,3}

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	5 V _{IN} =V _{SS} or V _{DD}	—	0.05	—	0.0005	0.05	—	1.5	μAdc
		10 All valid input combinations	—	0.10	—	0.001	0.10	—	3.0	
		15	—	0.20	—	0.002	0.20	—	6.0	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

² T_{LOW} = -55°C for C, D, F, H device.

= -40°C for E device.

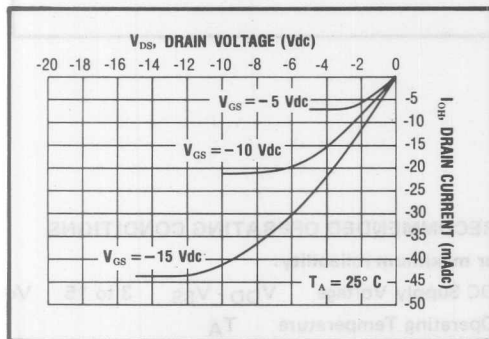
T_{HIGH} = +125°C for C, D, F, H device.

= + 85°C for E device.

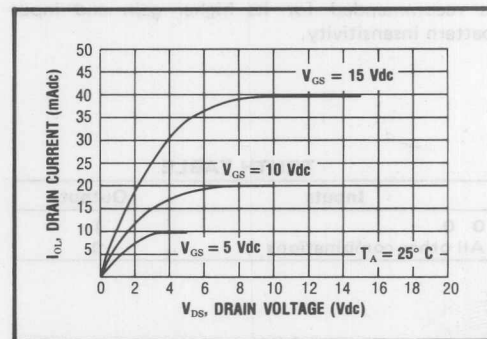
³ These devices have been designed for balanced output drive current specifications. Consult Family Specifications.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V _{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME	t _{PLH} , t _{PHL}	5	—	125	250	ns
		10	—	60	120	
		15	—	45	90	
OUTPUT TRANSITION TIME	t _{TLH} , t _{THL}	5	—	100	200	ns
		10	—	50	100	
		15	—	40	80	

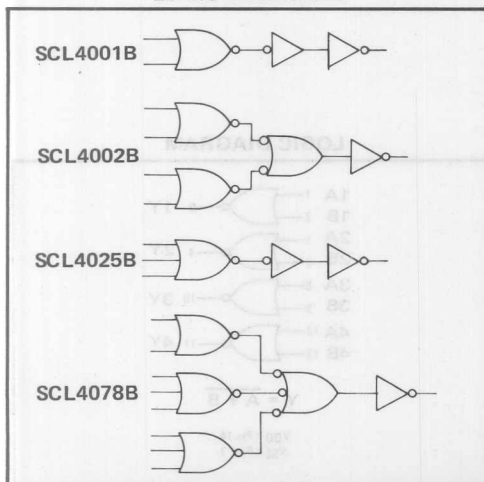


Typical P-Channel
Source Current Characteristics

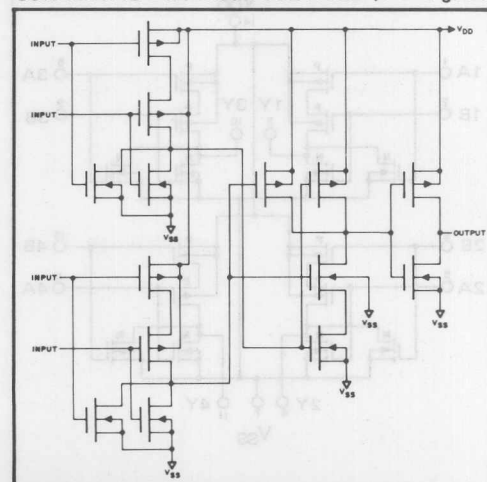


Typical N-Channel
Sink Current Characteristics

LOGIC DIAGRAMS



SCHEMATIC DIAGRAM SCL4002B (1 of 2 gates)



SCL4001UB



CMOS NOR GATE (Unbuffered)

FEATURES

- ◆ Unbuffered Outputs for Quasi-Linear Applications
- ◆ Quad 2-Input NOR Configuration
- ◆ Diode Protection on all Inputs
- ◆ Output Drive Current Compatible with "B" Series
- ◆ Pin Compatible with Buffered SCL4001B
- ◆ Balanced Output Drive Current Specifications

DESCRIPTION

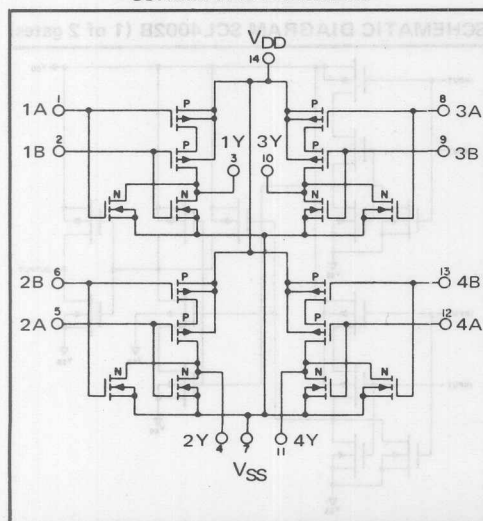
The SCL4001UB consists of four positive-logic NOR gates. The outputs are unbuffered, making the device suitable for quasi-linear applications, such as gated oscillators, multivibrators, and pulse shaping circuits.

For digital applications, the buffered SCL4001B is recommended for its higher gain and input pattern insensitivity.

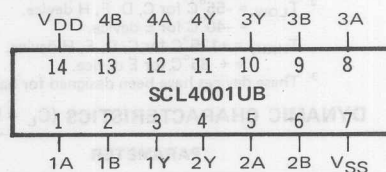
TRUTH TABLE

Inputs	Output
0 0	1
All other combinations	0

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM (all packages)



Add suffix for package:

- C 14-pin Cerdip
- D 14-pin Ceramic
- E 14-pin Epoxy
- F 14-pin Flat
- H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

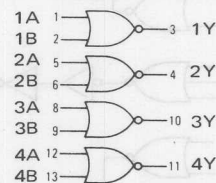
DC Supply Voltage $V_{DD} - V_{SS}$ 3 to 15 Vdc

Operating Temperature T_A

C, D, F, H Device -55 to +125 °C

E Device -40 to +85 °C

LOGIC DIAGRAM



$$Y = \overline{A + B}$$

V_{DD} = Pin 14

V_{SS} = Pin 7

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS^{1, 3}

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	V _{IN} = V _{SS} or V _{DD} All valid input combinations	—	0.05	—	0.0005	0.05	—	1.5	μAdc
			—	0.10	—	0.001	0.10	—	3.0	
			—	0.20	—	0.002	0.20	—	6.0	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

² T_{LOW} = -55°C for C, D, F, H device.

= -40°C for E device.

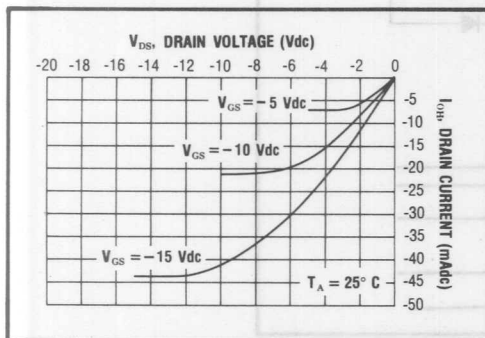
T_{HIGH} = +125°C for C, D, F, H device.

= + 85°C for E device.

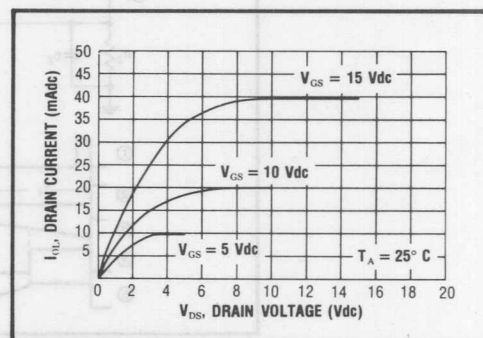
³ This device has been designed for balanced output drive current specifications. Consult Family Specifications.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V _{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME	t _{PLH} , t _{PHL}	5	—	75	150	ns
		10	—	35	70	
		15	—	25	50	
OUTPUT TRANSITION TIME	t _{TLH} , t _{THL}	5	—	100	200	ns
		10	—	50	100	
		15	—	40	80	

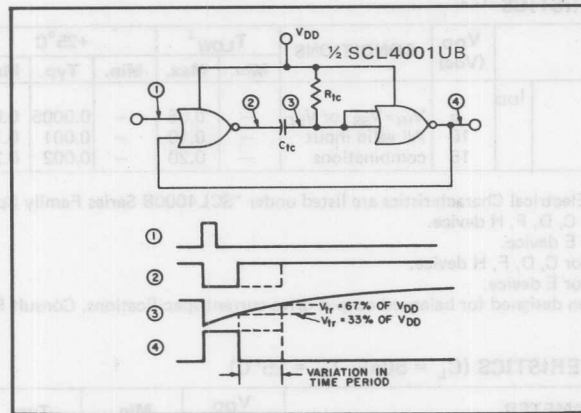


Typical P-Channel
Source Current Characteristics

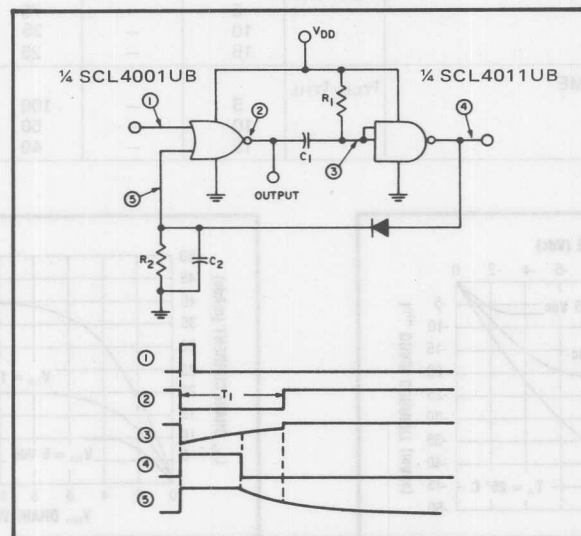


Typical N-Channel
Sink Current Characteristics

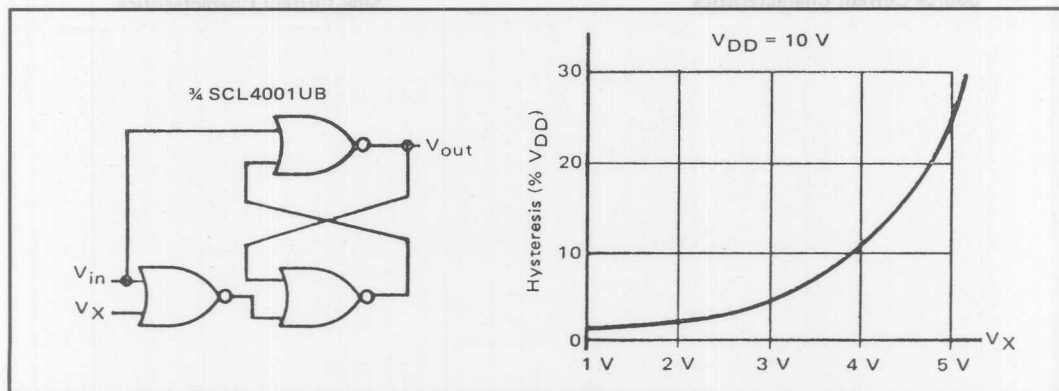
APPLICATIONS INFORMATION



MONOSTABLE MULTIVIBRATOR



COMPENSATED MONOSTABLE MULTIVIBRATOR



SCHMITT TRIGGER



FEATURES

- ◆ Fully Static Operation
- ◆ Cascadable
- ◆ 5MHz Shift Rate @ 10Vdc

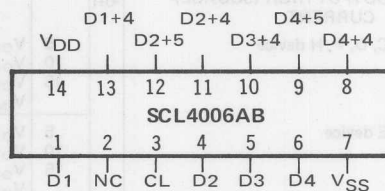
DESCRIPTION

The SCL4006AB is comprised of 4 separate Shift Register sections: two sections of four stages and two sections of five stages with an output tap at the fourth stage. Each section has an independent single rail data path.

A common Clock signal is used for all stages. Data is shifted to the next stage on negative-going transitions of the Clock. Through appropriate connections of inputs and outputs, multiple register sections of 4, 5, 8 and 9 stages or single register sections of 10, 12, 13, 14, 16, 17 and 18 can be implemented using one SCL4006AB package. Longer shift register sections can be assembled by using more than one SCL4006AB.

This part is useful in serial shift register and time delay circuits.

CONNECTION DIAGRAM (all packages)



Add suffix for package:

- C 14-pin Cerdip
- D 14-pin Ceramic
- E 14-pin Epoxy
- F 14-pin Flat
- H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

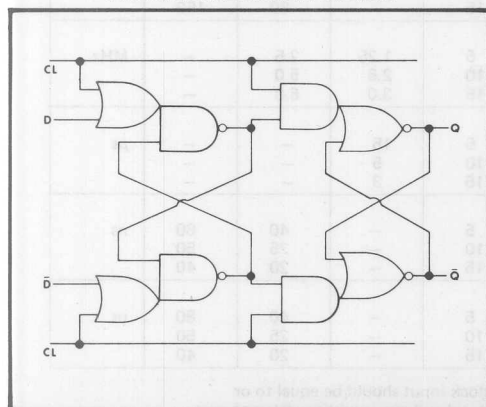
DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A	-55 to +125	°C
C, D, F, H Device		-40 to +85	°C
E Device			

TRUTH TABLE

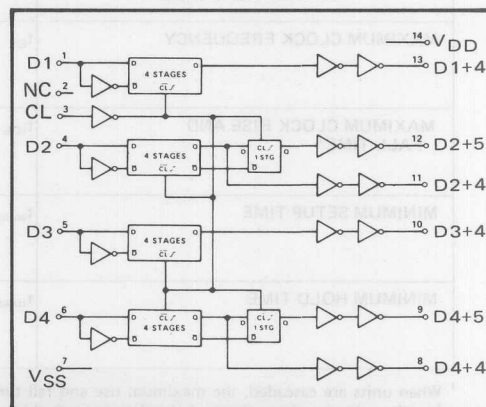
D_i	CL	D_{i+1}
0		0
1		1
X		No Change

X = Don't care

TYPICAL REGISTER STAGE



LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS¹

PARAMETER	V _{DD} (V _{dc})	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	5	V _{IN} =V _{SS} or V _{DD}	—	5	—	0.05	5	—	150
		10	All valid input combinations	—	10	—	0.1	10	—	300
		15		—	20	—	0.2	20	—	600
OUTPUT HIGH (SOURCE) CURRENT C, D, F, H device	I _{OH}	5	V _{OH} = 4.6V	-0.10	—	-0.08	-0.24	—	-0.056	—
		10	V _{OH} = 9.5V	-0.25	—	-0.2	-0.6	—	-0.14	—
		15	V _{OH} = 13.5V	-1.13	—	-0.9	-2.5	—	-0.64	—
			V _{IN} =V _{SS} or V _{DD}							
		5	V _{OH} = 4.6V	-0.096	—	-0.08	-0.24	—	-0.064	—
		10	V _{OH} = 9.5V	-0.24	—	-0.2	-0.6	—	-0.16	—
E device		15	V _{OH} = 13.5V	-1.06	—	-0.9	-2.5	—	-0.72	—
			V _{IN} =V _{SS} or V _{DD}							
OUTPUT LOW (SINK) CURRENT C, D, F, H device	I _{OL}	5	V _{OL} = 0.4V	0.125	—	0.1	0.3	—	0.07	—
		10	V _{OL} = 0.5V	0.31	—	0.25	0.8	—	0.175	—
		15	V _{OL} = 1.5V	1.44	—	1.15	3.3	—	0.81	—
			V _{IN} =V _{SS} or V _{DD}							
		5	V _{OL} = 0.4V	0.12	—	0.1	0.3	—	0.08	—
		10	V _{OL} = 0.5V	0.3	—	0.25	0.8	—	0.2	—
E device		15	V _{OL} = 1.5V	1.37	—	1.15	3.3	—	0.93	—
			V _{IN} =V _{SS} or V _{DD}							

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

² T_{LOW} = -55°C for C, D, F, H device.

= -40°C for E device.

T_{HIGH} = +125°C for C, D, F, H device.

= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER	V _{DD} (V _{dc})	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME	t _{PLH} , t _{PHL}	5	—	350	ns
		10	—	150	
		15	—	120	
OUTPUT TRANSITION TIME	t _{TLH} , t _{THL}	5	—	350	ns
		10	—	175	
		15	—	150	
MINIMUM CLOCK PULSE WIDTH	PW _{CL}	5	—	200	ns
		10	—	100	
		15	—	80	
MAXIMUM CLOCK FREQUENCY	f _{CL}	5	1.25	2.5	MHz
		10	2.5	5.0	
		15	3.0	6.0	
MAXIMUM CLOCK RISE AND FALL TIME ¹	t _{RCL} , t _{FCL}	5	15	—	μs
		10	5	—	
		15	3	—	
MINIMUM SETUP TIME	t _{setup}	5	—	40	ns
		10	—	25	
		15	—	20	
MINIMUM HOLD TIME	t _{hold}	5	—	40	ns
		10	—	25	
		15	—	20	

¹ When units are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the transition times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitive load.



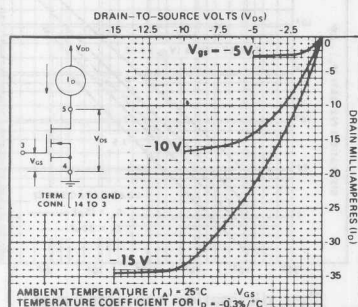
CMOS DUAL COMPLEMENTARY PAIR PLUS INVERTER

FEATURES

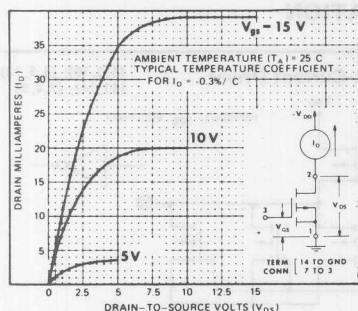
- ◆ Low Output Impedance
- ◆ Extremely High Input Impedance
- ◆ Single Supply Operation - Positive or Negative
- ◆ All Inputs Diode-Protected
- ◆ Balanced Output Drive Current Specifications

DESCRIPTION

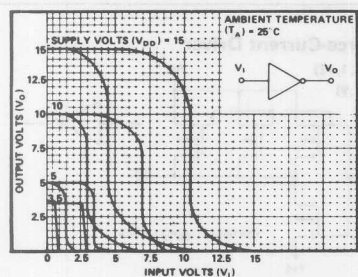
SCL4007UB contains three N-Channel and three P-Channel enhancement-type MOS transistors on a single monolithic silicon chip. The transistor elements are accessible through the package terminals to provide means for constructing various logic, transmission gating, and linear circuits.



Typ. P-Channel drain characteristics



Typ. N-Channel drain characteristics



Min. and max. voltage transfer characteristics for inverter

CONNECTION DIAGRAM (all packages)

V_{DD}	D-PA	OutC	S-PC	G_C	S-NC	D-NA
14	13	12	11	10	9	8
SCL4007UB						
1	2	3	4	5	6	7
D-PB	S-PB	G_B	S-NB	D-NB	G_A	V_{SS}
D = Drain S = Source G = Gate						

Add suffix for package:

- C 14-pin Cerdip
- D 14-pin Ceramic
- E 14-pin Epoxy
- F 14-pin Flat
- H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

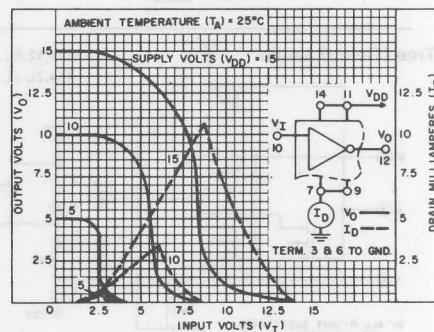
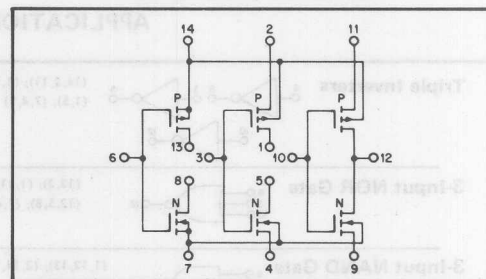
DC Supply Voltage $V_{DD} - V_{SS}$ 3 to 15 Vdc

Operating Temperature T_A

C, D, F, H Device -55 to +125 °C

E Device -40 to +85 °C

SCHEMATIC DIAGRAM



Typ. current and voltage transfer characteristics for inverter

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS^{1,3}

PARAMETER	V _{DD} (V _{dc})	CONDITIONS	T _{LOW} ²		+25°C		T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	
QUIESCENT DEVICE CURRENT	5	V _{IN} =V _{SS} or V _{DD}	—	0.05	—	0.0005	0.05	—	μAdc
	10	All valid input combinations	—	0.10	—	0.001	0.10	—	
	15		—	0.20	—	0.002	0.20	—	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".² T_{LOW} = -55°C for C, D, F, H device.

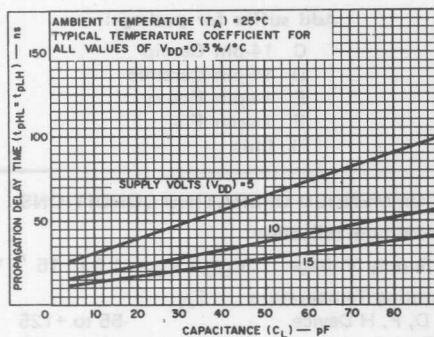
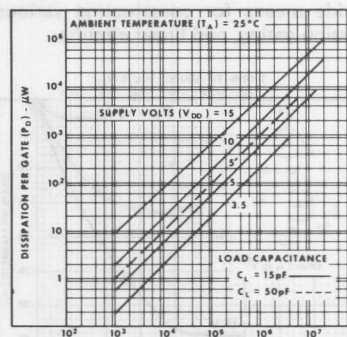
= -40°C for E device.

T_{HIGH} = +125°C for C, D, F, H device.

= + 85°C for E device.

³ This device has been designed for balanced output drive current specifications. Consult Family Specifications.DYNAMIC CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)¹

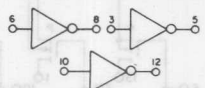
PARAMETER	V _{DD} (V _{dc})	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME					
	5	—	60	120	ns
	10	—	35	70	
OUTPUT TRANSITION TIME					
	5	—	100	200	ns
	10	—	50	100	
	15	—	40	80	

¹ Connected as inverterTyp. propagation delay time vs. C_L

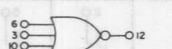
Typ. dissipation characteristics

APPLICATIONS INFORMATION

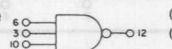
Triple Inverters

(14, 2, 11); (8, 13);
(1, 5); (7, 4, 9)

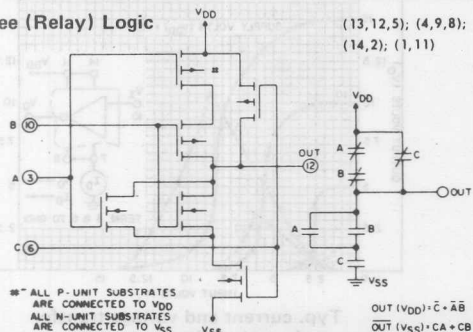
3-Input NOR Gate

(13, 2); (1, 11);
(12, 5, 8); (7, 4, 9)

3-Input NAND Gate

(1, 12, 13); (2, 14, 11);
(4, 8); (5, 9)

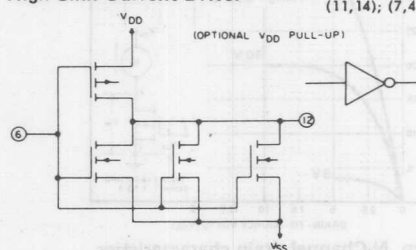
Tree (Relay) Logic

(13, 12, 5); (4, 9, 8);
(14, 2); (1, 11)

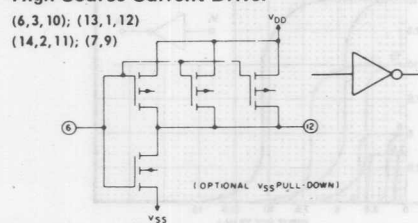
※ ALL P-UNIT SUBSTRATES
ARE CONNECTED TO V_{DD}
ALL N-UNIT SUBSTRATES
ARE CONNECTED TO V_{SS}

OUT (V_{DD}) = C · A · B
OUT (V_{SS}) = C · A · B

High Sink-Current Driver

(6, 3, 10); (8, 5, 12);
(11, 14); (7, 4, 9)

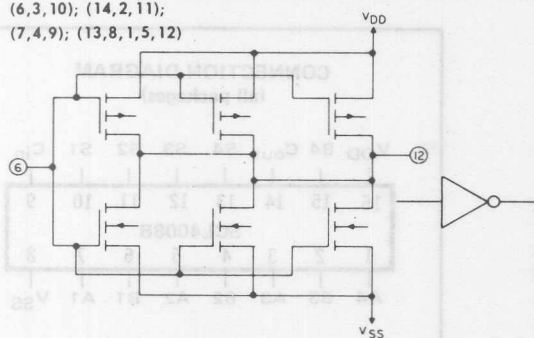
High Source-Current Driver

(6, 3, 10); (13, 1, 12)
(14, 2, 11); (7, 9)

APPLICATIONS INFORMATION (Continued)

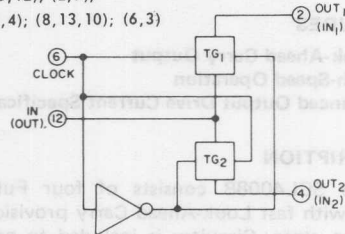
High Sink- and Source-Current Driver

(6,3,10); (14,2,11);
(7,4,9); (13,8,1,5,12)

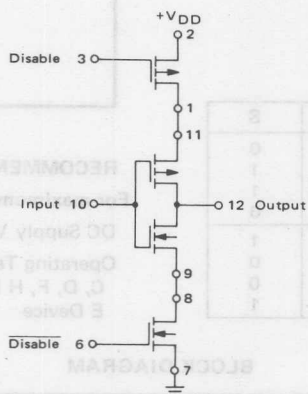


Dual Bi-Directional Transmission Gating

(1,5,12); (2,9);
(11,4); (8,13,10); (6,3)



3-State Buffer



INPUT	DISABLE	OUTPUT
1	0	0
0	0	1
X	1	Open

X = Don't Care



FEATURES

- ◆ Look-Ahead Carry Output
- ◆ High-Speed Operation
- ◆ Balanced Output Drive Current Specifications

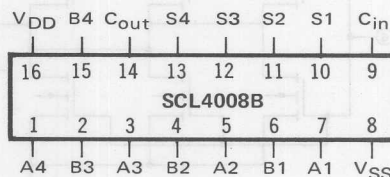
DESCRIPTION

The SCL4008B consists of four Full-Adder stages with fast Look-Ahead Carry provision from stage to stage. Circuitry is included to provide a fast Parallel-Carry-out bit to permit high-speed operation in arithmetic sections using several SCL4008B's. SCL4008B inputs include the four sets of bits to be added, A1 to A4 and B1 to B4, in addition to the Carry-in bit from a previous section. SCL4008B outputs include the four Sum bits, S1 and S4, in addition to the high-speed Parallel-Carry-out which may be utilized at a succeeding SCL4008B section.

TRUTH TABLE
(one stage)

C _{in}	B	A	C _{out}	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

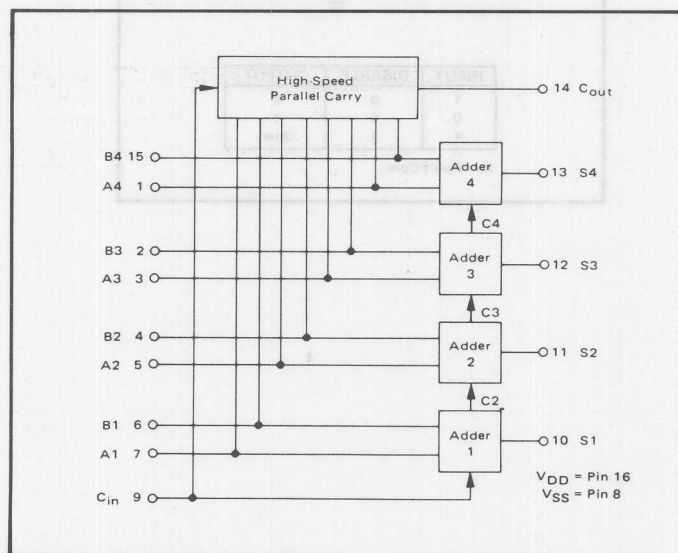
- C 16-pin Cerdip
- D 16-pin Ceramic
- E 16-pin Epoxy
- F 16-pin Flat
- H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A	-55 to +125	°C
C, D, F, H Device		-40 to +85	°C
E Device			

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS^{1, 3}

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	5	—	5	—	0.05	5	—	150	μAdc
		10	—	10	—	0.1	10	—	300	
		15	—	20	—	0.2	20	—	600	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

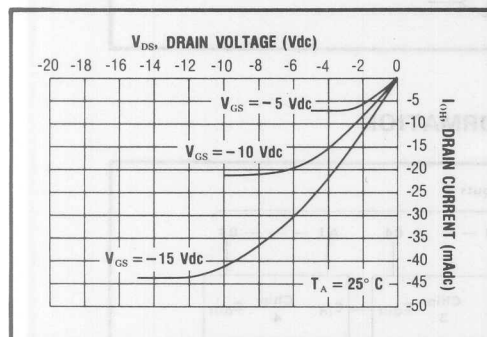
² T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.

T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

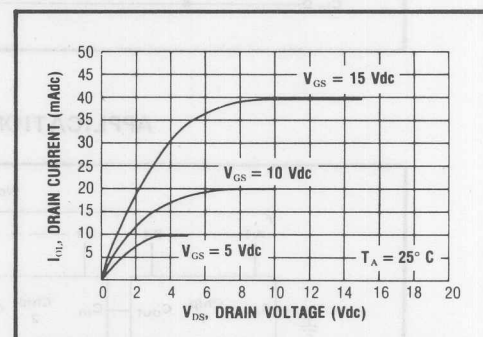
³ This device has been designed for balanced output drive current specifications. Consult Family Specifications.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER	V _{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME Sum In to Sum Out	t _{PLH} , t _{PHL}	5	—	400	ns
		10	—	160	
		15	—	115	
Sum In to Carry Out	t _{PLH} , t _{PHL}	5	—	310	ns
		10	—	140	
		15	—	110	
Carry In to Sum Out	t _{PLH} , t _{PHL}	5	—	380	ns
		10	—	150	
		15	—	115	
Carry In to Carry Out	t _{PLH} , t _{PHL}	5	—	180	ns
		10	—	75	
		15	—	55	
OUTPUT TRANSITION TIME	t _{TLH} , t _{THL}	5	—	100	ns
		10	—	50	
		15	—	40	

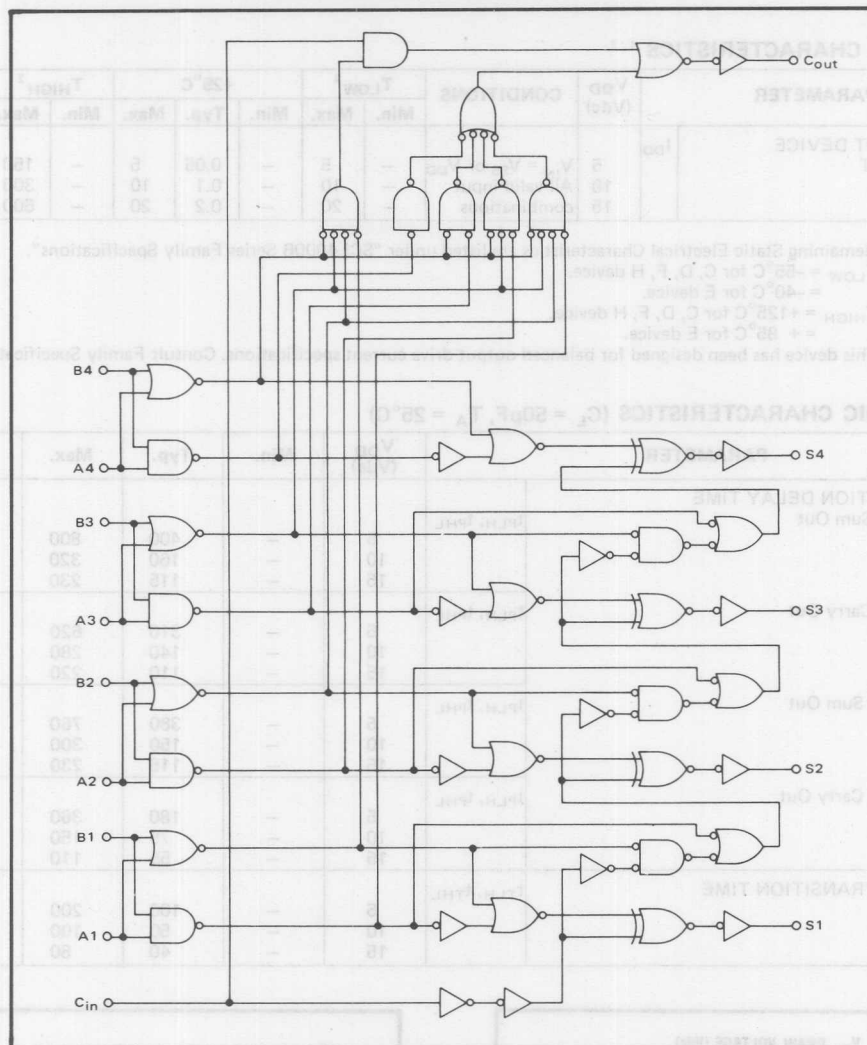


Typical P-Channel
Source Current Characteristics

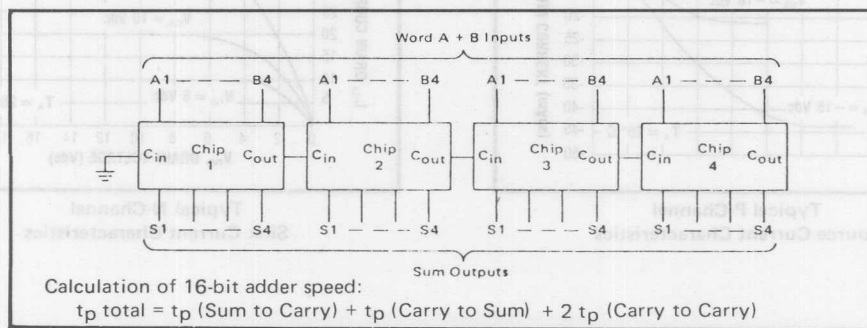


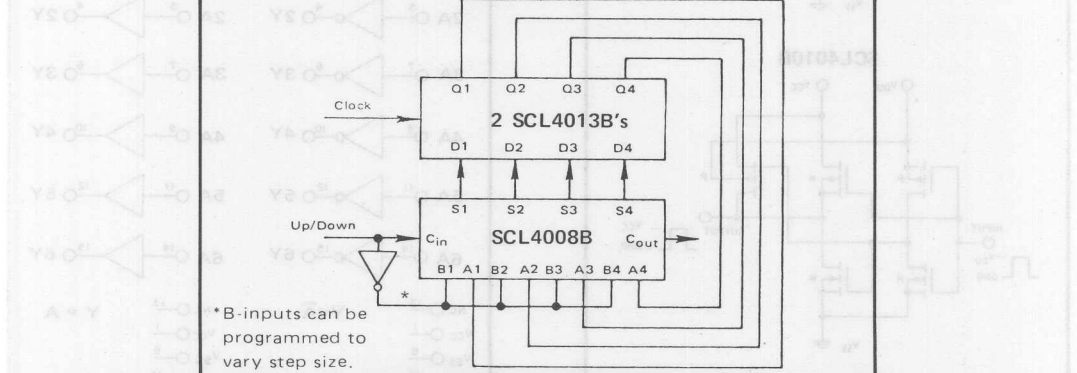
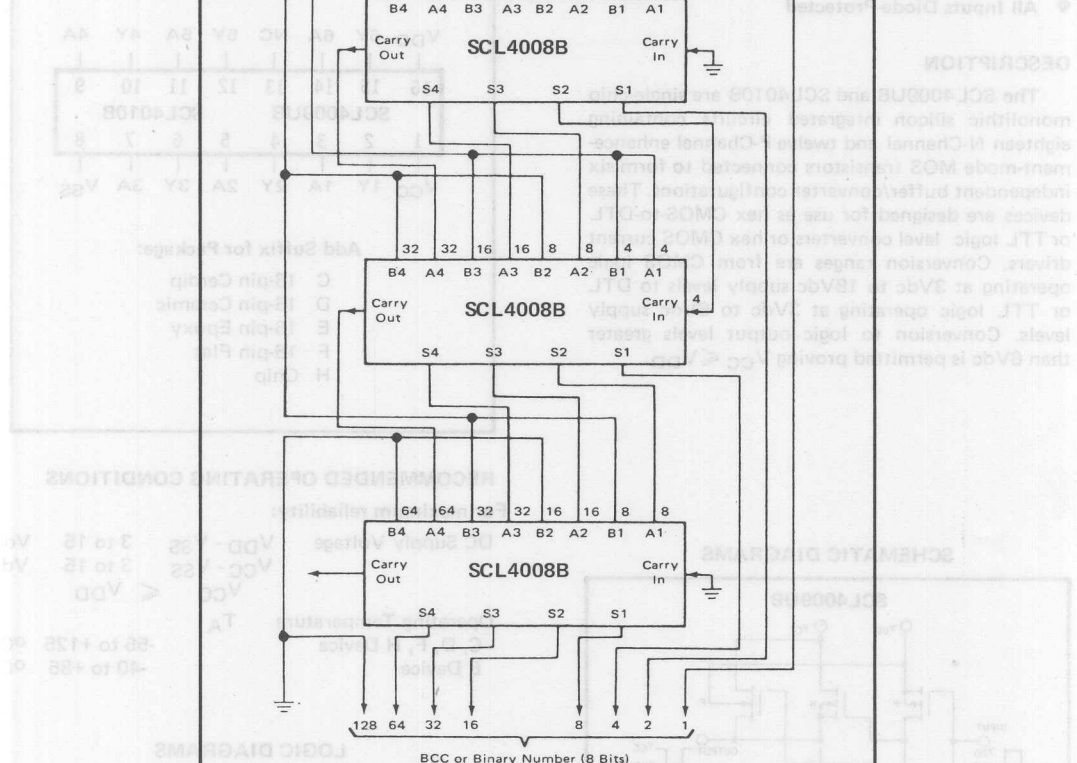
Typical N-Channel
Sink Current Characteristics

LOGIC DIAGRAM



APPLICATIONS INFORMATION





4-Bit Up/Down Counter

SCL4009UB Inverting SCL4010B Non-Inverting



CMOS HEX BUFFERS/CONVERTERS

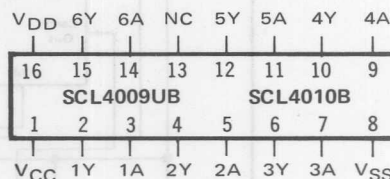
FEATURES

- ◆ Direct Drive of 2 TTL/DTL Loads
- ◆ Operation from Single or Dual Supplies
- ◆ All Inputs Diode-Protected

DESCRIPTION

The SCL4009UB and SCL4010B are single-chip monolithic silicon integrated circuits containing eighteen N-Channel and twelve P-Channel enhancement-mode MOS transistors connected to form six independent buffer/convert configurations. These devices are designed for use as hex CMOS-to-DTL or TTL logic level converters or hex CMOS current drivers. Conversion ranges are from CMOS logic operating at 3Vdc to 18Vdc supply levels to DTL or TTL logic operating at 3Vdc to 6Vdc supply levels. Conversion to logic output levels greater than 6Vdc is permitted providing $V_{CC} \leq V_{DD}$.

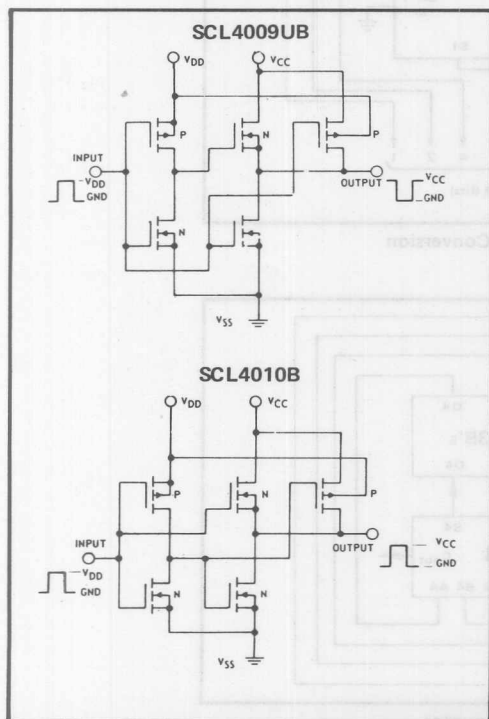
CONNECTION DIAGRAM (all packages)



Add Suffix for Package:

- C 16-pin Cerdip
- D 16-pin Ceramic
- E 16-pin Epoxy
- F 16-pin Flat
- H Chip

SCHEMATIC DIAGRAMS

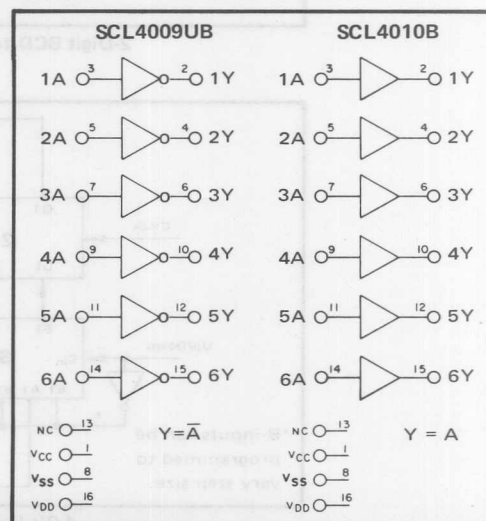


RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
	$V_{CC} - V_{SS}$	3 to 15	Vdc
	$V_{CC} \leq V_{DD}$		
Operating Temperature	T_A	-55 to +125	°C
C, D, F, H Device		-40 to +85	°C
E Device			

LOGIC DIAGRAMS



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS^{1, 3}

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units	
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.		
QUIESCENT DEVICE CURRENT	I _{DD}	5	V _{IN} = V _{SS} or V _{DD} All valid input combinations	—	1.0	—	0.005	1.0	—	30	μAdc
		10		—	2.0	—	0.01	2.0	—	60	
		15		—	4.0	—	0.02	4.0	—	120	
MINIMUM INPUT HIGH VOLTAGE SCL4009UB	V _{IH}	5	V _{OL} = 0.5V	—	4.0	—	2.75	4.0	—	4.0	Vdc
		10	V _{OL} = 1.0V	—	8.0	—	5.5	8.0	—	8.0	
		15	V _{OL} = 1.5V I _O ≤ 1μA	—	12.0	—	8.25	12.0	—	12.0	
MAXIMUM INPUT LOW VOLTAGE SCL4009UB	V _{IL}	5	V _{OH} = 3.6V	1.0	—	1.0	2.25	—	1.0	—	Vdc
		10	V _{OH} = 7.2V	2.0	—	2.0	4.5	—	2.0	—	
		15	V _{OH} = 10.8V I _O ≤ 1μA	3.0	—	3.0	6.75	—	3.0	—	
OUTPUT LOW (SINK) CURRENT C, D, F, H device	I _{OL}	5	V _{OL} = 0.4V	3.8	—	3.0	4.0	—	2.2	—	mAdc
		10	V _{OL} = 0.5V	10.0	—	8.0	10	—	5.6	—	
		15	V _{OL} = 1.5V V _{IN} = V _{SS} or V _{DD}	30	—	24	36	—	16	—	
E device		5	V _{OL} = 0.4V	3.6	—	3.0	4.0	—	2.4	—	mAdc
		10	V _{OL} = 0.5V	9.6	—	8.0	10	—	6.4	—	
		15	V _{OL} = 1.5V V _{IN} = V _{SS} or V _{DD}	28	—	24	36	—	20	—	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

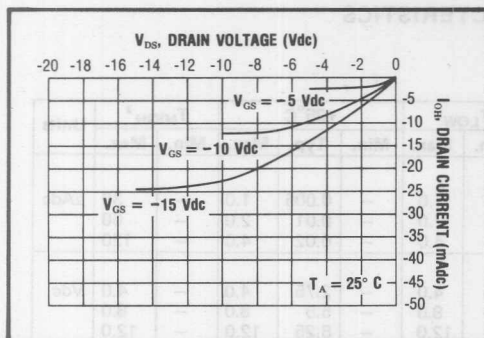
² T_{LOW} = -55°C for C, D, F, H device
= -40°C for E device.

T_{HIGH} = +125°C for C, D, F, H device
= + 85°C for E device.

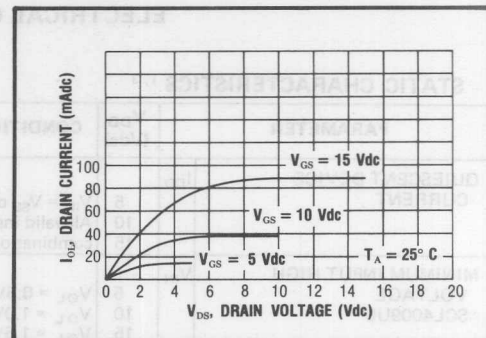
³ V_{CC} = V_{DD}

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

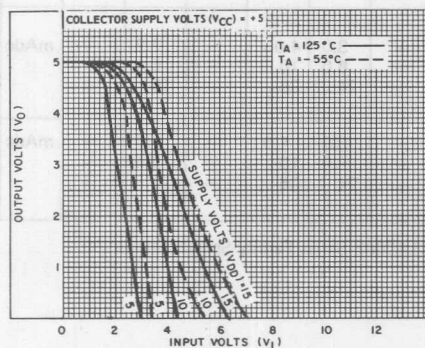
PARAMETER		V _{DD} (V _{dc})	V _{CC} (V _{dc})	Min.	Typ.	Max.	Units	
PROPAGATION DELAY TIME Driving CMOS	t _{PLH}	5	5	—	60	120	ns	
		10	10	—	35	70		
		15	15	—	28	56		
	Driving TTL/DTL	5	5	—	45	90	ns	
		10	5	—	20	40		
		15	5	—	15	30		
	Driving CMOS	t _{PHL}	5	5	—	30	60	ns
			10	10	—	18	36	
			15	15	—	12	24	
Driving TTL/DTL		5	5	—	35	70	ns	
		10	5	—	15	30		
		15	5	—	10	20		
OUTPUT TRANSITION TIME	t _{TLH}	5	5	—	150	300	ns	
		10	10	—	75	150		
		15	15	—	60	120		
	t _{THL}	5	5	—	30	60	ns	
		10	10	—	20	40		
		15	15	—	12	24		
INPUT CAPACITANCE SCL4009UB SCL4010B	C _{IN}	—	—	—	10	15	pF	
		—	—	—	5	7.5		



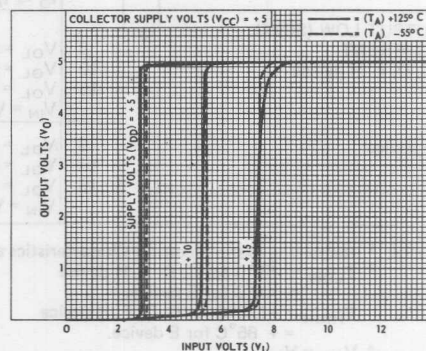
Typical P-Channel
Source Current Characteristics



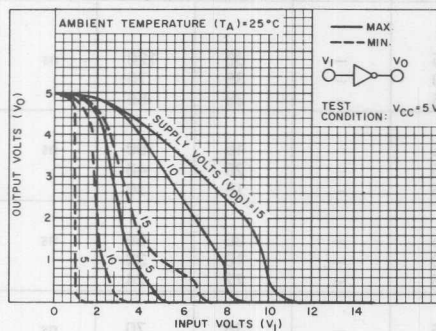
Typical N-Channel
Sink Current Characteristics



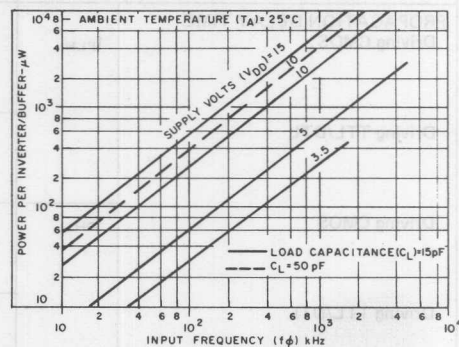
Typ. voltage transfer characteristics as function of
temperature — SCL4009UB



Typ. voltage transfer characteristics as a function
of temperature — SCL4010B



Min. & max. voltage transfer charac-
teristics — SCL4009UB



Typ. dissipation characteristics —
SCL4009UB, SCL4010B

SCL4011B, SCL4012B SCL4023B, SCL4068B



CMOS NAND GATES

SCL4011B – Quad 2-Input NAND
SCL4012B – Dual 4-Input NAND
SCL4023B – Triple 3-Input NAND
SCL4068B – 8-Input NAND

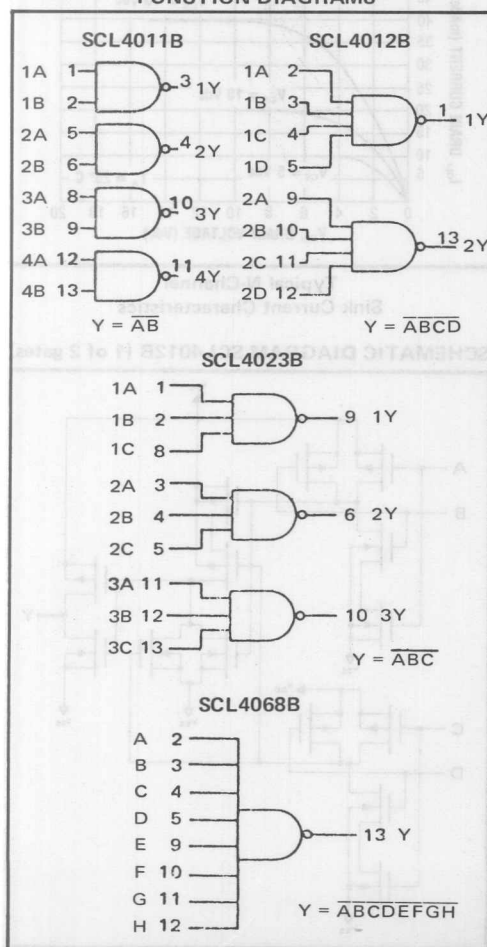
FEATURES

- ◆ Buffered Outputs
- ◆ Diode Protection on all Inputs
- ◆ Fully "B"-Series Compatible
- ◆ Balanced Output Drive Current Specifications

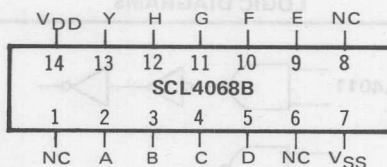
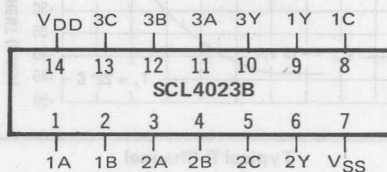
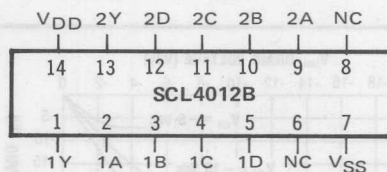
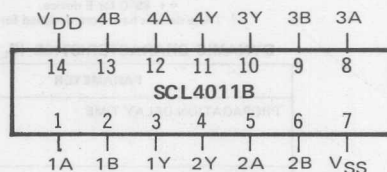
TRUTH TABLE

Inputs	Output
1 1 . . . 1	0
All other combinations	1

FUNCTION DIAGRAMS



CONNECTION DIAGRAMS (all packages)



Add suffix to package:

- C 14-pin Cerdip
- D 14-pin Ceramic
- E 14-pin Epoxy
- F 14-pin Flat
- H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A	-55 to +125	°C
C, D, F, H Device		-40 to +85	°C
E Device			

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS^{1, 3}

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	V _{IN} = V _{SS} or V _{DD} All valid input combinations	—	0.05	—	0.0005	0.05	—	1.5	μAdc
			—	0.10	—	0.001	0.10	—	3.0	
			—	0.20	—	0.002	0.20	—	6.0	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

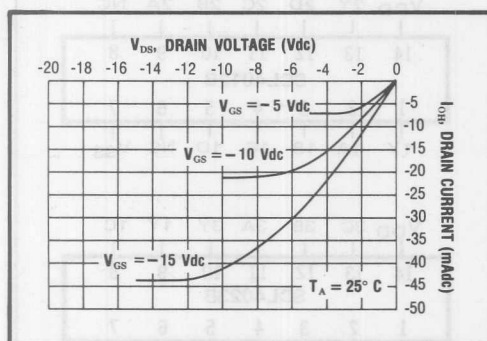
² T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.

T_{HIGH} = +125°C for C, D, F, H device.
= +85°C for E device.

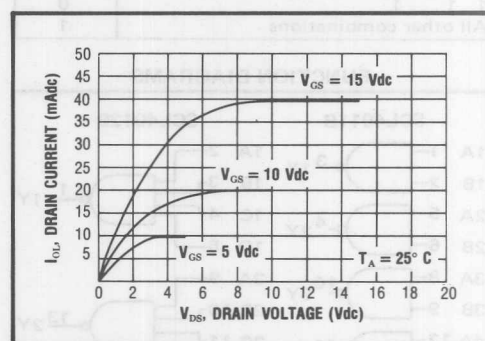
³ These devices have been designed for balanced output drive current specifications. Consult Family Specifications.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V _{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME	t _{PLH} , t _{PHL}	5	—	125	250	ns
		10	—	60	120	
		15	—	45	90	
		5	—	100	200	
OUTPUT TRANSITION TIME	t _{TLH} , t _{THL}	5	—	50	100	ns
		10	—	40	80	
		15	—	40	80	
		5	—	40	80	

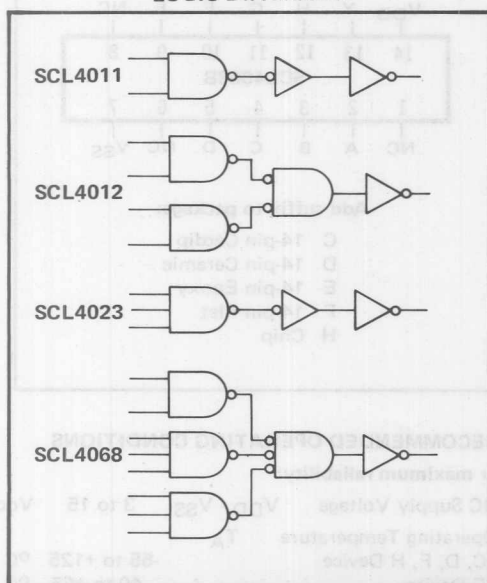


Typical P-Channel
Source Current Characteristics

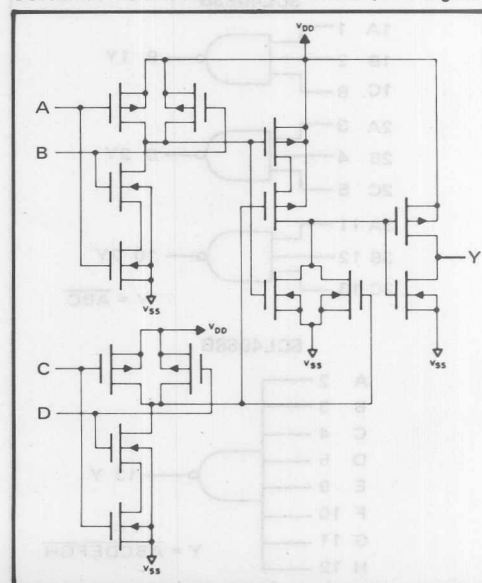


Typical N-Channel
Sink Current Characteristics

LOGIC DIAGRAMS



SCHEMATIC DIAGRAM SCL4012B (1 of 2 gates)



SCL4011UB



CMOS NAND GATE (Unbuffered)

FEATURES

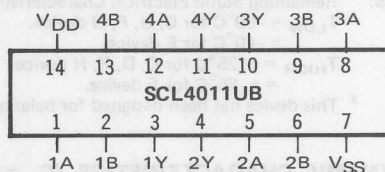
- ◆ Unbuffered Outputs for Quasi-Linear Applications
- ◆ Quad 2-Input NAND Configuration
- ◆ Diode Protection on all Inputs
- ◆ Output Drive Current Compatible with "B" Series
- ◆ Pin Compatible with Buffered SCL4011B
- ◆ Balanced Output Drive Current Specifications

DESCRIPTION

The SCL4011UB consists of four positive-logic NAND gates. The outputs are unbuffered, making the device suitable for quasi-linear applications, such as gated oscillators, multivibrators, and pulse shaping circuits.

For digital applications, the buffered SCL4011B is recommended for its higher gain and input pattern insensitivity.

CONNECTION DIAGRAM (all packages)



Add suffix for package:

- C 14-pin Cerdip
- D 14-pin Ceramic
- E 14-pin Epoxy
- F 14-pin Flat
- H Chip

TRUTH TABLE

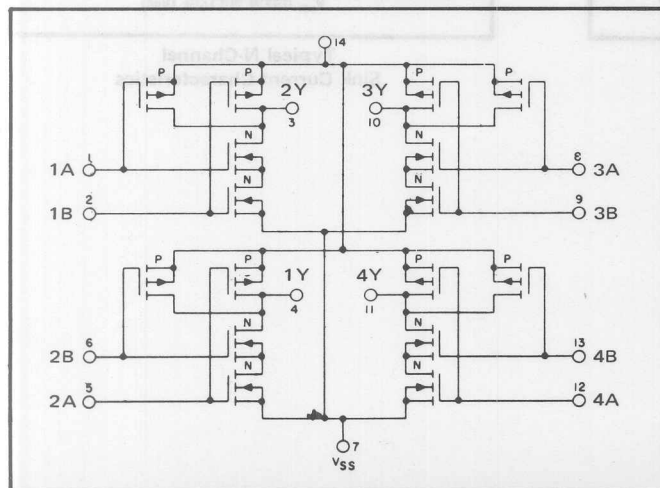
Inputs		Output
1	1	0
All other combinations		1

RECOMMENDED OPERATING CONDITIONS

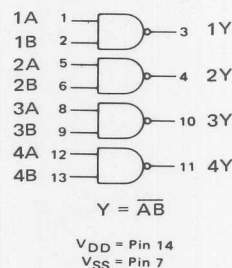
For maximum reliability:

DC Supply Voltage	V _{DD} - V _{SS}	3 to 15	V _{dc}
Operating Temperature	T _A	-55 to +125	°C
C, D, F, H Device		-40 to +85	°C
E Device			

SCHEMATIC DIAGRAM



LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS^{1, 3}

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	V _{IN} = V _{SS} or V _{DD} All valid input combinations	—	0.05	—	0.0005	0.05	—	1.5	μAdc
			—	0.10	—	0.001	0.10	—	3.0	
			—	0.20	—	0.002	0.20	—	6.0	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

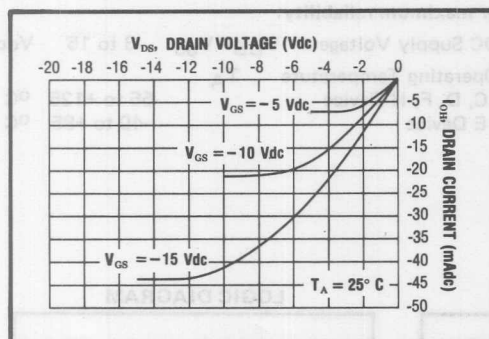
² T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.

T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

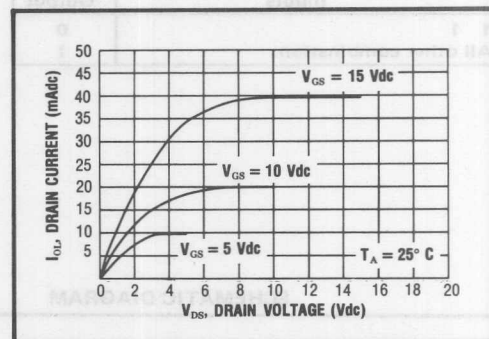
³ This device has been designed for balanced output drive current specifications. Consult Family Specifications.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER	V _{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME	t _{PLH} , t _{PHL}	5	—	75	ns
		10	—	35	
		15	—	25	
		—	—	—	
OUTPUT TRANSITION TIME	t _{TLH} , t _{THL}	5	—	100	ns
		10	—	50	
		15	—	40	
		—	—	—	

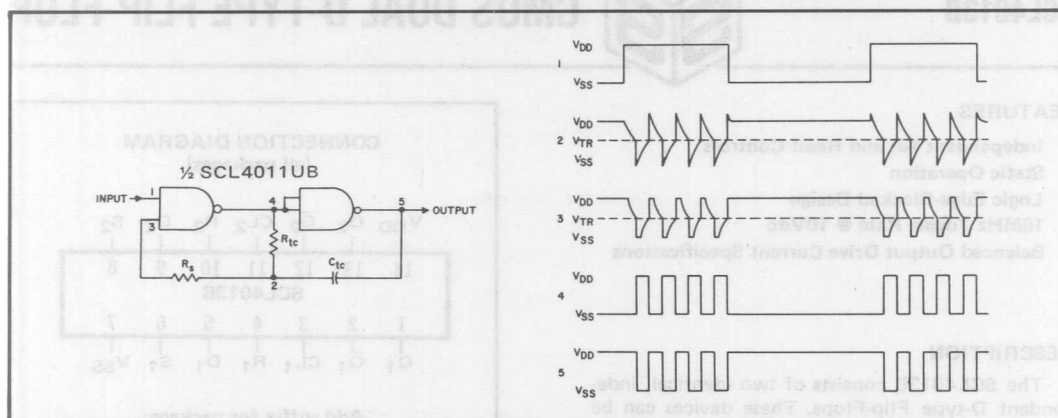


Typical P-Channel
Source Current Characteristics

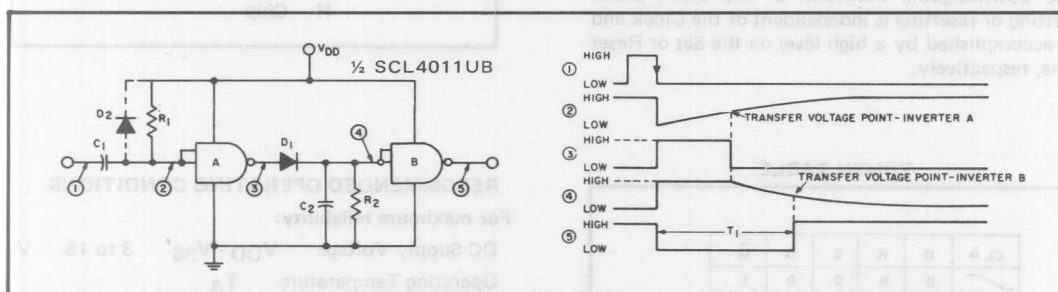
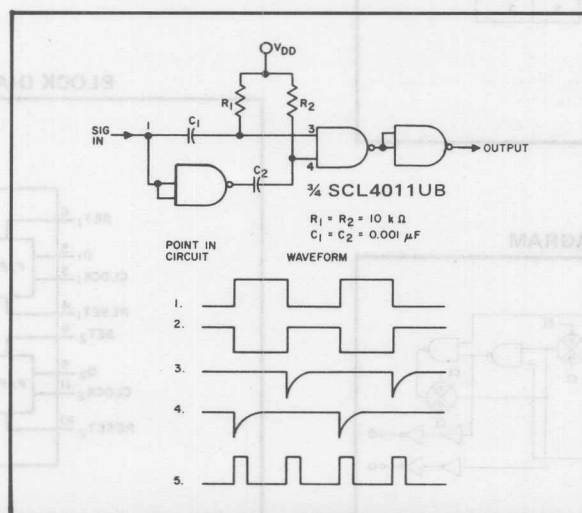


Typical N-Channel
Sink Current Characteristics

APPLICATIONS INFORMATION



Gated Oscillator

Compensated Monostable Multivibrator
(Independent of Transfer Voltage)

Frequency Doubler



FEATURES

- ◆ Independent Set and Reset Controls
- ◆ Static Operation
- ◆ Logic Edge-Clocked Design
- ◆ 16MHz Toggle Rate @ 10Vdc
- ◆ Balanced Output Drive Current Specifications

DESCRIPTION

The SCL4013B consists of two identical, independent D-type Flip-Flops. These devices can be used for shift register applications, and, by connecting the $\bar{Q}$ output to the Data input, for counter and toggle applications. The logic level present at the D input is transferred to the Q output during the positive-going transition of the Clock pulse. Setting or resetting is independent of the Clock and is accomplished by a high level on the Set or Reset line, respectively.

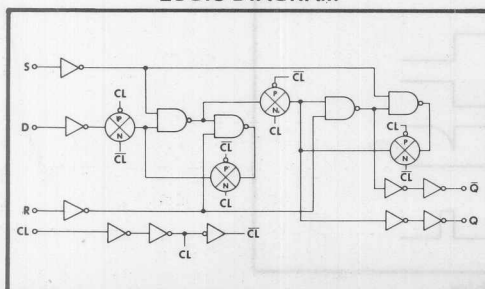
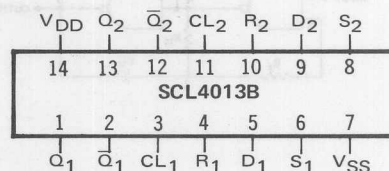
TRUTH TABLE

CL Δ	D	R	S	Q	$\bar{Q}$
	0	0	0	0	1
	1	0	0	1	0
	x	0	0	Q	$\bar{Q}$
x	x	1	0	0	1
x	x	0	1	1	0
x	x	1	1	1	1

NO CHANGE

Δ = Level Change
x = Don't Care

LOGIC DIAGRAM

CONNECTION DIAGRAM
(all packages)

Add suffix for package:

- C 14-pin Cerdip
- D 14-pin Ceramic
- E 14-pin Epoxy
- F 14-pin Flat
- H Chip

RECOMMENDED OPERATING CONDITIONS

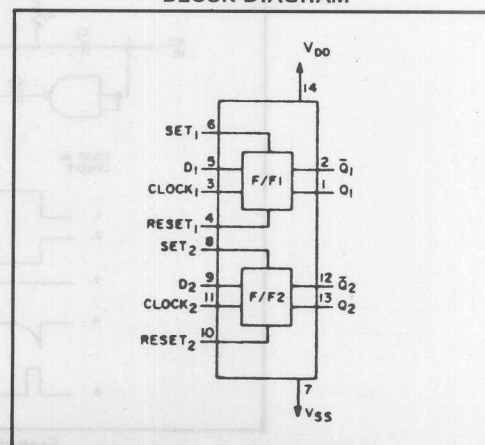
For maximum reliability:

DC Supply Voltage $V_{DD} - V_{SS}$ 3 to 15 VdcOperating Temperature T_A

C, D, F, H Device -55 to +125 °C

E Device -40 to +85 °C

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS^{1,3}

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	V _{IN} =V _{SS} or V _{DD} All valid input combinations	—	1.0	—	0.005	1.0	—	30	μAdc
			—	2.0	—	0.01	2.0	—	60	
			—	4.0	—	0.02	4.0	—	120	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

² T_{LOW} = -55°C for C, D, F, H device.

= -40°C for E device.

T_{HIGH} = +125°C for C, D, F, H device.

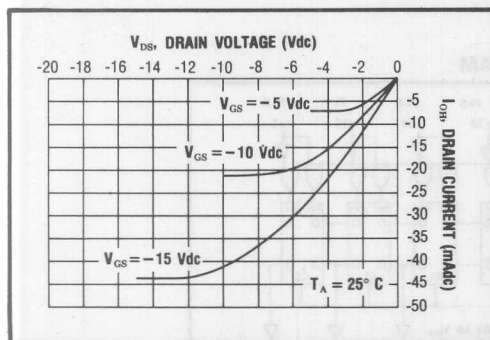
= + 85°C for E device.

³ This device has been designed for balanced output drive current specifications. Consult Family Specifications.

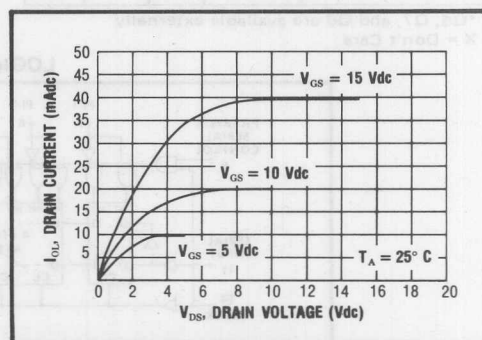
DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V _{DD} (Vdc)	Min.	Typ.	Max.	Units
CLOCKED OPERATION						
PROPAGATION DELAY TIME	t _{PLH} , t _{PHL}	5 10 15	— — —	125 65 45	250 130 90	ns
OUTPUT TRANSITION TIME	t _{TLH} , t _{THL}	5 10 15	— — —	100 50 40	200 100 80	ns
MINIMUM CLOCK PULSE WIDTH	PW _{CL}	5 10 15	— — —	70 30 20	140 60 40	ns
MAXIMUM CLOCK FREQUENCY	f _{CL}	5 10 15	3.5 8.0 12.5	7.0 16 25	— — —	MHz
MAXIMUM CLOCK RISE AND FALL TIME ¹	t _{rCL} , t _{fCL}	5 10 15	15 10 5	— — —	— — —	μs
MINIMUM SETUP TIME	t _{setup}	5 10 15	— — —	25 10 7.5	50 20 15	ns
MINIMUM HOLD TIME	t _{hold}	5 10 15	— — —	-25 -10 -5	0 0 0	ns
SET AND RESET OPERATIONS						
PROPAGATION DELAY TIME S to Q, R to $\bar{Q}$	t _{PLH}	5 10 15	— — —	125 65 45	250 130 90	ns
MINIMUM SET AND RESET PULSE WIDTH	PW _S , PW _R	5 10 15	— — —	65 30 25	130 60 50	ns
SET AND RESET REMOVAL TIME	t _{rem}	5 10 15	— — —	0 0 0	25 10 5	ns

¹When units are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the transition times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitive load.



Typical P-Channel
Source Current Characteristics



Typical N-Channel
Sink Current Characteristics

FEATURES

- ◆ Synchronous Parallel Input/Serial Output
- ◆ Synchronous Serial Input/Serial Output
- ◆ Fully Static Operation — DC to 6 MHz @ 10Vdc
- ◆ Q Outputs from Stages 6, 7, and 8 Available

DESCRIPTION

The SCL4014B is an 8-stage Parallel-Input/Serial Output Register having common Clock and Parallel/Serial Control inputs, a single Serial Data input, and individual parallel Jam inputs to each register stage. Each register stage is a D-type, master-slave flip-flop. In addition to an output from stage 8, Q outputs are also available from stages 6 and 7. Parallel as well as serial entry is made into the register synchronous with the positive Clock line transition and under control of the Parallel/Serial Control input. When the Parallel/Serial Control input is low, data is serially shifted into the 8-stage register synchronously with the transition of the Clock line. When the Parallel/Serial Control input is high, data is jammed into the 8-stage register via the Parallel Input lines and synchronous with the positive transition of the Clock line. Changes on the Parallel/Serial Control should be made only while the Clock is low. Register expansion using multiple SCL4014B packages is permitted.

TRUTH TABLE

Serial Operation

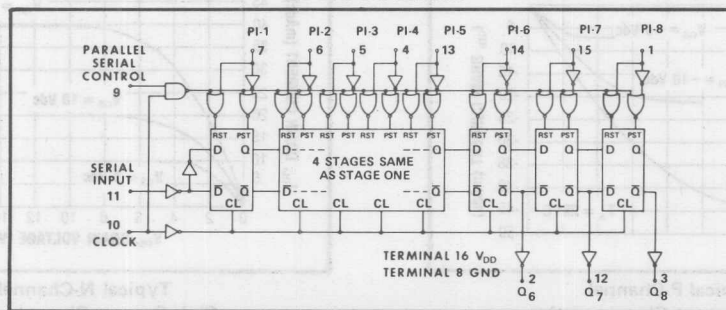
t	CLOCK	SER IN	P/S	Q6 t=n+6	Q7 t=n+7	Q8 t=n+8
n		0	0	0	?	?
n+1		1	0	1	0	?
n+2		0	0	0	1	0
n+3		1	0	1	0	1
		X	0	Q6	Q7	Q8

Parallel Operation

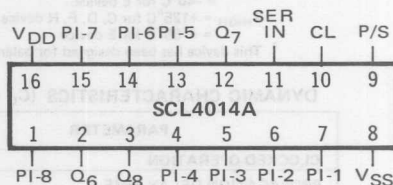
CLOCK	SER IN	P/S	PI-m	*Q _m
	X	1	0	0
	X	1	1	1

*Q6, Q7, and Q8 are available externally
X = Don't Care

LOGIC DIAGRAM



CONNECTION DIAGRAM (all packages)



Add suffix for package:

- C 16-pin Cerdip
- D 16-pin Ceramic
- E 16-pin Epoxy
- F 16-pin Flat
- H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A	-55 to +125	°C
C, D, F, H Device		-40 to +85	°C
E Device			

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS¹

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	V _{IN} =V _{SS} or V _{DD} All valid input combinations	—	5	—	0.05	5	—	150	μAdc
			—	10	—	0.1	10	—	300	
			—	20	—	0.2	20	—	600	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

² T_{LOW} = -55°C for C, D, F, H device.

= -40°C for E device.

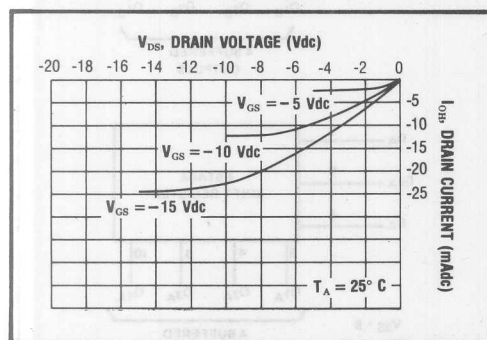
T_{HIGH} = +125°C for C, D, F, H device.

= + 85°C for E device.

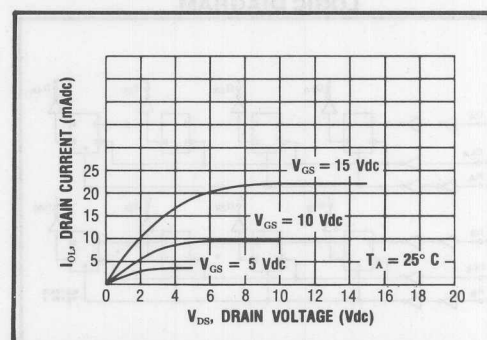
DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER	V _{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME	t _{PLH} , t _{PHL}	5	—	375	ns
		10	—	150	
		15	—	120	
OUTPUT TRANSITION TIME	t _{TLH} , t _{THL}	5	—	130	ns
		10	—	65	
		15	—	50	
MINIMUM CLOCK PULSE WIDTH	PW _{CL}	5	—	150	ns
		10	—	75	
		15	—	65	
MAXIMUM CLOCK FREQUENCY	f _{CL}	5	1.5	3.0	MHz
		10	3.0	6.0	
		15	4.0	8.0	
MAXIMUM CLOCK RISE AND FALL TIME ¹	t _{rCL} , t _{fCL}	5	15	—	μs
		10	15	—	
		15	5	—	
MINIMUM SETUP TIME Serial Input	t _{setup}	5	—	150	ns
		10	—	40	
		15	—	30	
P/S Input	t _{setup}	5	—	175	ns
		10	—	40	
		15	—	30	
Parallel Inputs	t _{setup}	5	—	190	ns
		10	—	50	
		15	—	35	
MINIMUM HOLD TIME All Inputs	t _{hold}	5	—	100	ns
		10	—	30	
		15	—	20	

¹ When units are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the transition times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitive load.



Typical P-Channel
Source Current Characteristics



Typical N-Channel
Sink Current Characteristics



CMOS DUAL 4-STAGE SHIFT REGISTER

FEATURES

- Serial Input/Parallel Output
- Direct Reset
- Two Independent Sections
- Fully Static Operation - DC to 5MHz @ 10Vdc
- Balanced Output Drive Current Specifications

DESCRIPTION

The SCL4015B consists of two identical, independent, 4-stage Serial-Input/Parallel-Output Registers. Each register has independent Clock and Reset inputs as well as a single serial Data input. Q outputs are available from each of the four stages on both registers. All register stages are D-type, master-slave flip-flops. The logic level present at the Data input is transferred into the first register stage and shifted right one stage at each positive-going Clock transition. Resetting of all stages is accomplished by a high level on the Reset line. Register expansion to 8 stages using one SCL4015B package, or to more than 8 stages using additional SCL4015B's, is possible.

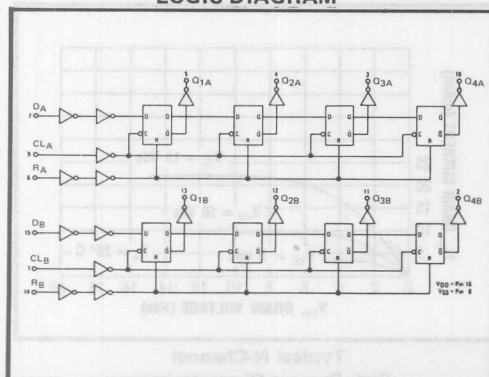
TRUTH TABLE

CL*	D	R	Q ₁	Q _n
	0	0	0	Q _{n-1}
	1	0	1	Q _{n-1}
	X	0	Q ₁	Q _n
X	X	1	0	0

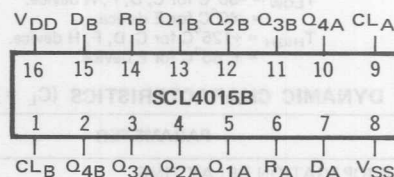
(NO CHANGE)

* = LEVEL CHANGE
X = DON'T CARE

LOGIC DIAGRAM



CONNECTION DIAGRAM (all packages)



Add suffix for package:

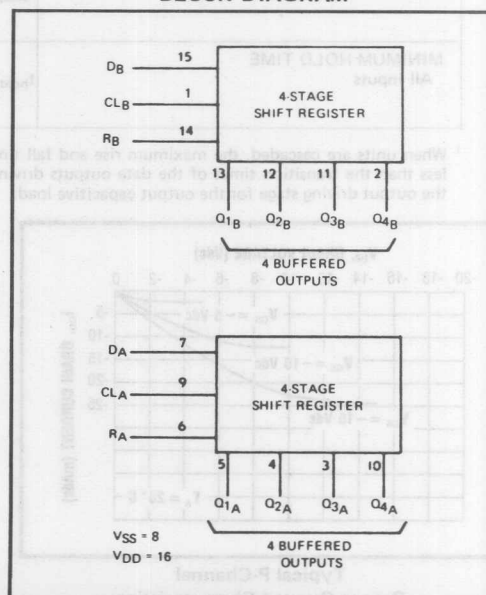
- C 16-pin Cerdip
- D 16-pin Ceramic
- E 16-pin Epoxy
- F 16-pin Flat
- H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	V _{DD} - V _{SS}	3 to 15	V _{dc}
Operating Temperature	T _A	-55 to +125	°C
C, D, F, H Device		-40 to +85	°C
E Device			

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS^{1, 3}

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	V _{IN} =V _{SS} or V _{DD} All valid input combinations	—	5	—	0.05	5	—	150	μAdc
			—	10	—	0.1	10	—	300	
			—	15	—	0.2	20	—	600	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

² T_{LOW} = -55°C for C, D, F, H device.

= -40°C for E device.

T_{HIGH} = +125°C for C, D, F, H device.

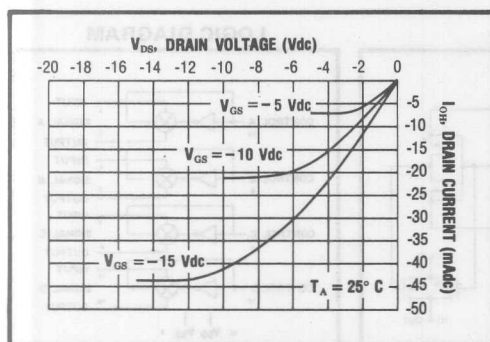
= + 85°C for E device.

³ This device has been designed for balanced output drive current specifications. Consult Family Specifications.

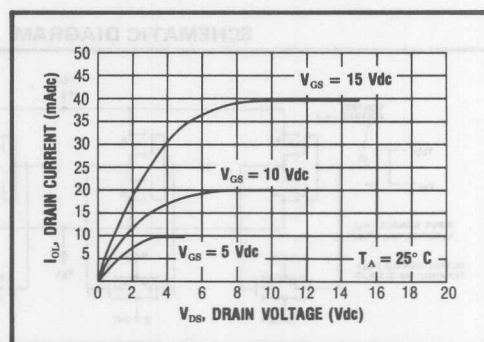
DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V _{DD} (Vdc)	Min.	Typ.	Max.	Units
CLOCKED OPERATION						
PROPAGATION DELAY TIME	t _{PLH} , t _{PHL}	5	—	375	750	ns
		10	—	125	250	
		15	—	100	200	
OUTPUT TRANSITION TIME	t _{TLH} , t _{THL}	5	—	100	200	ns
		10	—	50	100	
		15	—	40	80	
MINIMUM CLOCK PULSE WIDTH	PW _{CL}	5	—	200	400	ns
		10	—	100	200	
		15	—	80	160	
MAXIMUM CLOCK FREQUENCY	f _{CL}	5	1.25	2.5	—	MHz
		10	2.5	5.0	—	
		15	3.0	6.0	—	
MAXIMUM CLOCK RISE AND FALL TIME ¹	t _{rCL} , t _{fCL}	5	15	—	—	μs
		10	15	—	—	
		15	5	—	—	
MINIMUM DATA INPUT DATA SETUP TIME	t _{setup}	5	—	150	300	ns
		10	—	50	100	
		15	—	40	80	
MINIMUM DATA INPUT HOLD TIME	t _{hold}	5	—	0	50	ns
		10	—	0	25	
		15	—	0	15	
RESET OPERATION						
PROPAGATION DELAY TIME	t _{PHL}	5	—	375	750	ns
		10	—	125	250	
		15	—	100	200	
MINIMUM RESET PULSE WIDTH	PW _R	5	—	200	400	ns
		10	—	80	160	
		15	—	60	120	
RESET REMOVAL TIME	t _{rem}	5	—	375	750	ns
		10	—	125	250	
		15	—	100	200	

¹ When units are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the transition times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitive load.



Typical P-Channel
Source Current Characteristics



Typical N-Channel
Sink Current Characteristics

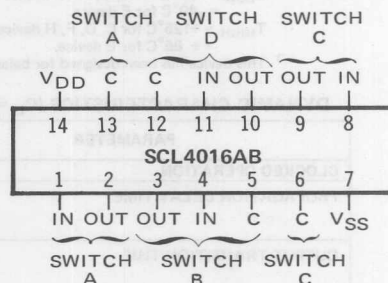


FEATURES

- ◆ Wide Range of Digital and Analog Signal Levels - Digital or Analog Signals to 18 Volts peak
- ◆ Low ON Resistance - 200 Ω typ. over 15Vp-p Signal Input Range, @ 15Vdc
- ◆ Matched Switch Characteristics - 10 Ω typ. Difference between R_{ON} Values at a Fixed Bias Point over 15Vp-p Signal Input Range @ 15Vdc
- ◆ High On/Off Output Voltage Ratio - 65 dB typ. @ $f_{is} = 10\text{kHz}$, $R_L = 10\text{k}\Omega$
- ◆ High degree of Linearity - $\leq 0.4\%$ Distortion typ. @ $f_{is} = 1\text{kHz}$, $V_{is} = 5\text{V}_{p-p}$, $V_{DD}-V_{SS} \geq 10\text{V}$, $R_L = 10\text{k}\Omega$
- ◆ Extremely Low OFF Switch Leakage Resulting in Very Low Offset Current and High Effective OFF resistance - 10pA typ. @ $V_{DD}-V_{SS} = 10\text{V}$, $T_A = 25^\circ\text{C}$
- ◆ Extremely High Control Input Impedance (Control Circuit Isolated from Signal Circuit) - $10^{12}\Omega$ typ.
- ◆ Low Crosstalk between Switches - -50dB typ. @ $f_{is} = 0.9\text{MHz}$, $R_L = 1\text{k}\Omega$
- ◆ Matched Control-Input to Signal-Output Capacitances - Reduces Output Signal Transients
- ◆ Transmits Frequencies up to 40MHz

DESCRIPTION

The SCL4016AB is a single-chip monolithic silicon integrated circuit containing eight N-channel and eight P-channel enhancement-mode MOS transistors connected to form four independent bilateral signal switches. Each switch consists of both P- and N-channel devices with common source and drain connections. A single control signal is required per switch. Both P and N devices in a given switch are biased ON or OFF by the control signal. The CMOS switch permits peak input-signal voltage swings equal to the full supply voltage, a considerable advantage over single-channel types.

CONNECTION DIAGRAM
(all packages)

Add suffix for package:

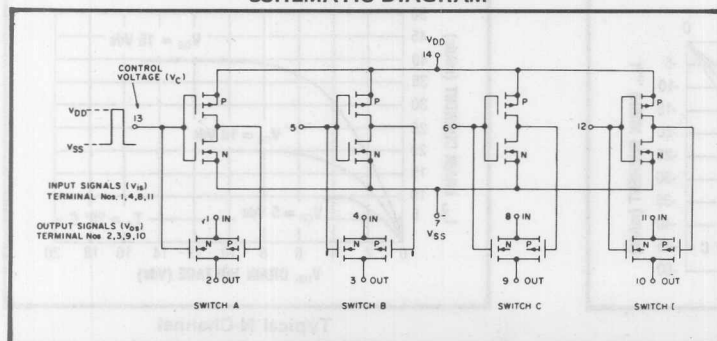
C	14-pin Cerdip
D	14-pin Ceramic
E	14-pin Epoxy
F	14-pin Flat
H	Chip

RECOMMENDED OPERATING CONDITIONS

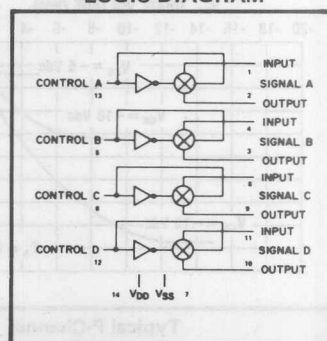
For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A	-55 to +125	$^\circ\text{C}$
C, D, F, H Device		-40 to +85	$^\circ\text{C}$
E Device			

SCHEMATIC DIAGRAM



LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS^{1,3}

PARAMETER	CONDITIONS	V _{SS} (Vdc)	V _{DD} (Vdc)	T _{LOW} ²		25°C			T _{HIGH} ²		Units		
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.			
QUIESCENT DEVICE CURRENT	I _{DD} V _{IN} = V _{SS} or V _{DD} All valid input combinations	0 0 0	5 10 15	— — —	0.05 0.1 0.2	— — —	0.0005 0.001 0.002	0.05 0.1 0.2	— — —	1.5 3.0 6.0	μAdc		
MINIMUM INPUT HIGH VOLTAGE (Control Input)	V _{IH} V _{IS} = V _{SS} V _{OS} = V _{DD} I _{OS} = 10μA	0 0 0	5 10 15	— — —	2.9 2.9 2.9	— — —	1.5 1.5 1.5	2.9 2.7 2.7	— — —	2.4 2.4 2.4	Vdc		
MAXIMUM INPUT LOW VOLTAGE (Control Input)	V _{IL} V _{IS} = V _{SS} V _{OS} = V _{DD} I _{OS} = 10μA	0 0 0	5 10 15	0.9 0.9 0.9	— — —	0.7 0.7 0.7	1.5 1.5 1.5	— — —	0.4 0.4 0.4	— — —	Vdc		
SWITCH INPUT/OUTPUT LEAKAGE (Switch off)	I _{OFF} V _C = V _{SS} V _{IS}	±7.5 ±5	+7.5 +5	— —	±250 ±125	— —	±0.1 ±0.01	±250 ±125	— —	±2500 ±1250	nAdc		
ON-RESISTANCE C, D, F, H device	R _{ON} V _C = V _{DD} R _L = 10kΩ	V _{IS} (Vdc)											
		+7.5 -7.5 ±0.25		-7.5	+7.5	— — —	360 360 775	— — —	200 200 280	400 400 850	— — —	600 600 1230	Ω
		+5 -5 ±0.25		-5	+5	— — —	600 600 1870	— — —	250 250 580	660 660 2000	— — —	960 960 2600	Ω
		+15 +0.25 +9.3		0	+15	— — —	360 360 775	— — —	200 200 300	400 400 850	— — —	600 600 1230	Ω
		+10 +0.25 +5.6		0	+10	— — —	600 600 1870	— — —	250 250 560	660 660 2000	— — —	960 960 2600	Ω
		+7.5 -7.5 ±0.25		-7.5	+7.5	— — —	370 370 790	— — —	200 200 280	400 400 850	— — —	520 520 1080	Ω
E device	R _{ON} V _C = V _{DD} R _L = 10kΩ	V _{IS} (Vdc)											
		+7.5 -7.5 ±0.25		-7.5	+7.5	— — —	370 370 790	— — —	200 200 280	400 400 850	— — —	520 520 1080	Ω
		+5 -5 ±0.25		-5	+5	— — —	610 610 1900	— — —	250 250 580	660 660 2000	— — —	840 840 2380	Ω
		+15 +0.25 +9.3		0	+15	— — —	370 370 790	— — —	200 200 300	400 400 850	— — —	520 520 1080	Ω
		+10 +0.25 +5.6		0	+10	— — —	610 610 1900	— — —	250 250 560	660 660 2000	— — —	840 840 2380	Ω
		+7.5 -7.5 ±5		-7.5 -5	+7.5 +5	— —	— —	— —	10 15	— —	— —	— —	Ω

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".² T_{LOW} = -55°C for C, D, F, H device.

= -40°C for E device.

T_{HIGH} = +125°C for C, D, F, H device.

= + 85°C for E device.

³ This device has been designed for balanced output drive current specifications. Consult Family Specifications.DYNAMIC CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

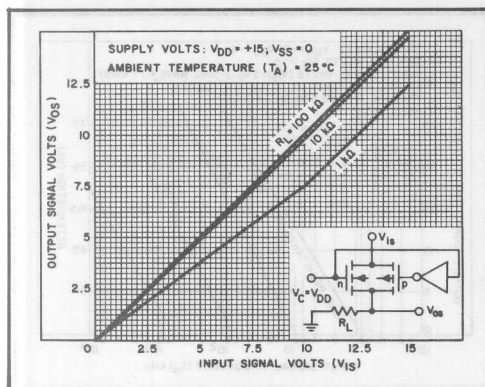
PARAMETER	CONDITIONS		V _{SS} (Vdc)	V _{DD} (Vdc)	Min.	Typ.	Max.	UNIT	
SIGNAL INPUTS (V _{IS}) AND OUTPUTS (V _{OS})									
PROPAGATION DELAY TIME Signal input to signal output	t _{PLH} , t _{PHL}	V _C = V _{DD} V _{IS} = square wave R _L = 10kΩ	0 0 0	5 10 15	— — —	20 10 7.5	40 20 15	ns	
BANDWIDTH (-3dB) (Sine Wave)	BW	V _C = V _{DD} V _{IS} = 5V _{pp} centered @0.0Vdc	R _L 1kΩ 10kΩ 100kΩ 1MΩ		-5	+5	— 54 40 38 37	— — — — —	MHz

SIGNAL INPUTS (V _{IS}) AND OUTPUTS (V _{OS}) (Continued)													
INSERTION LOSS (= 20 log ₁₀ $\frac{V_{OS}}{V_{IS}}$)		V _C = V _{DD} V _{IS} = 5V _{pp} centered @0.0Vdc	R _L	-5	+5	-	2.3	-	dB				
			1kΩ				0.2						
			10kΩ				0.1						
			100kΩ				0.05						
			1MΩ										
SIGNAL DISTORTION (Sine Wave)		V _C = V _{DD} V _{IS} = 5V _{pp} centered @0.0Vdc f _{IS} = 1.0kHz R _L = 10kΩ		-5	+5	-	0.4	-	%				
FEEDTHROUGH (-50dB)		V _C = V _{SS} V _{IS} = 5V _{pp} centered @0.0Vdc	R _L	-5	+5	-	1250	-	kHz				
			1kΩ				140						
			10kΩ				18						
			100kΩ				2						
			1MΩ										
CROSSTALK (-50dB) (Between two switches)		V _C (A) = V _{DD} V _C (B) = V _{SS} V _{IS} (A) = 5V _{pp} centered @0.0Vdc R _L = 1.0k		-5	+5	-	0.9	-	MHz				
CAPACITANCE Input	C _{IS}	V _C = V _{SS}		-5	+5	-	4	-	pF				
Output	C _{OS}	V _C = V _{SS}		-5	+5	-	4	-	pF				
Feedthrough	C _{IOS}	V _C = V _{SS}		-5	+5	-	0.2	-	pF				
CONTROL INPUT (V _C)													
PROPAGATION DELAY TIME Turn on	t _{PLH} , t _{PHL}	V _{SS} ≤ V _{IS} ≤ V _{DD} R _L = 10kΩ		0	5	-	40	80	ns				
										0	10	20	40
										0	15	15	30
MAXIMUM INPUT FREQUENCY	f _C	V _{SS} ≤ V _{IS} ≤ V _{DD} R _L = 1.0kΩ		0	5	-	5	10	MHz				
										0	10	10	
										0	15	12	
CROSSTALK (To signal port)		V _C = Square wave R _L = 10kΩ R _{IN} = 1.0kΩ		0	5	-	30	50	mV				
										0	10	100	
										0	15		

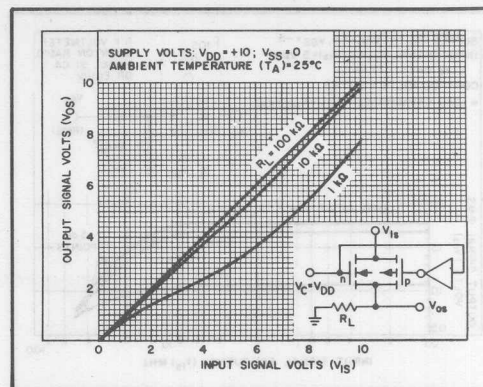
TYPICAL ON-RESISTANCE CHARACTERISTICS

CHARACTERISTIC*	SUPPLY CONDITIONS		LOAD CONDITIONS					
	V_{DD} (V)	V_{SS} (V)	$R_L = 1k\Omega$		$R_L = 10k\Omega$		$R_L = 100k\Omega$	
			VALUE (Ω)	V_{IS} (V)	VALUE (Ω)	V_{IS} (V)	VALUE (Ω)	V_{IS} (V)
R_{ON}	+15	0	200	+15	200	+15	180	+15
$R_{ON(max.)}$	+15	0	300	+11	300	+9.3	320	+9.2
R_{ON}	+10	0	290	+10	250	+10	240	+10
$R_{ON(max.)}$	+10	0	290	0	250	0	300	0
R_{ON}	+5	0	500	+7.4	560	+5.6	610	+5.5
$R_{ON(max.)}$	+5	0	860	+5	470	+5	450	+5
R_{ON}	+5	0	600	0	580	0	800	0
$R_{ON(max.)}$	+5	0	1.7k	+4.2	7k	+2.9	33k	+2.7
R_{ON}	+7.5	-7.5	200	+7.5	200	+7.5	180	+7.5
$R_{ON(max.)}$	+7.5	-7.5	290	-7.5	200	-7.5	180	-7.5
R_{ON}	+5	-5	260	+5	250	+5	240	+5
$R_{ON(max.)}$	+5	-5	310	-5	250	-5	240	-5
R_{ON}	+2.5	-2.5	590	+2.5	450	+2.5	490	+2.5
$R_{ON(max.)}$	+2.5	-2.5	720	-2.5	520	-2.5	520	-2.5
R_{ON}	+2.5	-2.5	232k	+0.25	300k	+0.25	870k	+0.25

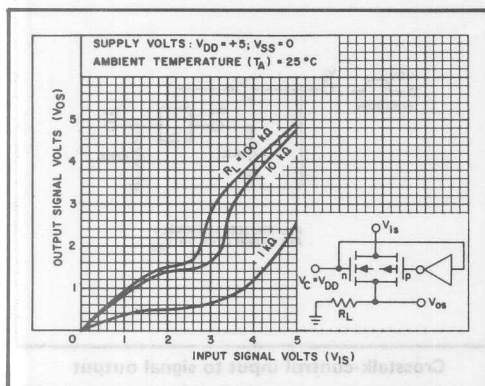
* Variation from a perfect switch: $R_{ON} = 0\Omega$.



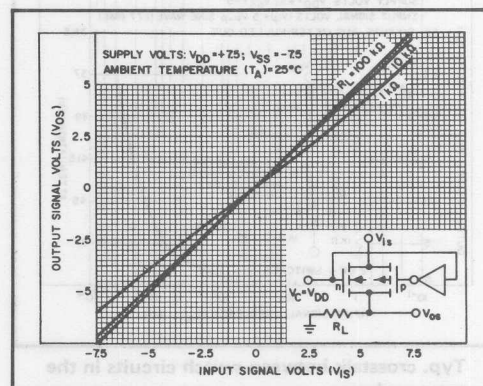
Typ. ON characteristics for 1 of 4 switches
 with $V_{DD} = +15\text{V}$, $V_{SS} = 0\text{V}$



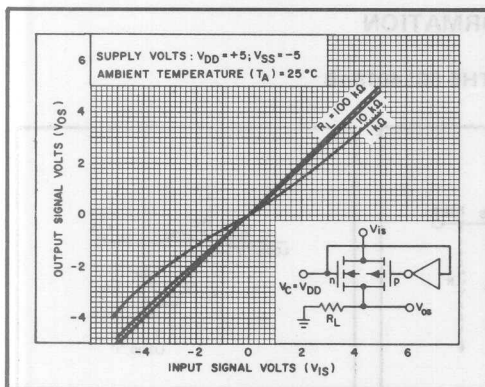
Typ. ON characteristics for 1 of 4 switches
 with $V_{DD} = +10\text{V}$, $V_{SS} = 0\text{V}$



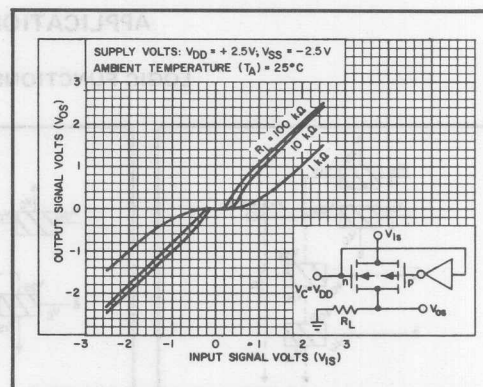
Typ. ON characteristics for 1 of 4 switches
 with $V_{DD} = +5\text{V}$, $V_{SS} = 0\text{V}$



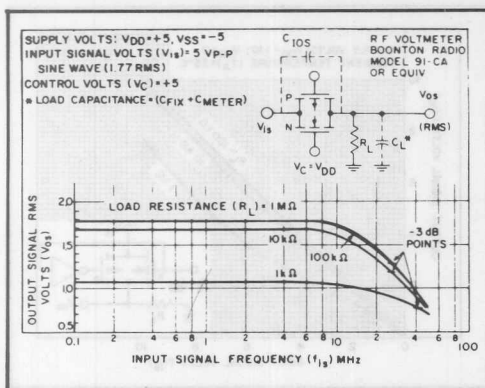
Typ. ON characteristics for 1 of 4 switches
 with $V_{DD} = +7.5\text{V}$, $V_{SS} = -7.5\text{V}$



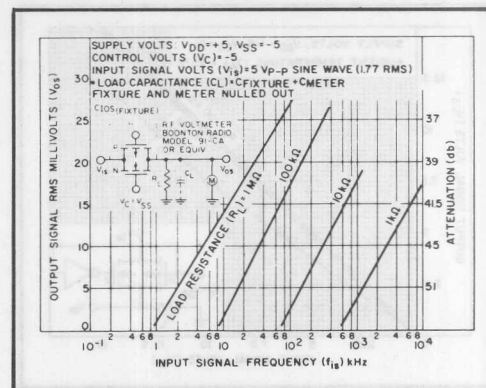
Typ. ON characteristics for 1 of 4 switches
 with $V_{DD} = +5\text{V}$, $V_{SS} = -5\text{V}$



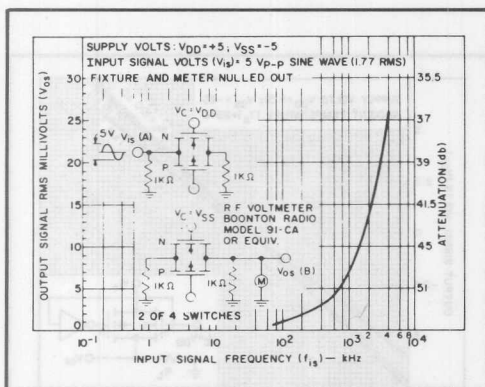
Typ. ON characteristics for 1 of 4 switches
 with $V_{DD} = +2.5\text{V}$, $V_{SS} = -2.5\text{V}$



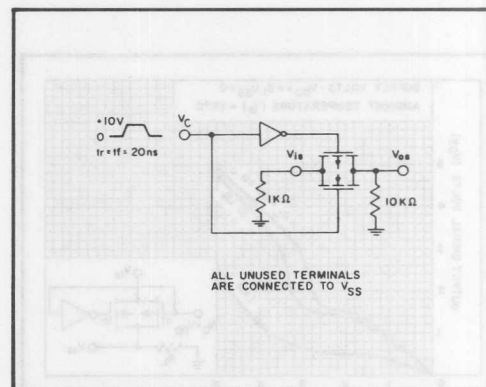
Typ. switch frequency response - switch ON



Typ. feedthru vs. freq. - switch OFF



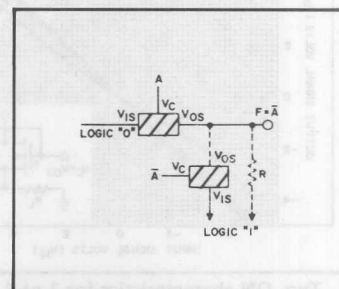
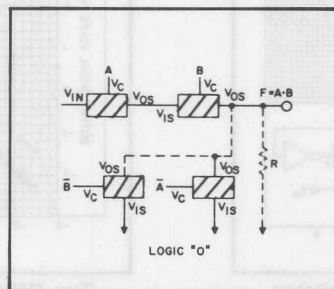
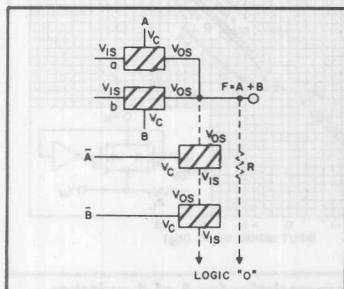
Typ. crosstalk between switch circuits in the same package



Crosstalk-control input to signal output

APPLICATIONS INFORMATION

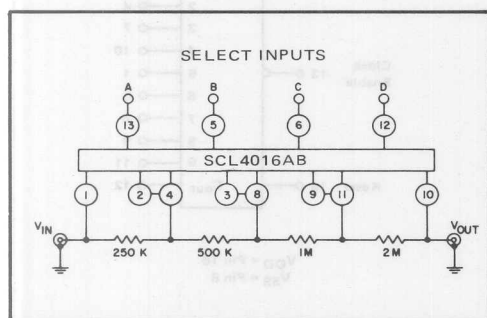
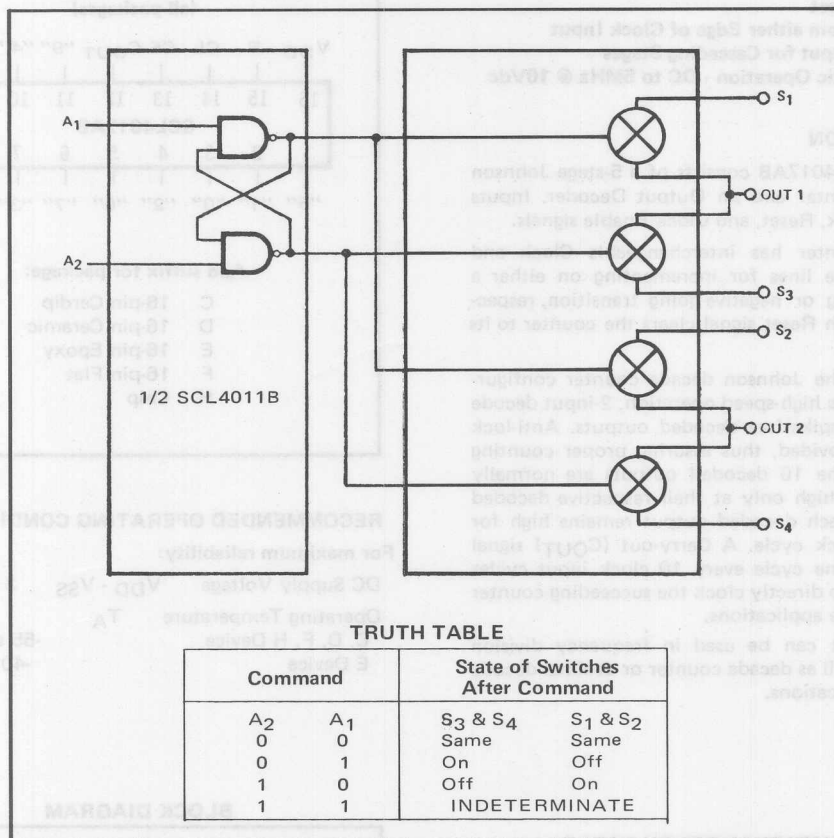
LOGIC FUNCTIONS USING THE SCL4016AB



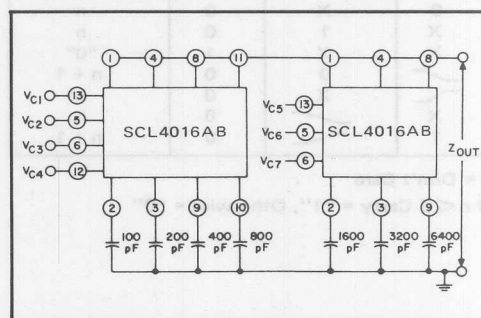
APPLICATIONS INFORMATION (Continued)

LATCHING DPDT SWITCH

The latch feature insures positive switching action in response to non-repetitive or erratic commands. A HIGH input to A₁ turns S₃ and S₄ ON, a HIGH to A₂ turns S₁ and S₂ ON. Desirable for use with limit detectors, peak detectors, or mechanical contact closures.



Digitally controlled resistor network

Digitally-controlled capacitor network.
(V_{C1} → V_{C7} are Select Inputs)

SCL4017AB



CMOS DECADE COUNTER/DIVIDER

FEATURES

- ◆ 10 Decoded Decimal Outputs
- ◆ Direct Reset
- ◆ Trigger from either Edge of Clock Input
- ◆ Carry Output for Cascading Stages
- ◆ Fully Static Operation - DC to 5MHz @ 10Vdc

DESCRIPTION

The SCL4017AB consists of a 5-stage Johnson Decade Counter and an Output Decoder. Inputs include Clock, Reset, and Clock Enable signals.

The counter has interchangeable Clock and Clock Enable lines for incrementing on either a positive-going or negative-going transition, respectively. A high Reset signal clears the counter to its zero count.

Use of the Johnson decade counter configuration permits high-speed operation, 2-input decode gating, and spike-free decoded outputs. Anti-lock gating is provided, thus assuring proper counting sequence. The 10 decoded outputs are normally low and go high only at their respective decoded time slot. Each decoded output remains high for one full clock cycle. A Carry-out (COUT) signal completes one cycle every 10 clock input cycles and is used to directly clock the succeeding counter in multi-stage applications.

This part can be used in frequency division circuits as well as decade counter or decimal decode display applications.

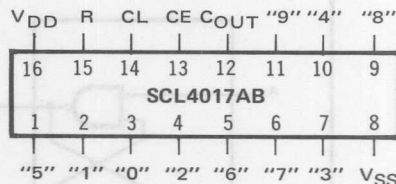
FUNCTIONAL TRUTH TABLE
(Positive Logic)

Clock	Clock Enable	Reset	Decode Output = n
0	X	0	n
X	1	0	n
X	X	1	"0"
—	0	0	n + 1
—	X	0	n
X	—	0	n
1	—	0	n + 1

x = Don't Care

If n < 5 Carry = "1", Otherwise = "0"

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

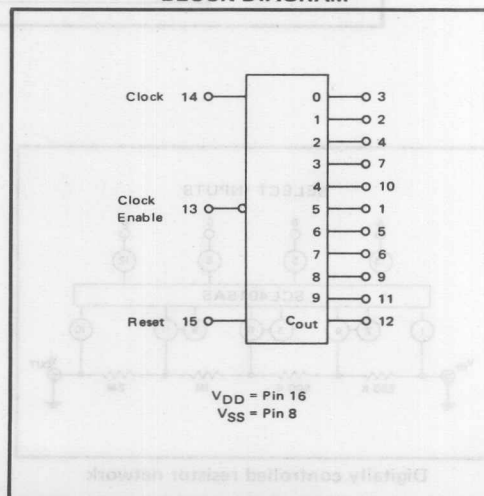
- C 16-pin Cerdip
- D 16-pin Ceramic
- E 16-pin Epoxy
- F 16-pin Flat
- H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A	-55 to +125	°C
C, D, F, H Device		-40 to +85	°C
E Device			

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS¹

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	5 V _{IN} =V _{SS} or V _{DD}	—	5	—	0.05	5	—	150	μAdc
		10 All valid input combinations	—	10	—	0.1	10	—	300	
		15	—	20	—	0.2	20	—	600	
OUTPUT HIGH (SOURCE) CURRENT C, D, F, H device Decoded Outputs	I _{OH}	5 V _{OH} = 4.6V	-0.05	—	-0.04	-0.3	—	-0.028	—	mAdc
		10 V _{OH} = 9.5V	-0.125	—	-0.1	-0.75	—	-0.07	—	
		15 V _{OH} = 13.5V V _{IN} =V _{SS} or V _{DD}	-0.375	—	-0.3	-2.5	—	-0.21	—	
	Carry Output	5 V _{OH} = 4.6V	-0.25	—	-0.2	-0.75	—	-0.14	—	mAdc
		10 V _{OH} = 9.5V	-0.62	—	-0.5	-1.1	—	-0.35	—	
		15 V _{OH} = 13.5V V _{IN} =V _{SS} or V _{DD}	-1.9	—	-1.5	-3.5	—	-1.1	—	
E device Decoded Outputs	I _{OH}	5 V _{OH} = 4.6V	-0.048	—	-0.04	-0.3	—	-0.032	—	mAdc
		10 V _{OH} = 9.5V	-0.12	—	-0.1	-0.75	—	-0.08	—	
		15 V _{OH} = 13.5V V _{IN} =V _{SS} or V _{DD}	-0.36	—	-0.3	-2.5	—	-0.24	—	
	Carry Output	5 V _{OH} = 4.6V	-0.24	—	-0.2	-0.75	—	-0.16	—	mAdc
		10 V _{OH} = 9.5V	-0.6	—	-0.5	-1.1	—	-0.4	—	
		15 V _{OH} = 13.5V V _{IN} =V _{SS} or V _{DD}	-1.8	—	-1.5	-3.5	—	-1.2	—	
OUTPUT LOW (SINK) CURRENT C, D, F, H device Decoded Outputs	I _{OL}	5 V _{OL} = 0.4V	0.05	—	0.04	0.4	—	0.028	—	mAdc
		10 V _{OL} = 0.5V	0.125	—	0.1	1.0	—	0.07	—	
		15 V _{OL} = 1.5V V _{IN} =V _{SS} or V _{DD}	0.375	—	0.3	3.0	—	0.21	—	
	Carry Output	5 V _{OL} = 0.4V	0.25	—	0.2	0.75	—	0.14	—	mAdc
		10 V _{OL} = 0.5V	0.62	—	0.5	1.3	—	0.35	—	
		15 V _{OL} = 1.5V V _{IN} =V _{SS} or V _{DD}	1.9	—	1.5	4.0	—	1.1	—	
E device Decoded Outputs	I _{OL}	5 V _{OL} = 0.4V	0.048	—	0.04	0.4	—	0.032	—	mAdc
		10 V _{OL} = 0.5V	0.12	—	0.1	1.0	—	0.08	—	
		15 V _{OL} = 1.5V V _{IN} =V _{SS} or V _{DD}	0.36	—	0.3	3.0	—	0.24	—	
	Carry Output	5 V _{OL} = 0.4V	0.24	—	0.2	0.75	—	0.16	—	mAdc
		10 V _{OL} = 0.5V	0.6	—	0.5	1.3	—	0.4	—	
		15 V _{OL} = 1.5V V _{IN} =V _{SS} or V _{DD}	1.8	—	1.5	4.0	—	1.2	—	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

² T_{LOW} = -55°C for C, D, F, H device.

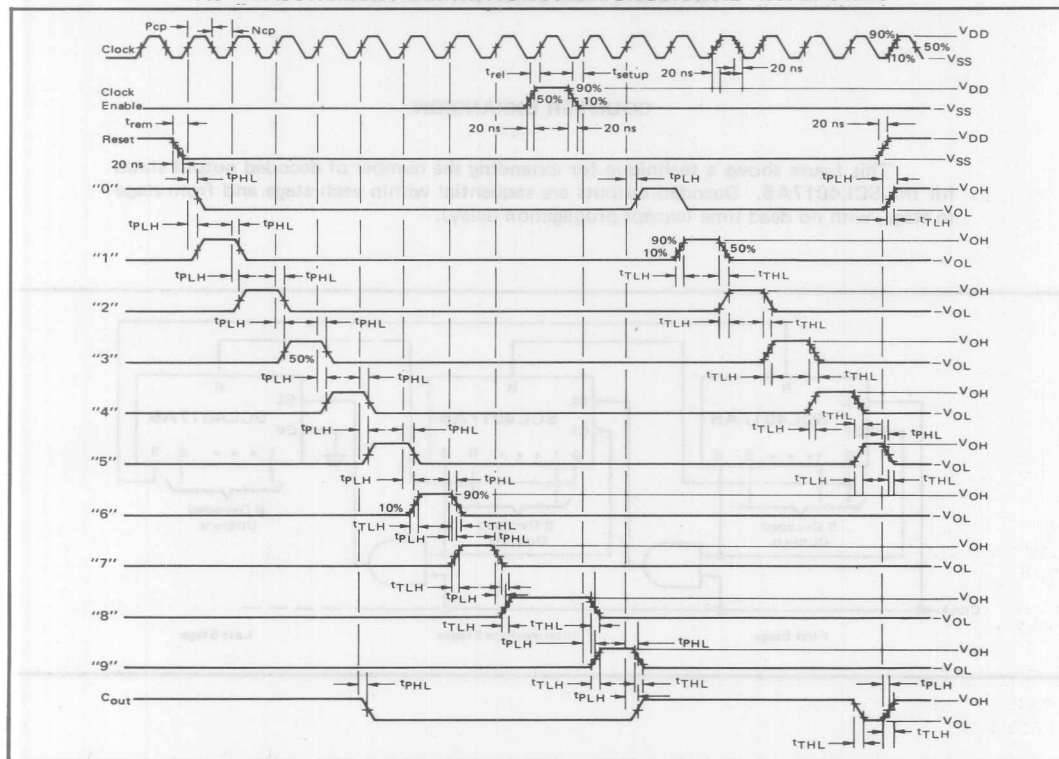
= -40°C for E device.

T_{HIGH} = +125°C for C, D, F, H device.

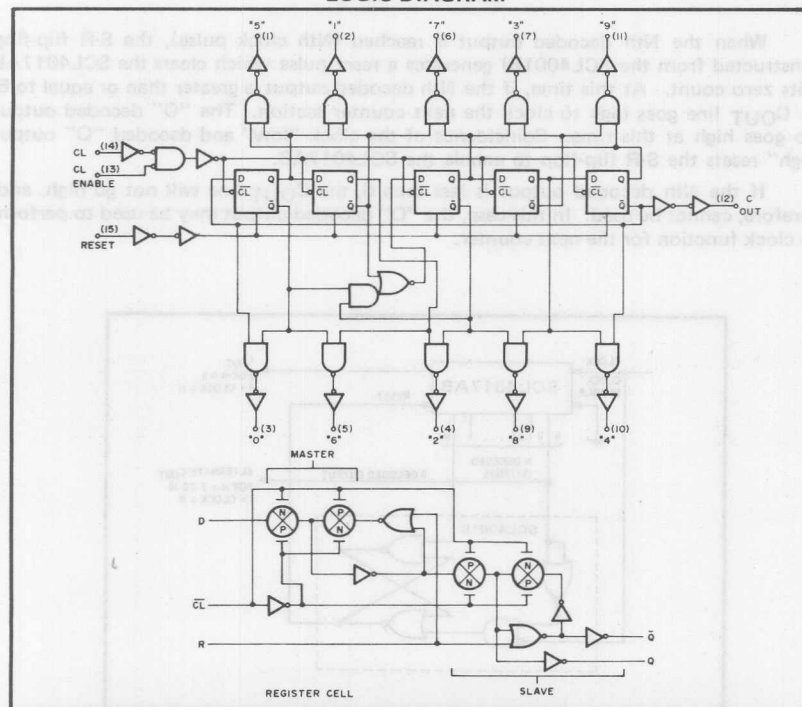
= + 85°C for E device.

PARAMETER		V _{DD} (V _{dc})	Min.	Typ.	Max.	Units
CLOCKED OPERATION						
PROPAGATION DELAY TIME To Decoded Outputs	t _{PLH} , t _{PHL}	5	—	600	1200	ns
		10	—	240	480	
		15	—	180	360	
To Carry Output	t _{PLH} , t _{PHL}	5	—	500	1000	ns
		10	—	200	400	
		15	—	150	300	
OUTPUT TRANSITION TIME Decoded Outputs	t _{TLH} , t _{THL}	5	—	250	500	ns
		10	—	125	250	
		15	—	90	180	
Carry Output	t _{TLH} , t _{THL}	5	—	180	360	ns
		10	—	90	180	
		15	—	65	130	
MINIMUM CLOCK PULSE WIDTH	PW _{CL}	5	—	200	400	ns
		10	—	100	200	
		15	—	80	160	
MAXIMUM CLOCK FREQUENCY	f _{CL}	5	1.25	2.5	—	MHz
		10	2.5	5.0	—	
		15	3.0	6.0	—	
MAXIMUM CLOCK OR ENABLE RISE AND FALL TIME	t _{rCL} , t _{fCL}	5	15	—	—	μs
		10	15	—	—	
		15	5	—	—	
MINIMUM ENABLE SETUP TIME	t _{setup}	5	—	175	350	ns
		10	—	75	150	
		15	—	55	110	
MINIMUM ENABLE REMOVAL TIME	t _{rem}	5	—	250	500	ns
		10	—	100	200	
		15	—	75	150	
RESET OPERATION						
PROPAGATION DELAY TIME To Decoded Outputs	t _{PLH} , t _{PHL}	5	—	500	1000	ns
		10	—	200	400	
		15	—	140	280	
To Carry Output	t _{PLH}	5	—	400	800	ns
		10	—	150	300	
		15	—	110	220	
MINIMUM RESET PULSE WIDTH	PW _R	5	—	150	300	ns
		10	—	75	150	
		15	—	60	120	
RESET REMOVAL TIME	t _{rem}	5	—	250	500	ns
		10	—	100	200	
		15	—	80	160	

AC MEASUREMENT DEFINITION AND FUNCTIONAL WAVEFORMS



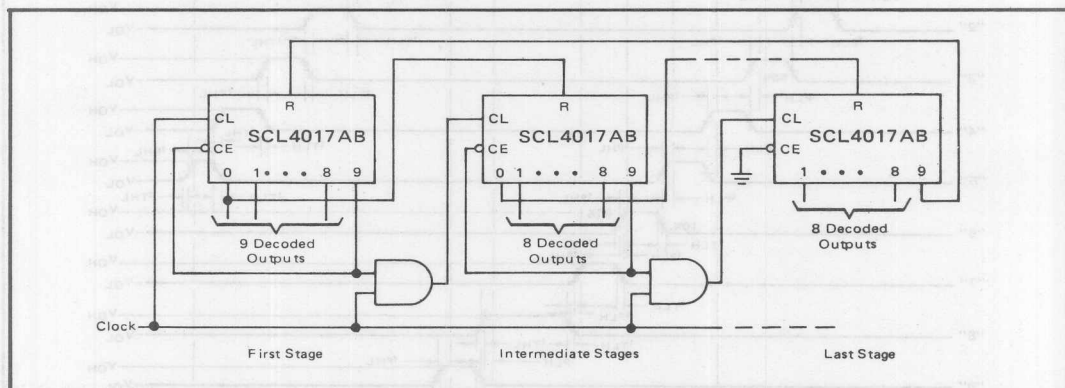
LOGIC DIAGRAM



APPLICATIONS INFORMATION

COUNTER EXPANSION

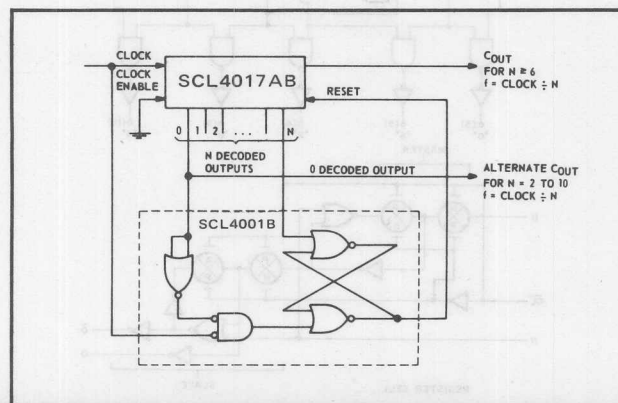
This figure shows a technique for extending the number of decoded output states for the SCL4017AB. Decoded outputs are sequential within each stage and from stage to stage, with no dead time (except propagation delay).



DIVIDE-BY-N COUNTER

When the Nth decoded output is reached (Nth clock pulse), the S-R flip-flop (constructed from the SCL4001B) generates a reset pulse which clears the SCL4017AB to its zero count. At this time, if the Nth decoded output is greater than or equal to 6, the **COUT** line goes high to clock the next counter section. The "O" decoded output also goes high at this time. Coincidence of the clock "low" and decoded "O" output "high" resets the S-R flip-flop to enable the SCL4017AB.

If the Nth decoded output is less than 6, the **COUT** line will not go high, and, therefore, cannot be used. In this case, the "O" decoded output may be used to perform the clock function for the next counter.



SCL4018B



CMOS PRESETTABLE DIVIDE-BY-N COUNTER

FEATURES

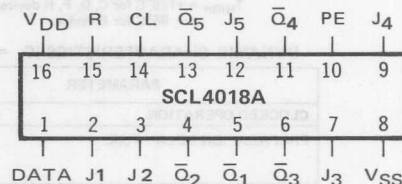
- ◆ Divide by any Number Between 2 and 10 with One External Gate
- ◆ Johnson Counter Configuration for Spike-Free Counting
- ◆ Fully Static operation - DC to 5MHz @ 10Vdc

DESCRIPTION

The SCL4018B consists of 5 Johnson-Counter stages, buffered Q outputs from each stage, and counter preset control gating. Clock, Reset, Data, Preset Enable, and 5 individual Jam inputs are provided. Divide-by 10, 8, 6, 4, or 2 counter configurations can be implemented by feeding the Q5, Q4, Q3, Q2, Q1 signals, respectively, back to the Data input. Divide-by-9, 7, 5, or 3 counter configurations can be implemented by use of a single SCL4018B gate to properly gate the feedback connections to the Data input. Divide-by functions greater than 10 can be achieved by use of multiple SCL4018B units. The counter is advanced one count at the positive clock-signal transition. A high Reset signal clears the counter to an all-zero condition. A high Preset-Enable signal allows information on the Jam inputs to preset the counter. Reset and Preset gating is provided to assure the proper counting sequence.

This device is particularly useful in frequency-division and control applications.

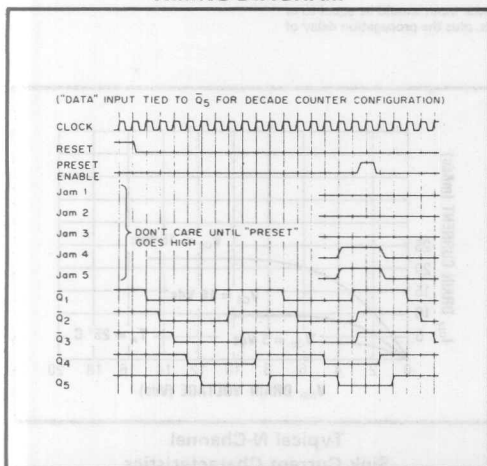
CONNECTION DIAGRAM (all packages)



Add suffix for package:

- C 16-pin Cerdip
- D 16-pin Ceramic
- E 16-pin Epoxy
- F 16-pin Flat
- H Chip

TIMING DIAGRAM

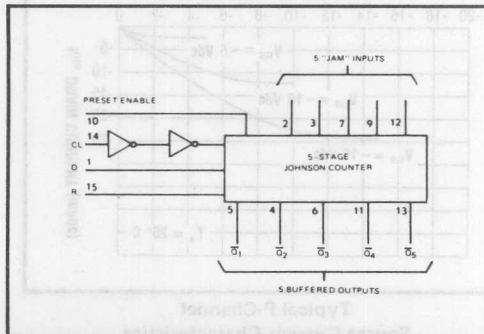


RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A	-55 to +125	°C
C, D, F, H Device		-40 to +85	°C
E Device			

BLOCK DIAGRAM



QUIESCENT DEVICE CURRENT	V_{DD}										
	5	$V_{IN} = V_{SS}$ or V_{DD}	—	5	—	0.05	5	—	150	μA_{dc}	
	10	All valid input	—	10	—	0.1	10	—	300		
	15	combinations	—	20	—	0.2	20	—	600		

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

² $T_{LOW} = -55^{\circ}C$ for C, D, F, H device.

$T_{LOW} = -40^{\circ}C$ for E device.

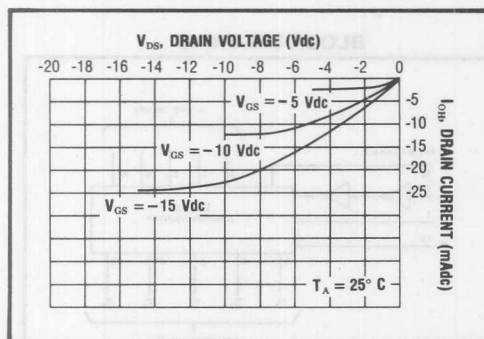
$T_{HIGH} = +125^{\circ}C$ for C, D, F, H device.

$T_{HIGH} = +85^{\circ}C$ for E device.

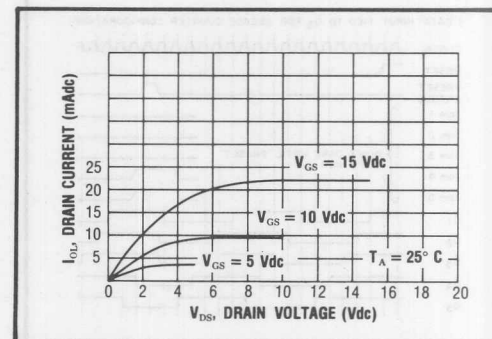
DYNAMIC CHARACTERISTICS ($C_L = 50pF$, $T_A = 25^{\circ}C$)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
CLOCKED OPERATION						
PROPAGATION DELAY TIME	t_{PLH}, t_{PHL}	5	—	500	1000	ns
		10	—	150	300	
		15	—	120	240	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	—	130	260	ns
		10	—	65	130	
		15	—	50	100	
MINIMUM CLOCK PULSE WIDTH	PW_{CL}	5	—	200	400	ns
		10	—	100	200	
		15	—	80	160	
MAXIMUM CLOCK FREQUENCY	f_{CL}	5	1.25	2.5	—	MHz
		10	2.5	5.0	—	
		15	3.0	6.0	—	
MAXIMUM CLOCK RISE AND FALL TIME ¹	t_{rCL}, t_{fCL}	5	15	—	—	μs
		10	15	—	—	
		15	5	—	—	
MINIMUM DATA INPUT SETUP TIME	t_{setup}	5	—	200	400	ns
		10	—	100	200	
		15	—	80	160	
MINIMUM DATA INPUT HOLD TIME	t_{hold}	5	—	0	100	ns
		10	—	0	50	
		15	—	0	40	
PRESET OR RESET OPERATION						
PROPAGATION DELAY TIME From PE or Reset Input	t_{PLH}, t_{PHL}	5	—	500	1000	ns
		10	—	250	500	
		15	—	200	400	
MINIMUM PRESET OR RESET PULSE WIDTH	PW_{PR}, PW_{R}	5	—	200	400	ns
		10	—	100	200	
		15	—	80	160	
MINIMUM JAM INPUT SETUP TIME	t_{setup}	5	—	200	400	ns
		10	—	100	200	
		15	—	80	160	
PRESET OR RESET REMOVAL TIME	t_{rem}	5	—	375	750	ns
		10	—	125	250	
		15	—	90	180	

¹ When units are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the transition times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitive load.

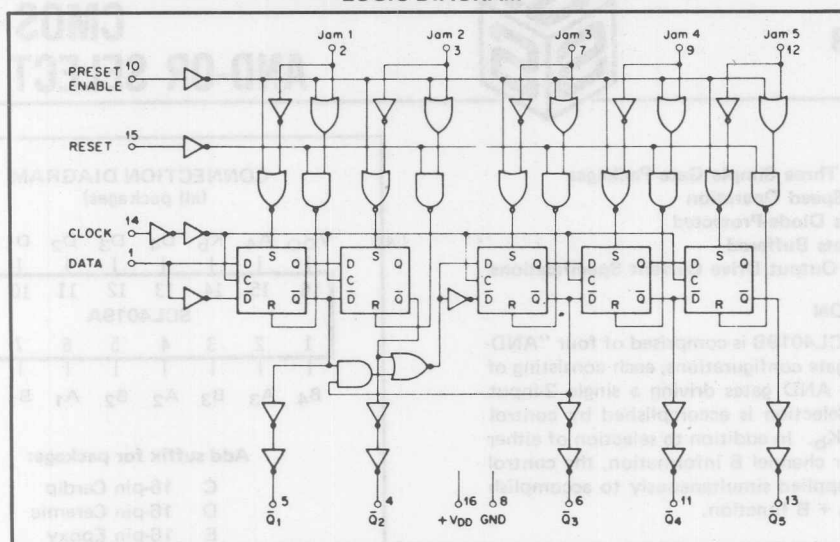


Typical P-Channel
Source Current Characteristics

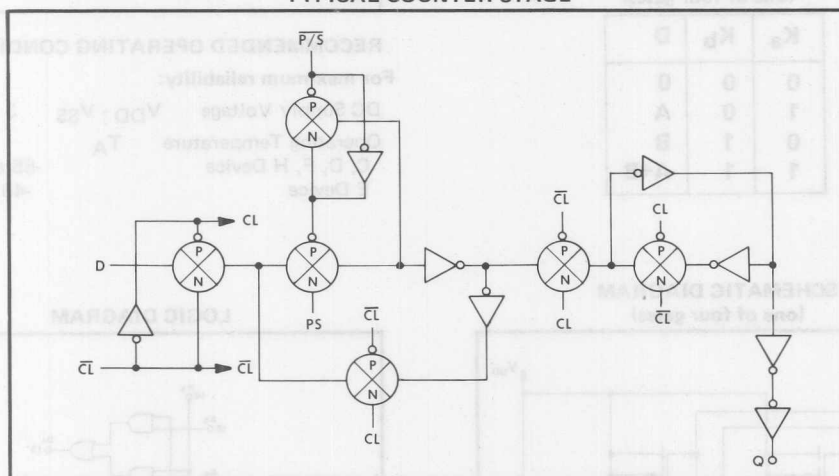


Typical N-Channel
Sink Current Characteristics

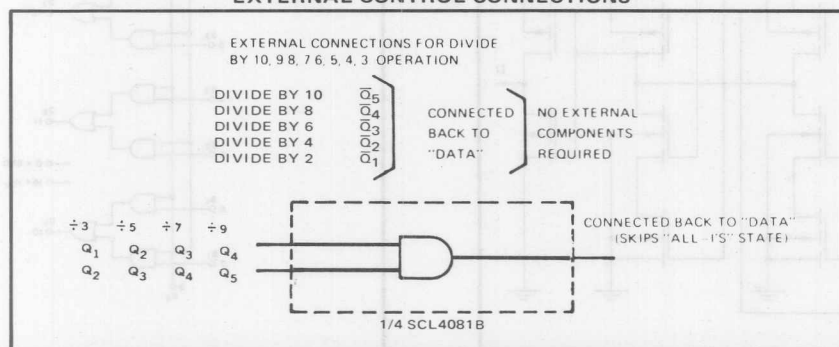
LOGIC DIAGRAM



TYPICAL COUNTER STAGE



EXTERNAL CONTROL CONNECTIONS





CMOS QUAD AND-OR SELECT GATE

FEATURES

- ◆ Replaces Three Simple Gate Packages
- ◆ Medium Speed Operation
- ◆ All Inputs Diode-Protected
- ◆ All Outputs Buffered
- ◆ Balanced Output Drive Current Specifications

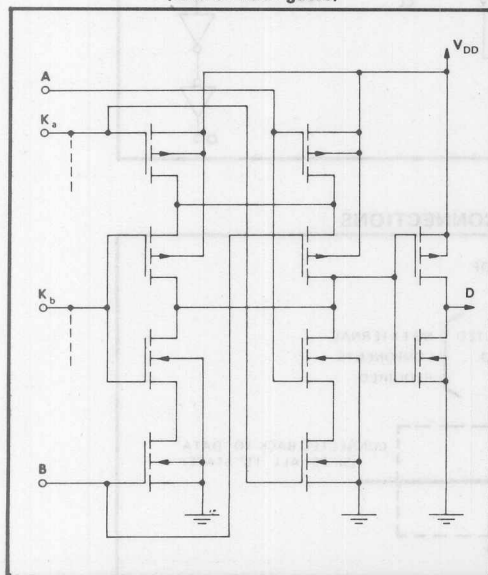
DESCRIPTION

The SCL4019B is comprised of four "AND-OR Select" gate configurations, each consisting of two 2-input AND gates driving a single 2-input OR gate. Selection is accomplished by control bits K_a and K_b . In addition to selection of either channel A or channel B information, the control bits can be applied simultaneously to accomplish the logical A + B function.

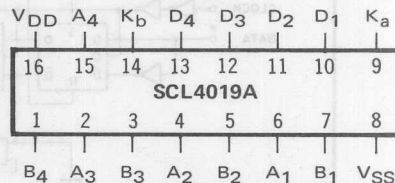
TRUTH TABLE
(one of four gates)

K_a	K_b	D
0	0	0
1	0	A
0	1	B
1	1	A+B

SCHEMATIC DIAGRAM
(one of four gates)



CONNECTION DIAGRAM
(all packages)



Add suffix for package:

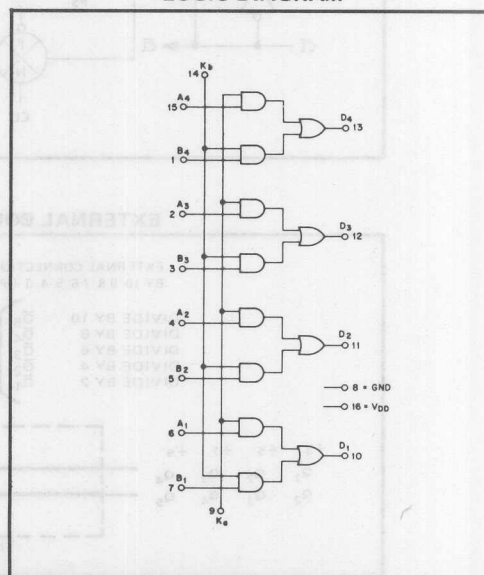
- C 16-pin Cerdip
- D 16-pin Ceramic
- E 16-pin Epoxy
- F 16-pin Flat
- H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A	-55 to +125	°C
C, D, F, H Device		-40 to +85	°C
E Device			

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS^{1,3}

PARAMETER	V_{DD} (Vdc)	CONDITIONS	T_{LOW}^2		+25°C			T_{HIGH}^2		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I_{DD}	$V_{IN}=V_{SS}$ or V_{DD} All valid input combinations	—	1.0	—	0.005	1.0	—	30	μA_{dc}
			—	2.0	—	0.01	2.0	—	60	
			—	4.0	—	0.02	4.0	—	120	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

² $T_{LOW} = -55^\circ C$ for C, D, F, H device.

$= -40^\circ C$ for E device.

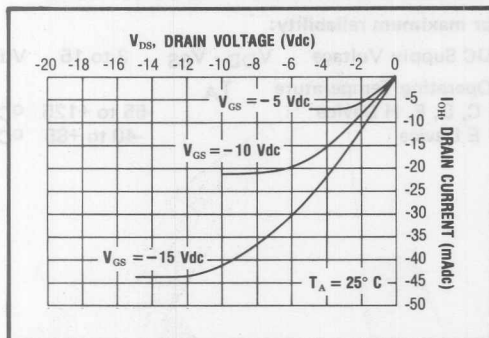
$T_{HIGH} = +125^\circ C$ for C, D, F, H device.

$= +85^\circ C$ for E device.

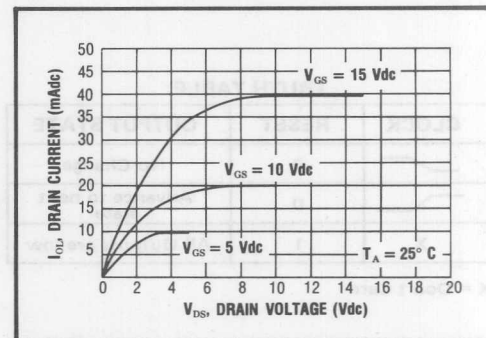
³ This device has been designed for balanced output drive current specifications. Consult Family Specifications.

DYNAMIC CHARACTERISTICS ($C_L = 50pF$, $T_A = 25^\circ C$)

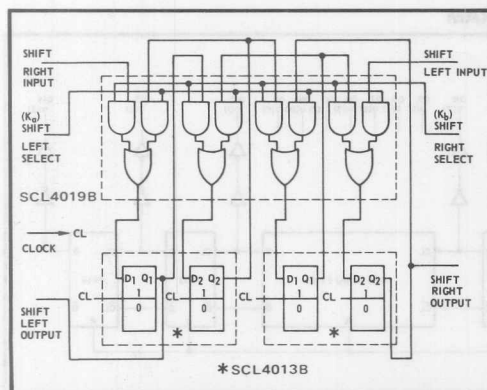
PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME From Any Input	t_{PLH}, t_{PHL}	5	—	150	300	ns
		10	—	60	120	
		15	—	50	100	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	—	100	200	ns
		10	—	50	100	
		15	—	40	80	



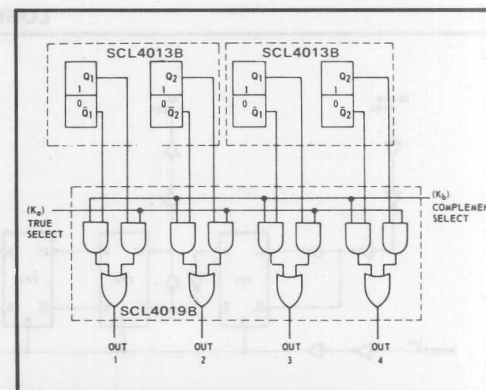
Typical P-Channel
Source Current Characteristics



Typical N-Channel
Sink Current Characteristics



"Shift left/shift right" register.



"True/complement" selector.

FEATURES

- ◆ 14 Fully Static Stages
- ◆ Buffered Outputs Available from 12 Stages
- ◆ Common Reset Line
- ◆ 8MHz Counting Rate @ 10Vdc
- ◆ All Inputs Buffered

DESCRIPTION

The SCL4020AB consists of 14 ripple-carry binary counter stages with appropriate input buffers and reset circuitry. Buffered outputs are externally available from stages 1, and 4 through 14. The counter is reset to its "all zeroes" state by a high level on the Reset input. The counter is advanced one count on the negative-going transition of each input pulse. Isolation from external noise and the effects of loading is provided by output buffering.

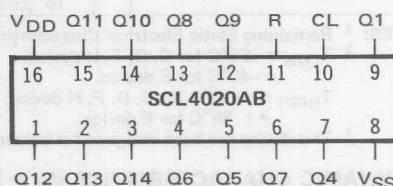
Applications include time delay circuits, counter controls, and frequency-dividing circuits.

TRUTH TABLE

CLOCK	RESET	OUTPUT STATE
	0	No Change
	0	Advance to next state
X	1	All Outputs are low

X = Don't Care

CONNECTION DIAGRAM (all packages)



Add suffix for package:

- C 16-pin Cerdip
- D 16-pin Ceramic
- E 16-pin Epoxy
- F 16-pin Flat
- H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

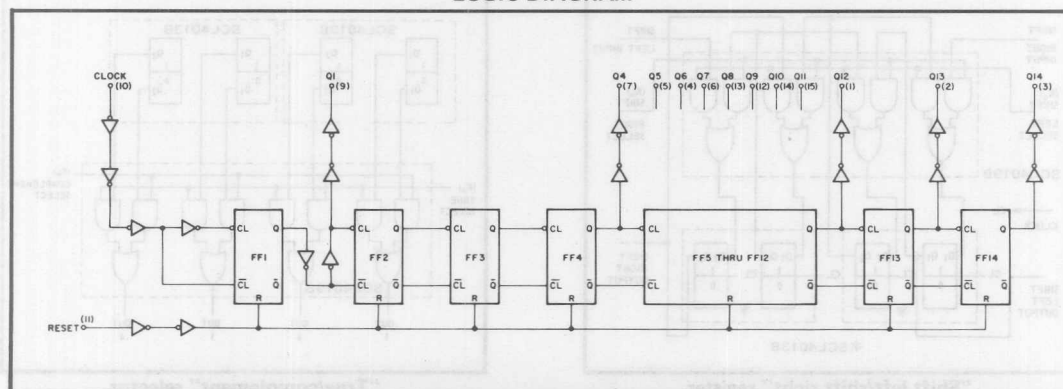
DC Supply Voltage $V_{DD} - V_{SS}$ 3 to 15 Vdc

Operating Temperature T_A

C, D, F, H Device -55 to +125 °C

E Device -40 to +85 °C

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS¹

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT I _{DD}	5	V _{IN} =V _{SS} or V _{DD}	—	5	—	0.05	5	—	150	μAdc
	10	All valid input combinations	—	10	—	0.1	10	—	300	
	15		—	15	—	0.2	20	—	600	
OUTPUT HIGH (SOURCE) CURRENT C, D, F, H device	5	V _{OH} = 4.6V	-0.15	—	-0.12	-0.5	—	-0.08	—	mAdc
	10	V _{OH} = 9.5V	-0.37	—	-0.3	-1.15	—	-0.21	—	
	15	V _{OH} = 13.5V V _{IN} =V _{SS} or V _{DD}	-1.25	—	-1.0	-4.5	—	-0.69	—	
E device	5	V _{OH} = 4.6V	-0.14	—	-0.12	-0.5	—	-0.10	—	mAdc
	10	V _{OH} = 9.5V	-0.35	—	-0.3	-1.15	—	-0.25	—	
	15	V _{OH} = 13.5V V _{IN} =V _{SS} or V _{DD}	-1.2	—	-1.0	-4.5	—	-0.85	—	
OUTPUT LOW (SINK) CURRENT C, D, F, H device	5	V _{OL} = 0.4V	0.15	—	0.12	0.5	—	0.08	—	mAdc
	10	V _{OL} = 0.5V	0.37	—	0.3	1.0	—	0.21	—	
	15	V _{OL} = 1.5V V _{IN} =V _{SS} or V _{DD}	1.25	—	1.0	5.8	—	0.69	—	
E device	5	V _{OL} = 0.4V	0.14	—	0.12	0.5	—	0.10	—	mAdc
	10	V _{OL} = 0.5V	0.35	—	0.3	1.0	—	0.25	—	
	15	V _{OL} = 1.5V V _{IN} =V _{SS} or V _{DD}	1.2	—	1.0	5.8	—	0.85	—	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

² T_{LOW} = -55°C for C, D, F, H device.

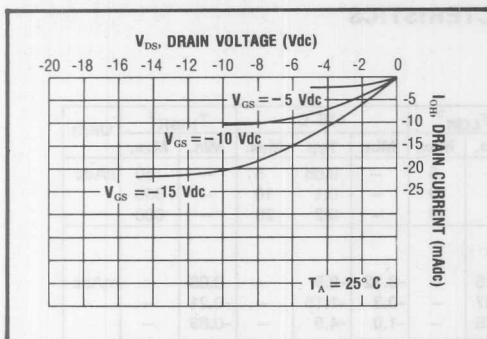
= -40°C for E device.

T_{HIGH} = +125°C for C, D, F, H device.

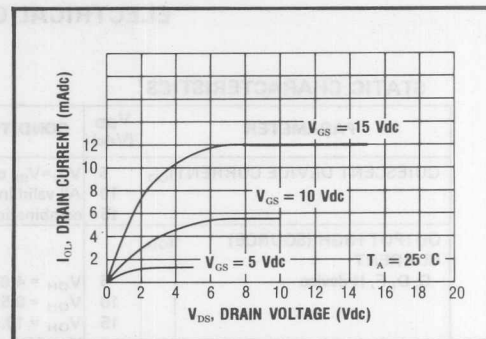
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V _{DD} (Vdc)	Min.	Typ.	Max.	Units	
CLOCKED OPERATION							
PROPAGATION DELAY TIME Clock to Q1	t _{PLH} , t _{PHL}	5	—	200	400	ns	
		10	—	100	200		
		15	—	80	160		
	Q _i to Q _i + 1	t _{PLH} , t _{PHL}	5	—	150	300	ns
			10	—	75	150	
			15	—	60	120	
OUTPUT TRANSITION TIME	t _{TLH} , t _{THL}	5	—	180	360	ns	
		10	—	90	180		
		15	—	65	130		
MINIMUM CLOCK PULSE WIDTH	PW _{CL}	5	—	100	200	ns	
		10	—	50	100		
		15	—	40	80		
MAXIMUM CLOCK FREQUENCY	f _{CL}	5	2.0	4.0	—	MHz	
		10	4.0	8	—		
		15	5	10	—		
MAXIMUM CLOCK RISE AND FALL TIME	t _{rCL} , t _{fCL}	5	15	—	—	μs	
		10	15	—	—		
		15	5	—	—		
RESET OPERATION							
PROPAGATION DELAY TIME	t _{PHL}	5	—	300	600	ns	
		10	—	150	300		
		15	—	120	240		
MINIMUM RESET PULSE WIDTH	PW _R	5	—	150	300	ns	
		10	—	75	150		
		15	—	60	120		
RESET REMOVAL TIME	t _{rem}	5	—	250	500	ns	
		10	—	125	250		
		15	—	100	200		

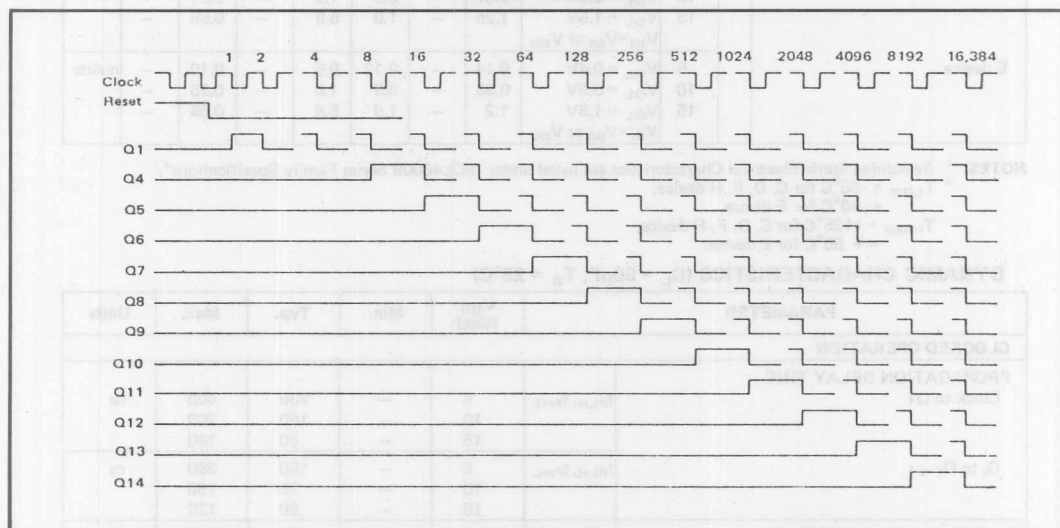


Typical P-Channel
Source Current Characteristics

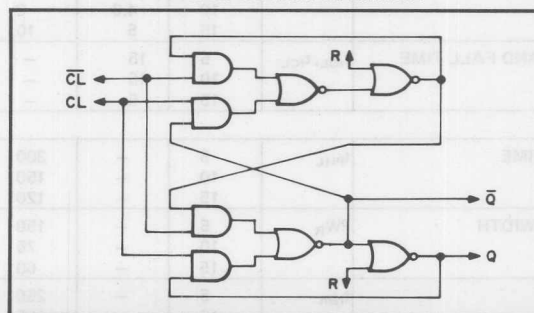


Typical N-Channel
Sink Current Characteristics

TIMING DIAGRAM



TYPICAL COUNTER STAGE





CMOS 8-STAGE STATIC SHIFT REGISTER

FEATURES

- ◆ Asynchronous Parallel Input/Serial Output
- ◆ Synchronous Serial Input/Serial Output
- ◆ Fully Static Operation - DC to 8MHz @ 10Vdc
- ◆ Q Outputs from Stages 6, 7, and 8 Available

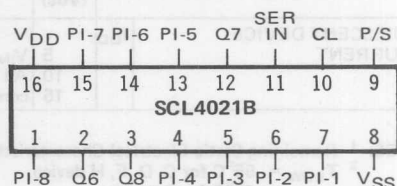
DESCRIPTION

The SCL4021B is an 8-Stage Parallel or Serial-Input/Serial-Output Shift Register having common Clock and Parallel/Serial Control inputs, a single Serial Data input, and individual parallel Jam inputs to each register stage. Each register stage is a D-type, master-slave flip-flop. "Q" outputs are available from the sixth, seventh, and eighth stages. When the Parallel/Serial Control input is low, data is serially shifted into the 8-stage register synchronously with the positive-going transition of the Clock pulse.

When the Parallel/Serial Control input is "high" data is jammed into the 8-stage register via the Parallel input line asynchronously with the Clock line.

Register expansion is possible using additional SCL4021B packages.

CONNECTION DIAGRAM (all packages)



Add suffix for package:

C	16-pin Cerdip	F	16-pin Flat
D	16-pin Ceramic	H	Chip
E	16-pin Epoxy		

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage $V_{DD} - V_{SS}$ 3 to 15 Vdc

Operating Temperature T_A -55 to +125 °C

C, D, F, H Device -40 to +85 °C

E Device

TRUTH TABLE

SERIAL OPERATION:

t	CLOCK	SER IN	P/S	Q6 t=n+6	Q7 t=n+7	Q8 t=n+8
n		0	0	0	?	?
n+1		1	0	1	0	?
n+2		0	0	0	1	0
n+3		1	0	1	0	1
		X	0	Q6	Q7	Q8

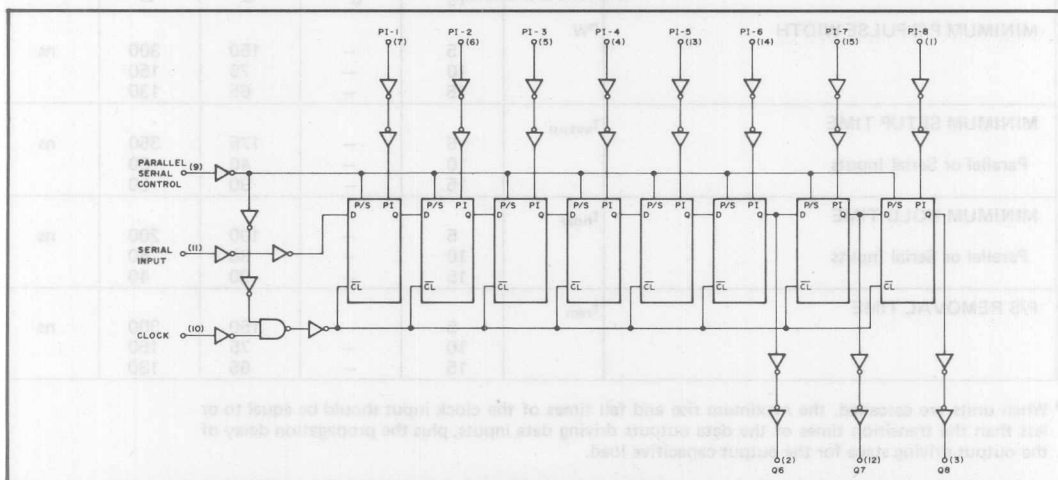
PARALLEL OPERATION:

CLOCK	SER IN	P/S	PI-m	*Q _m
X	X	1	0	0
X	X	1	1	1

*Q6, Q7, & Q8 are available externally

X = Don't Care

LOGIC DIAGRAM



STATIC CHARACTERISTICS ¹

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	5 V _{IN} = V _{SS} or V _{DD}	—	5	—	0.05	5	—	150	μAdc
		10 All valid input combinations	—	10	—	0.01	10	—	300	
		15	—	20	—	0.2	20	—	600	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

² T_{LOW} = -55°C for C, D, F, H device.

= -40°C for E device.

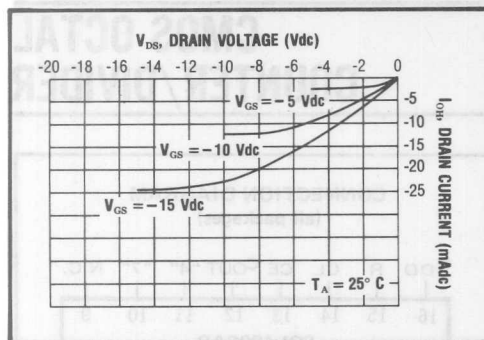
T_{HIGH} = +125°C for C, D, F, H device.

= +85°C for E device.

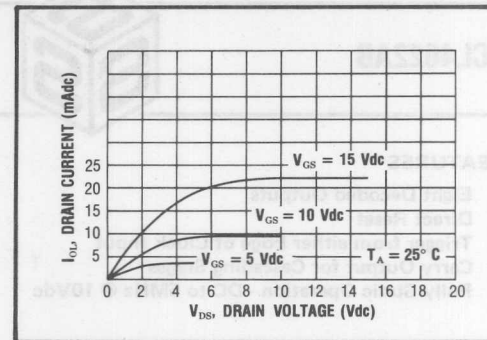
DYNAMIC CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

PARAMETER	V _{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME	t _{PLH} , t _{PHL}				
From Clock or P/S Input	5	—	250	500	ns
	10	—	100	200	
	15	—	80	160	
OUTPUT TRANSITION TIME	t _{TLH} , t _{THL}				
	5	—	130	260	ns
	10	—	65	130	
	15	—	50	100	
MINIMUM CLOCK PULSE WIDTH	PW _{CL}				
	5	—	125	250	ns
	10	—	50	100	
	15	—	40	80	
MAXIMUM CLOCK FREQUENCY	f _{CL}				
	5	2.0	4.0	—	MHz
	10	4.0	8.0	—	
	15	6.0	12.0	—	
MAXIMUM CLOCK RISE & FALL TIME ¹	t _{rCL} , t _{fCL}				
	5	15	—	—	μs
	10	15	—	—	
	15	5	—	—	
MINIMUM P/S PULSE WIDTH	PW				
	5	—	150	300	ns
	10	—	75	150	
	15	—	65	130	
MINIMUM SETUP TIME	t _{setup}				
Parallel or Serial Inputs	5	—	175	350	ns
	10	—	40	80	
	15	—	30	60	
MINIMUM HOLD TIME	t _{hold}				
Parallel or Serial Inputs	5	—	100	200	ns
	10	—	30	60	
	15	—	20	40	
P/S REMOVAL TIME	t _{rem}				
	5	—	150	300	ns
	10	—	75	150	
	15	—	65	130	

¹ When units are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the transition times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitive load.

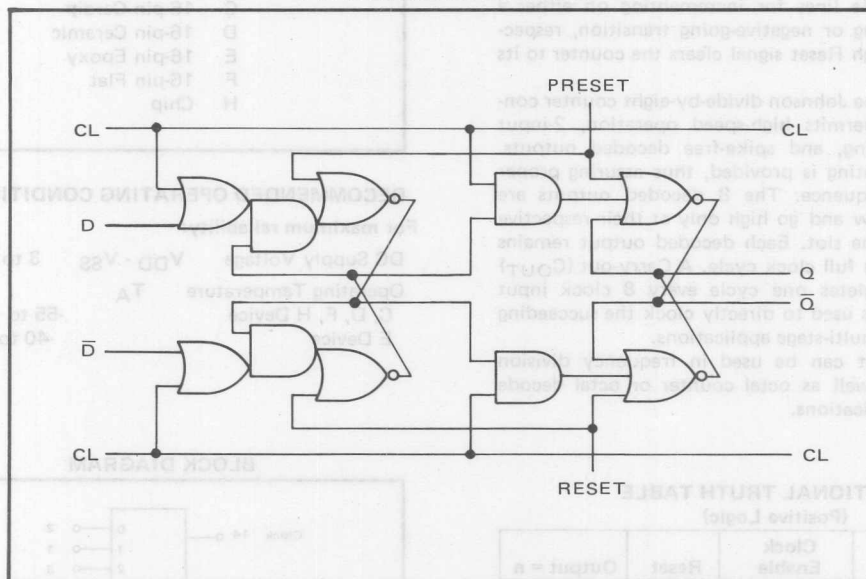


Typical P-Channel
Source Current Characteristics



Typical N-Channel
Sink Current Characteristics

TYPICAL REGISTER STAGE





FEATURES

- ◆ Eight Decoded Outputs
- ◆ Direct Reset
- ◆ Trigger from either Edge of Clock Input
- ◆ Carry Output for Cascading Stages
- ◆ Fully Static Operation - DC to 5MHz @ 10Vdc

DESCRIPTION

The SCL4022AB consists of a 4-stage Johnson Divide-by-8 Counter and an Output Decoder. Inputs include Clock, Reset, and Clock Enable signals.

The counter has interchangeable Clock and Clock Enable lines for incrementing on either a positive-going or negative-going transition, respectively. A high Reset signal clears the counter to its zero count.

Use of the Johnson divide-by-eight counter configuration permits high-speed operation, 2-input decode gating, and spike-free decoded outputs. Anti-lock gating is provided, thus assuring proper counting sequence. The 8 decoded outputs are normally low and go high only at their respective decoded time slot. Each decoded output remains high for one full clock cycle. A Carry-out (C_{OUT}) signal completes one cycle every 8 clock input cycles and is used to directly clock the succeeding counter in multi-stage applications.

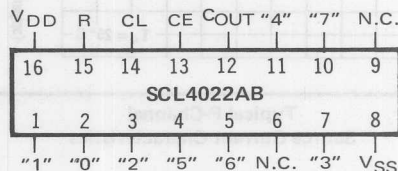
This part can be used in frequency division circuits as well as octal counter or octal decode display applications.

FUNCTIONAL TRUTH TABLE
(Positive Logic)

Clock	Clock Enable	Reset	Output = n
0	X	0	n
X	1	0	n
	0	0	n + 1
	X	0	n
1		0	n + 1
X		0	n
X	X	1	"0"

X Don't Care If $n < 4$ Carry = 1, otherwise = 0

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

- C 16-pin Cerdip
- D 16-pin Ceramic
- E 16-pin Epoxy
- F 16-pin Flat
- H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

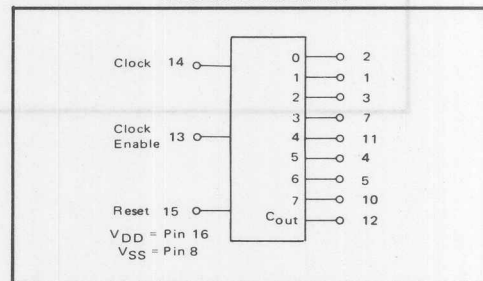
DC Supply Voltage $V_{DD} - V_{SS}$ 3 to 15 Vdc

Operating Temperature T_A

C, D, F, H Device -55 to +125 °C

E Device -40 to +85 °C

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS¹

PARAMETER	V _{DD} (V _{dc})	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	5 V _{IN} = V _{SS} or V _{DD}	—	5	—	0.05	5	—	150	μAdc
		10 All valid input combinations	—	10	—	0.1	10	—	300	
		15	—	20	—	0.2	20	—	600	
OUTPUT HIGH (SOURCE) CURRENT C, D, F, H device: Decoded Outputs	I _{OH}	5 V _{OH} = 4.6V	-0.05	—	-0.04	-0.3	—	-0.028	—	mAdc
		10 V _{OH} = 9.5V	-0.125	—	-0.1	-0.75	—	-0.07	—	
		15 V _{OH} = 13.5V V _{IN} = V _{SS} or V _{DD}	-0.375	—	-0.3	-2.5	—	-0.21	—	
Carry Output		5 V _{OH} = 4.6V	-0.25	—	-0.2	-0.75	—	-0.14	—	mAdc
		10 V _{OH} = 9.5V	-0.62	—	-0.5	-1.1	—	-0.35	—	
		15 V _{OH} = 13.5V V _{IN} = V _{SS} or V _{DD}	-1.9	—	-1.5	-3.5	—	-1.1	—	
E device: Decoded Outputs	I _{OH}	5 V _{OH} = 4.6V	-0.048	—	-0.04	-0.3	—	-0.032	—	mAdc
		10 V _{OH} = 9.5V	-0.12	—	-0.1	-0.75	—	-0.08	—	
		15 V _{OH} = 13.5V V _{IN} = V _{SS} or V _{DD}	-0.36	—	-0.3	-2.5	—	-0.24	—	
Carry Output		5 V _{OH} = 4.6V	-0.24	—	-0.2	-0.75	—	-0.16	—	mAdc
		10 V _{OH} = 9.5V	-0.6	—	-0.5	-1.1	—	-0.4	—	
		15 V _{OH} = 13.5V V _{IN} = V _{SS} or V _{DD}	-1.8	—	-1.5	-3.5	—	-1.2	—	
OUTPUT LOW (SINK) CURRENT C, D, F, H device: Decoded Outputs	I _{OL}	5 V _{OL} = 0.4V	0.05	—	0.04	0.4	—	0.028	—	mAdc
		10 V _{OL} = 0.5V	0.125	—	0.1	1.0	—	0.07	—	
		15 V _{OL} = 1.5V V _{IN} = V _{SS} or V _{DD}	0.375	—	0.3	3.0	—	0.21	—	
Carry Output		5 V _{OL} = 0.4V	0.25	—	0.2	0.75	—	0.14	—	mAdc
		10 V _{OL} = 0.5V	0.62	—	0.5	1.3	—	0.35	—	
		15 V _{OL} = 1.5V V _{IN} = V _{SS} or V _{DD}	1.9	—	1.5	4.0	—	1.1	—	
E device: Decoded Outputs	I _{OL}	5 V _{OL} = 0.4V	0.048	—	0.04	0.4	—	0.032	—	mAdc
		10 V _{OL} = 0.5V	0.12	—	0.1	1.0	—	0.08	—	
		15 V _{OL} = 1.5V V _{IN} = V _{SS} or V _{DD}	0.36	—	0.3	3.0	—	0.24	—	
Carry Output		5 V _{OL} = 0.4V	0.24	—	0.2	0.75	—	0.16	—	mAdc
		10 V _{OL} = 0.5V	0.6	—	0.5	1.3	—	0.4	—	
		15 V _{OL} = 1.5V V _{IN} = V _{SS} or V _{DD}	1.8	—	1.5	4.0	—	1.2	—	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

² T_{LOW} = -55°C for C, D, F, H device.

= -40°C for E device.

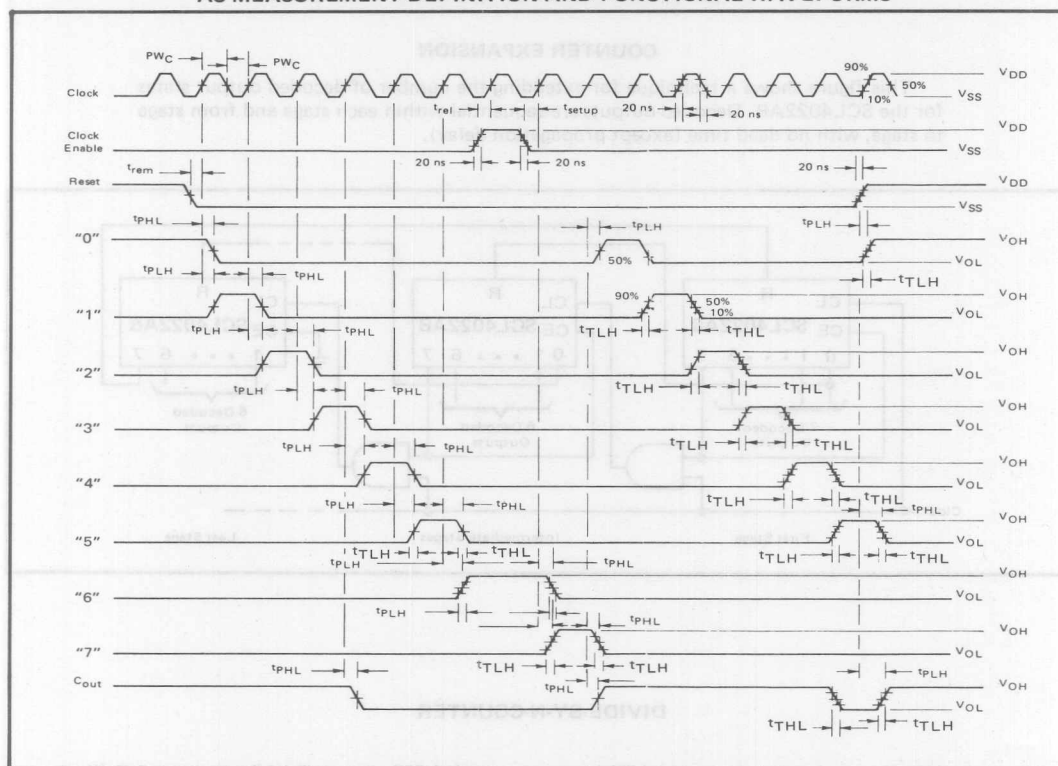
T_{HIGH} = +125°C for C, D, F, H device.

= + 85°C for E device.

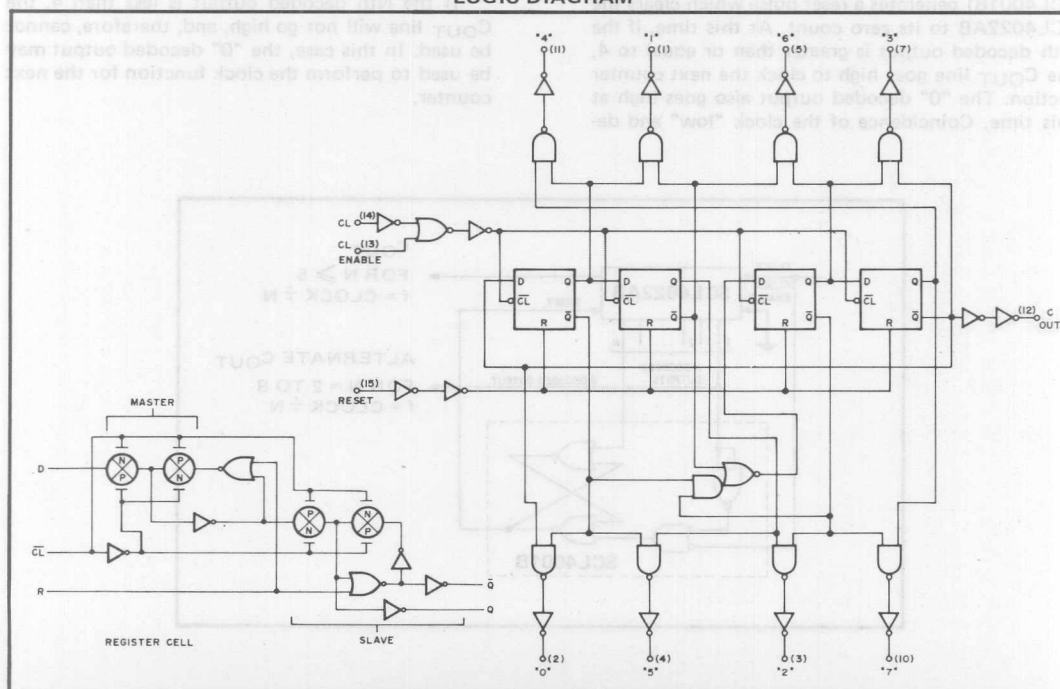
DYNAMIC CHARACTERISTICS ($C_L = 50\text{pF}$, $T_A = 25^\circ\text{C}$)

PARAMETER		V _{DD} (Vdc)	Min.	Typ.	Max.	Units
CLOCKED OPERATION						
PROPAGATION DELAY TIME	t _{PLH} , t _{PHL}	5	—	600	1200	ns
To Decoded Outputs		10	—	240	480	
		15	—	180	360	
To Carry Output	t _{PLH} , t _{PHL}	5	—	500	1000	ns
	10	—	200	400		
	15	—	150	300		
OUTPUT TRANSITION TIME	t _{TLH} , t _{THL}	5	—	250	500	ns
Decoded Outputs		10	—	125	250	
		15	—	90	180	
Carry Output	t _{TLH} , t _{THL}	5	—	180	360	ns
	10	—	90	180		
	15	—	65	130		
MINIMUM CLOCK PULSE WIDTH	PW _{CL}	5	—	200	400	ns
		10	—	100	200	
		15	—	80	160	
MAXIMUM CLOCK FREQUENCY	f _{CL}	5	1.25	2.5	—	MHz
		10	2.5	5.0	—	
		15	3.0	6.0	—	
MAXIMUM CLOCK OR ENABLE RISE AND FALL TIME	t _{rCL} , t _{fCL}	5	15	—	—	μs
		10	15	—	—	
		15	5	—	—	
MINIMUM ENABLE SETUP TIME	t _{setup}	5	—	175	350	ns
		10	—	75	150	
		15	—	55	110	
MINIMUM ENABLE REMOVAL TIME	t _{rem}	5	—	250	500	ns
		10	—	100	200	
		15	—	75	150	
RESET OPERATION						
PROPAGATION DELAY TIME	t _{PLH} , t _{PHL}	5	—	500	1000	ns
To Decoded Outputs		10	—	200	400	
		15	—	140	280	
To Carry Output	t _{PLH}	5	—	400	800	ns
	10	—	150	300		
	15	—	110	220		
MINIMUM RESET PULSE WIDTH	PW _R	5	—	150	300	ns
		10	—	75	150	
		15	—	60	120	
RESET REMOVAL TIME	t _{rem}	5	—	250	500	ns
		10	—	100	200	
		15	—	80	160	

AC MEASUREMENT DEFINITION AND FUNCTIONAL WAVEFORMS



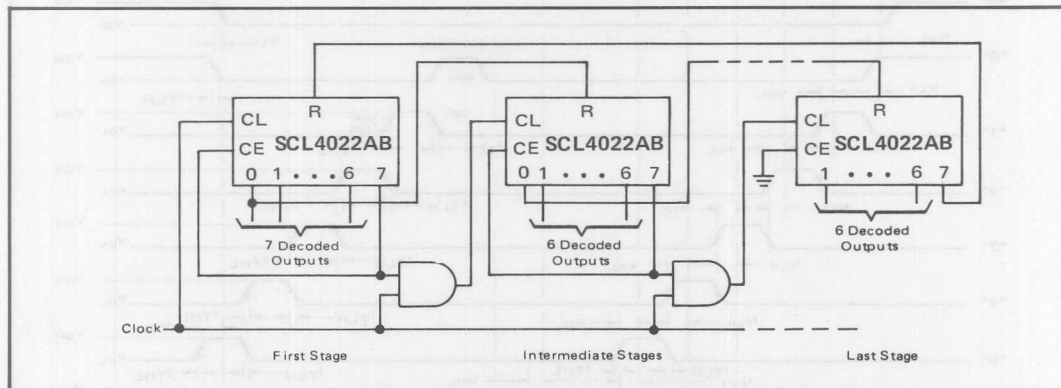
LOGIC DIAGRAM



APPLICATIONS INFORMATION

COUNTER EXPANSION

This figure shows a technique for extending the number of decoded output states for the SCL4022AB. Decoded outputs are sequential within each stage and from stage to stage, with no dead time (except propagation delay).

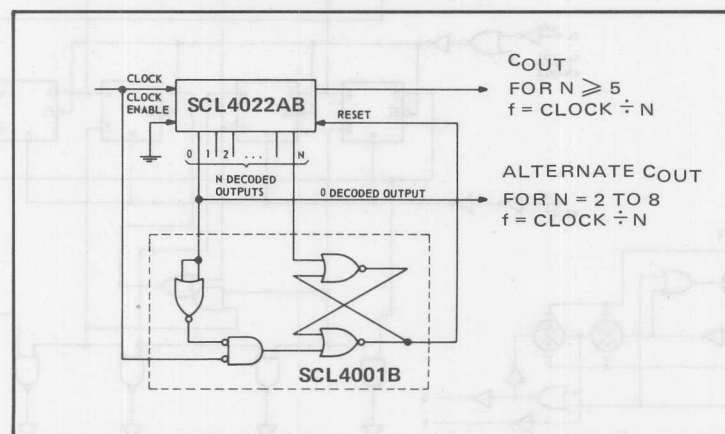


DIVIDE-BY-N-COUNTER

When the Nth decoded output is reached (Nth clock pulse) the S-R flip-flop (constructed from the SCL4001B) generates a reset pulse which clears the SCL4022AB to its zero count. At this time, if the Nth decoded output is greater than or equal to 4, the COUT line goes high to clock the next counter section. The "0" decoded output also goes high at this time. Coincidence of the clock "low" and de-

coded "0" output "high" resets the S-R flip-flop to enable the SCL4022AB.

If the Nth decoded output is less than 4, the COUT line will not go high, and, therefore, cannot be used. In this case, the "0" decoded output may be used to perform the clock function for the next counter.





CMOS 7-STAGE BINARY COUNTER

FEATURES

- ◆ 7 Fully Static Stages
- ◆ Buffered Outputs Available from All Stages
- ◆ Common Reset Line
- ◆ 8 MHz Counting Rate @ 10Vdc
- ◆ All Inputs Buffered

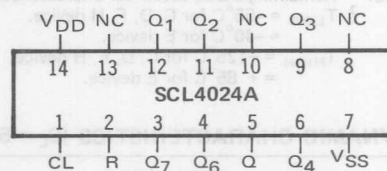
DESCRIPTION

The SCL4024B is a single chip monolithic medium scale integrated circuit containing N-Channel and P-Channel enhancement-mode MOS transistors. Seven single-phase clocked counting stages are provided with the Q output of each stage accessible. The Counter is reset to "zero" by a high level on the Reset input. Each counter stage is a static master-slave flip-flop. The counter state is advanced one count on the negative-going transition of each input pulse.

TRUTH TABLE

Clock	Reset	State
0	0	No Change
0	1	All Outputs Low
1	0	No Change
1	1	All Outputs Low
	0	No Change
	1	All Outputs Low
	0	Advance One Count
	1	All Outputs Low

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

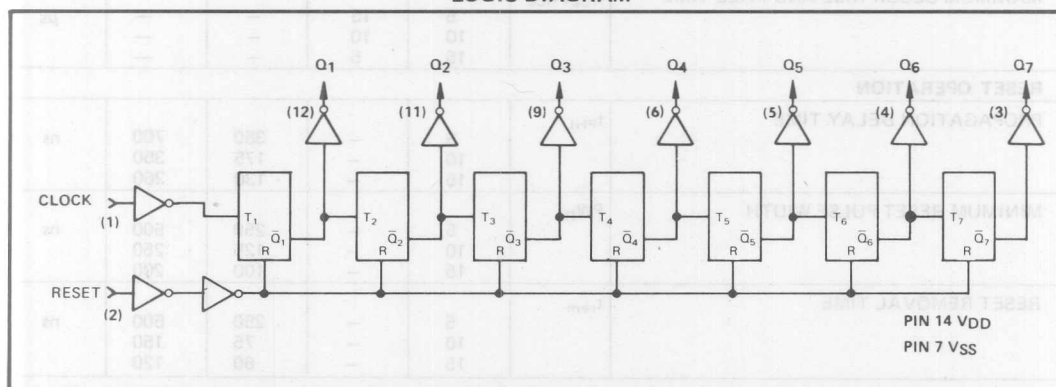
- C 14-pin Cerdip
- D 14-pin Ceramic
- E 14-pin Epoxy
- F 14-pin Flat
- H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

LOGIC DIAGRAM



QUIESCENT DEVICE CURRENT	I_{DD}	$V_{IN} = V_{SS}$ or V_{DD} All valid input combinations	—	5	—	0.05	5	—	150	μA_{dc}
	5									
	10									
	15									

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

² $T_{LOW} = -55^{\circ}C$ for C, D, F, H device.

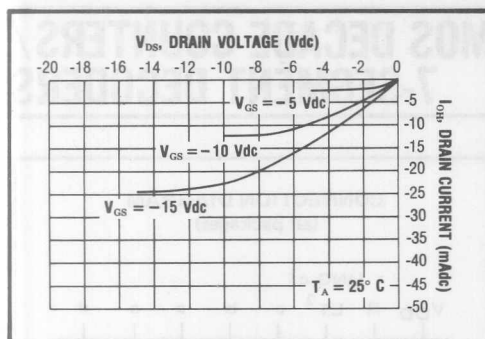
= $-40^{\circ}C$ for E device.

$T_{HIGH} = +125^{\circ}C$ for C, D, F, H device.

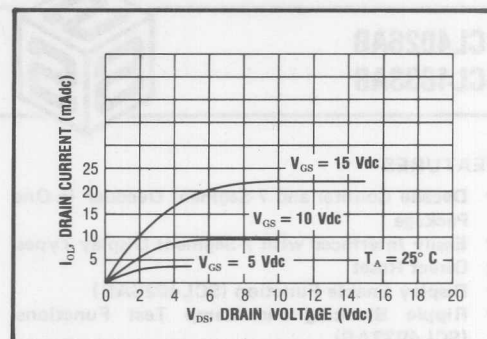
= $+85^{\circ}C$ for E device.

DYNAMIC CHARACTERISTICS ($C_L = 50$ pF, $T_A = 25^{\circ}C$)

PARAMETER		V _{DD} (V _{DC})	Min.	Typ.	Max.	Units	
CLOCKED OPERATION							
PROPAGATION DELAY TIME Clock to Q ₁	t _{PLH} , t _{PHL}	5	—	200	400	ns	
		10	—	100	200		
		15	—	80	160		
	Q _i to Q _{i+1}	t _{PLH} , t _{PHL}	5	—	125	250	ns
			10	—	60	120	
			15	—	45	90	
OUTPUT TRANSITION TIME	t _{TLH} , t _{THL}	5	—	130	260	ns	
		10	—	65	130		
		15	—	50	100		
MINIMUM CLOCK PULSE WIDTH	PW _{CL}	5	—	165	330	ns	
		10	—	60	120		
		15	—	45	90		
MAXIMUM CLOCK FREQUENCY	f _{CL}	5	1.5	3.0	—	MHz	
		10	4.0	8.0	—		
		15	5.5	11	—		
MAXIMUM CLOCK RISE AND FALL TIME	t _{rCL} , t _{fCL}	5	15	—	—	μs	
		10	10	—	—		
		15	5	—	—		
RESET OPERATION							
PROPAGATION DELAY TIME	t _{PHL}	5	—	350	700	ns	
		10	—	175	350		
		15	—	130	260		
MINIMUM RESET PULSE WIDTH	PW _R	5	—	250	500	ns	
		10	—	125	250		
		15	—	100	200		
RESET REMOVAL TIME	t _{rem}	5	—	250	500	ns	
		10	—	75	150		
		15	—	60	120		

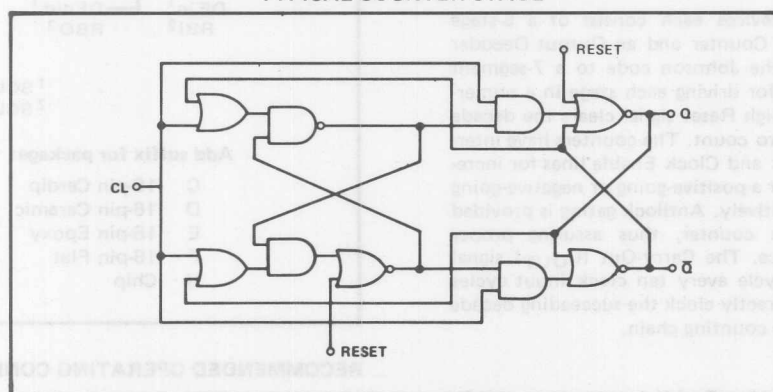


Typical P-Channel
Source Current Characteristics



Typical N-Channel
Sink Current Characteristics

TYPICAL COUNTER STAGE



SCL4026AB SCL4033AB



CMOS DECADE COUNTERS/ 7-SEGMENT DECODERS

FEATURES

- ◆ Decade Counter and 7-Segment Decoder in One Package
- ◆ Easily Interfaced with 7-Segment Display Types
- ◆ Direct Reset
- ◆ Display Enable Function (SCL4026AB)
- ◆ Ripple Blanking and Lamp Test Functions (SCL4033AB)
- ◆ Trigger from either Edge of Clock Input
- ◆ Carry Output for Cascading Stages
- ◆ Fully Static Operation - DC to 5MHz @ 10Vdc

DESCRIPTION

These two devices each consist of a 5-stage Johnson Decade Counter and an Output Decoder which converts the Johnson code to a 7-segment decoded output for driving each stage in a numerical display. A high Reset signal clears the decade counter to its zero count. The counters have interchangeable Clock and Clock Enable lines for incrementing on either a positive-going or negative-going transition, respectively. Antilock gating is provided on the Johnson counter, thus assuring proper counting sequence. The Carry-Out (C_{OUT}) signal completes one cycle every ten clock input cycles and is used to directly clock the succeeding decade in a multi-decade counting chain.

SCL4026AB

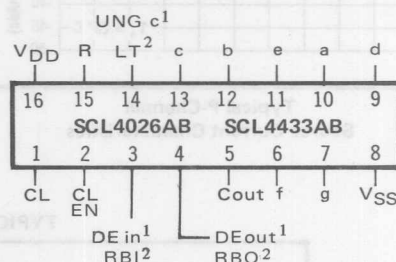
When the Display Enable is low, the seven decoded outputs are forced off regardless of the state of the counter. Activation of the display only when required results in significant power savings. This system also facilitates implementation of display-character multiplexing.

The Carry Out and ungated "C-segment" signals are not gated by the Display Enable and therefore are available continuously. This feature is a requirement in implementation of certain divider functions such as divide-by-60 and divide-by-12.

SCL4033AB

The SCL4033AB has provisions for automatic blanking of the non-significant zeros in a multi-digit decimal number which results in an easily readable display consistent with normal writing practice. For example, the number 0050.0700 in an eight digit display would be displayed as 50.07. Zero suppression on the integer side is obtained by connecting the RBI terminal of the SCL4033AB associated with the most significant digit in the display to a "low-level" voltage and connecting the RBO terminal of that stage to the RBI terminal of the SCL4033AB in the next-lower-significant position in the display. This procedure is continued for each succeeding SCL4033AB on the integer side of the display. On the fraction side of the display the

CONNECTION DIAGRAM (all packages)



¹ SCL4026AB

² SCL4033AB

Add suffix for package:

C	16-pin Cerdip
D	16-pin Ceramic
E	16-pin Epoxy
F	16-pin Flat
H	Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

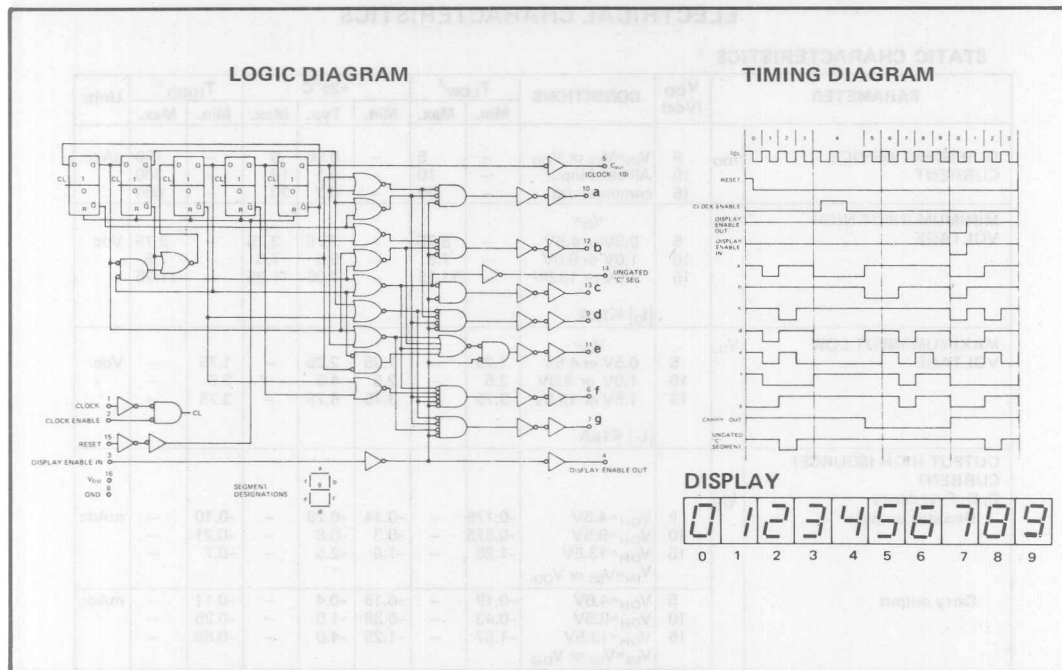
DC Supply Voltage	V _{DD} - V _{SS}	3 to 15	Vdc
Operating Temperature	T _A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

RBI of the SCL4033AB associated with the least significant digit is connected to a "low-level" voltage and the RBO of the SCL4033AB is connected to the RBI terminal of the SCL4033AB in the next-more-significant-digit position. Again, this procedure is continued for each SCL4033AB on the fraction side of the display.

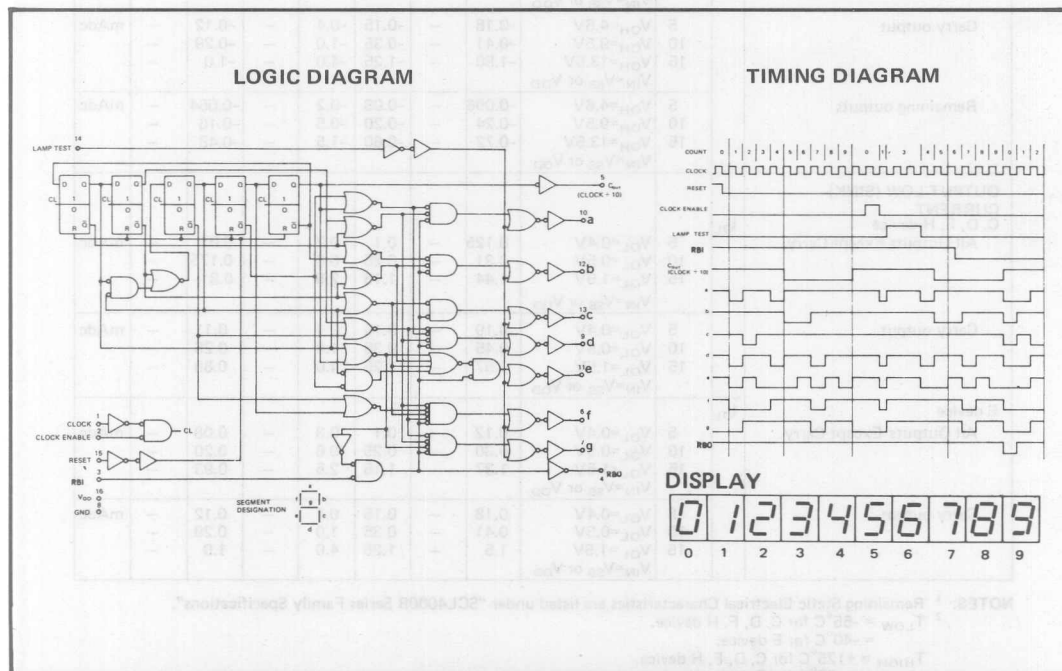
In a purely fractional number the zero immediately preceding the decimal point can be displayed by connecting the RBI of that stage to a high voltage (instead of to the RBO of the next-more-significant stage). For Example: optional zero - 0.7346.

Likewise, the zero in a number such as 763.0 can be displayed by connecting the RBI of the SCL4033AB associated with it to a "high-level" voltage.

A "high" Lamp Test signal turns on all outputs.



SCL4026AB Decode Counter/7-Segment Decoder with Display Enable



SCL4033AB Decode Counter/7-Segment Decoder with Ripple Blanking

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS ¹

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	5 V _{IN} =V _{SS} or V _{DD}	—	5	—	0.05	5	—	150	μAdc
		10 All valid input combinations	—	10	—	0.1	10	—	300	
		15	—	20	—	0.2	20	—	600	
MINIMUM INPUT HIGH VOLTAGE	V _{IH}	5 V _O = 0.5V or 4.5V	—	3.75	—	2.75	3.75	—	3.75	Vdc
		10 1.0V or 9.0V	—	7.5	—	5.5	7.5	—	7.5	
		15 1.5V or 13.5V	—	11.25	—	8.25	11.25	—	11.25	
		I _O ≤ 1μA								
MAXIMUM INPUT LOW VOLTAGE	V _{IL}	5 V _O = 0.5V or 4.5V	1.25	—	1.25	2.25	—	1.75	—	Vdc
		10 1.0V or 9.0V	2.5	—	2.5	4.5	—	2.5	—	
		15 1.5V or 13.5V	3.75	—	3.75	6.75	—	3.75	—	
		I _O ≤ 1μA								
OUTPUT HIGH (SOURCE) CURRENT C, D, F, H device Decoded outputs	I _{OH}	5 V _{OH} =4.6V	-0.175	—	-0.14	-0.28	—	-0.10	—	mAdc
		10 V _{OH} =9.5V	-0.375	—	-0.3	-0.6	—	-0.21	—	
		15 V _{OH} =13.5V	-1.25	—	-1.0	-2.5	—	-0.7	—	
		V _{IN} =V _{SS} or V _{DD}								
		5 V _{OH} =4.6V	-0.19	—	-0.15	-0.4	—	-0.11	—	mAdc
		10 V _{OH} =9.5V	-0.43	—	-0.35	-1.0	—	-0.25	—	
		15 V _{OH} =13.5V	-1.57	—	-1.25	-4.0	—	-0.88	—	
		V _{IN} =V _{SS} or V _{DD}								
		5 V _{OH} =4.6V	-0.10	—	-0.08	-0.2	—	-0.056	—	mAdc
		10 V _{OH} =9.5V	-0.25	—	-0.20	-0.5	—	-0.14	—	
		15 V _{OH} =13.5V	-0.75	—	-0.60	-1.5	—	-0.42	—	
		V _{IN} =V _{SS} or V _{DD}								
E device Decoded outputs	I _{OH}	5 V _{OH} =4.6V	-0.168	—	-0.14	-0.28	—	-0.112	—	mAdc
		10 V _{OH} =9.5V	-0.36	—	-0.3	-0.6	—	-0.24	—	
		15 V _{OH} =13.5V	-1.2	—	-1.0	-2.5	—	-0.8	—	
		V _{IN} =V _{SS} or V _{DD}								
		5 V _{OH} =4.6V	-0.18	—	-0.15	-0.4	—	-0.12	—	mAdc
		10 V _{OH} =9.5V	-0.41	—	-0.35	-1.0	—	-0.29	—	
		15 V _{OH} =13.5V	-1.50	—	-1.25	-4.0	—	-1.0	—	
		V _{IN} =V _{SS} or V _{DD}								
		5 V _{OH} =4.6V	-0.096	—	-0.08	-0.2	—	-0.064	—	mAdc
		10 V _{OH} =9.5V	-0.24	—	-0.20	-0.5	—	-0.16	—	
		15 V _{OH} =13.5V	-0.72	—	-0.60	-1.5	—	-0.48	—	
		V _{IN} =V _{SS} or V _{DD}								
OUTPUT LOW (SINK) CURRENT C, D, F, H device All Outputs Except Carry	I _{OL}	5 V _{OL} =0.4V	0.125	—	0.1	0.3	—	0.07	—	mAdc
		10 V _{OL} =0.5V	0.31	—	0.25	0.6	—	0.175	—	
		15 V _{OL} =1.5V	1.44	—	1.15	2.5	—	0.81	—	
		V _{IN} =V _{SS} or V _{DD}								
		5 V _{OL} =0.4V	0.19	—	0.15	0.4	—	0.11	—	mAdc
		10 V _{OL} =0.5V	0.45	—	0.35	1.0	—	0.25	—	
		15 V _{OL} =1.5V	1.57	—	1.25	4.0	—	0.88	—	
		V _{IN} =V _{SS} or V _{DD}								
		5 V _{OL} =0.4V	0.12	—	0.1	0.3	—	0.08	—	mAdc
		10 V _{OL} =0.5V	0.30	—	0.25	0.6	—	0.20	—	
		15 V _{OL} =1.5V	1.37	—	1.15	2.5	—	0.93	—	
		V _{IN} =V _{SS} or V _{DD}								
Carry output	I _{OL}	5 V _{OL} =0.4V	0.18	—	0.15	0.4	—	0.12	—	mAdc
		10 V _{OL} =0.5V	0.41	—	0.35	1.0	—	0.29	—	
		15 V _{OL} =1.5V	1.5	—	1.25	4.0	—	1.0	—	
		V _{IN} =V _{SS} or V _{DD}								

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".² T_{LOW} = -55°C for C, D, F, H device.

= -40°C for E device.

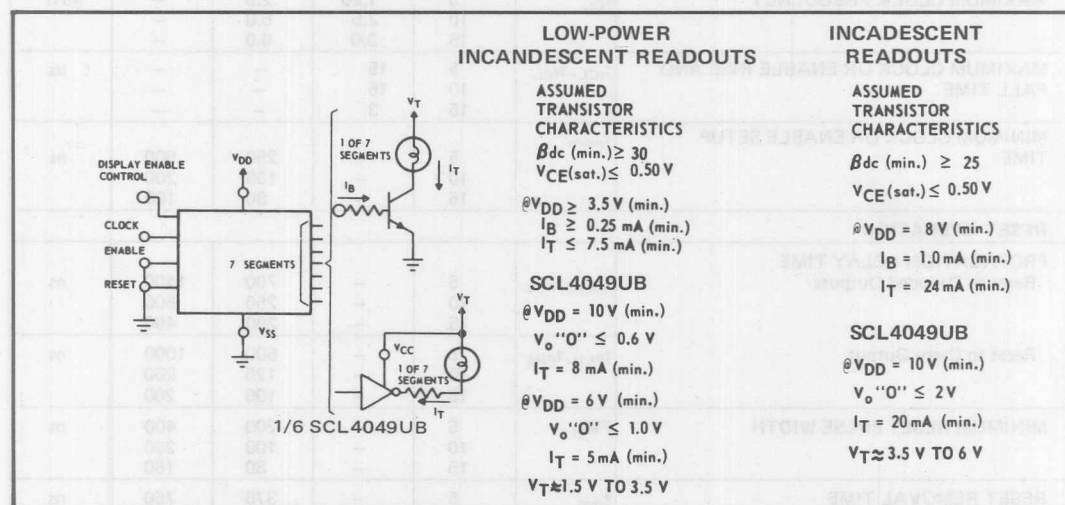
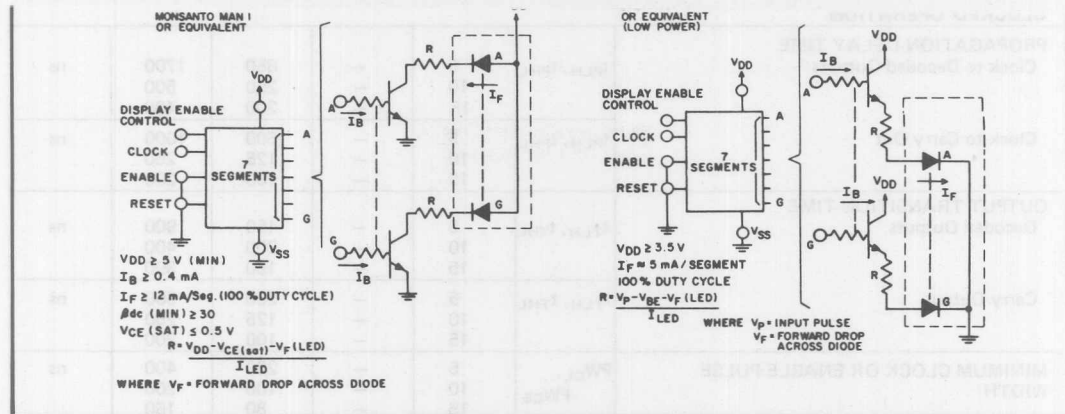
T_{HIGH} = +125°C for C, D, F, H device.

= + 85°C for E device.

ELECTRICAL CHARACTERISTICS (Continued)

DYNAMIC CHARACTERISTICS ($C_L = 50\text{pF}$, $T_A = 25^\circ\text{C}$)

PARAMETER		V _{DD} (V _{dc})	Min.	Typ.	Max.	Units
CLOCKED OPERATION						
PROPAGATION DELAY TIME Clock to Decoded Outputs	t _{PLH} , t _{PHL}	5	—	850	1700	ns
		10	—	250	500	
		15	—	200	400	
Clock to Carry Out	t _{PLH} , t _{PHL}	5	—	500	1000	ns
		10	—	125	250	
		15	—	100	200	
OUTPUT TRANSITION TIME Decoded Outputs	t _{TLH} , t _{THL}	5	—	450	900	ns
		10	—	200	400	
		15	—	150	300	
Carry Output	t _{TLH} , t _{THL}	5	—	250	500	ns
		10	—	125	250	
		15	—	100	200	
MINIMUM CLOCK OR ENABLE PULSE WIDTH	PW _{CL} , PW _{CE}	5	—	200	400	ns
		10	—	100	200	
		15	—	80	160	
MAXIMUM CLOCK FREQUENCY	f _{CL}	5	1.25	2.5	—	MHz
		10	2.5	5.0	—	
		15	3.0	6.0	—	
MAXIMUM CLOCK OR ENABLE RISE AND FALL TIME	t _{rCL} , t _{fCL}	5	15	—	—	μs
		10	15	—	—	
		15	3	—	—	
MINIMUM CLOCK OR ENABLE SETUP TIME	t _{setup}	5	—	250	500	ns
		10	—	100	200	
		15	—	80	160	
RESET OPERATION						
PROPAGATION DELAY TIME Reset to Decoded Outputs	t _{PLH} , t _{PHL}	5	—	700	1400	ns
		10	—	250	500	
		15	—	200	400	
Reset to Carry Output	t _{PLH} , t _{PHL}	5	—	500	1000	ns
		10	—	125	250	
		15	—	100	200	
MINIMUM RESET PULSE WIDTH	PW _R	5	—	200	400	ns
		10	—	100	200	
		15	—	80	160	
RESET REMOVAL TIME	t _{rem}	5	—	375	750	ns
		10	—	150	300	
		15	—	125	250	



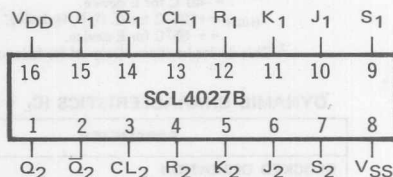


FEATURES

- ◆ Individual Set and Reset Controls
- ◆ Fully Static Operation
- ◆ Logic Edge-Clocked Design
- ◆ 8MHz Toggle Rate @ 10Vdc
- ◆ Balanced Output Drive Current Specifications

DESCRIPTION

The SCL4027B consists of two identical independent CMOS J-K master-slave Flip-Flops. The SCL4027B is useful in performing control, register, and toggle functions. Logic levels present at the J and K inputs along with internal self-steering control the state of each flip-flop; changes in the flip-flop state are synchronous with the positive-going transition of the Clock pulse. Set and Reset functions are independent of the Clock and are initiated when a high level signal is present at either the Set or Reset input.

CONNECTION DIAGRAM
(all packages)

Add suffix for package:

C	16-pin Cerdip	F	16-pin Flat
D	16-pin Ceramic	H	Chip
E	16-pin Epoxy		

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage $V_{DD} - V_{SS}$ 3 to 15 VdcOperating Temperature T_A

C, D, F, H Device -55 to +125 °C

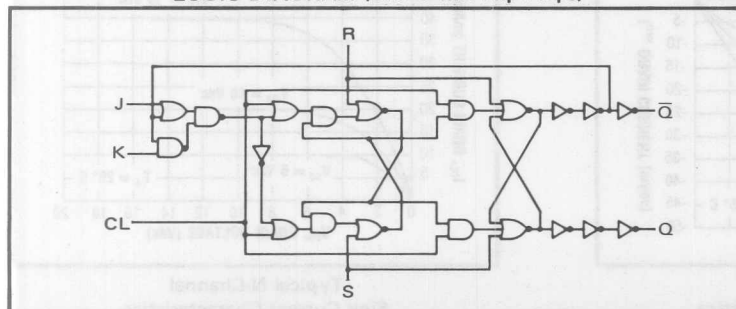
E Device -40 to +85 °C

TRUTH TABLE

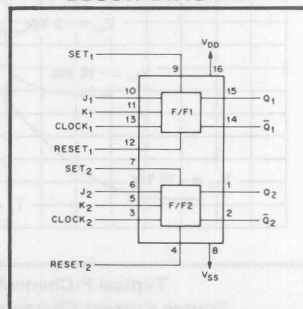
$\bullet t_{n-1}$ INPUTS						$\dagger t_n$ OUTPUTS	
CL▲	J	K	S	R	Q	Q	Q̄
	1	X	0	0	0	1	0
	X	0	0	0	1	1	0
	0	X	0	0	0	0	1
	X	1	0	0	1	0	1
	X	X	0	0	X	(No Change)	
X	X	X	1	0	X	1	0
X	X	X	0	1	X	0	1
X	X	X	1	1	X	1	1

WHERE 1 = HIGH LEVEL
0 = LOW LEVEL▲ - LEVEL CHANGE
X - DON'T CARE● - t_{n-1} REFERS TO THE INTERVAL PRIOR TO THE POSITIVE CLOCK PULSE TRANSITION† - t_n REFERS TO THE TIME INTERVAL AFTER THE POSITIVE CLOCK PULSE TRANSITION

LOGIC DIAGRAM (one of two Flip-Flops)



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS^{1,3}

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	5	—	1.0	—	0.005	1.0	—	30	μAdc
		10	—	2.0	—	0.01	2.0	—	60	
		15	—	4.0	—	0.02	4.0	—	120	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

² T_{LOW} = -55°C for C, D, F, H device.

= -40°C for E device.

T_{HIGH} = +125°C for C, D, F, H device.

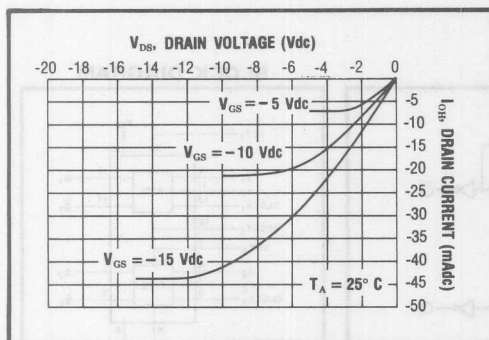
= + 85°C for E device.

³ This device has been designed for balanced output drive current specifications. Consult Family Specifications.

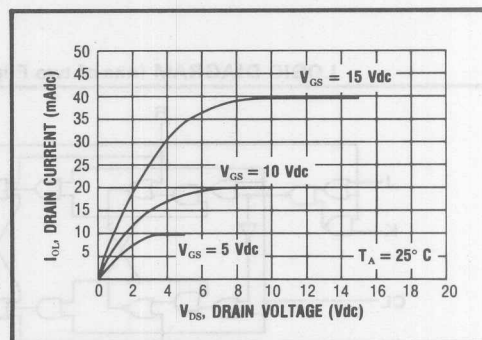
DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V _{DD} (V _{dc})	Min.	Typ.	Max.	Units
CLOCKED OPERATION						
PROPAGATION DELAY TIME	t _{PLH} , t _{PHL}	5 10 15	— — —	175 80 60	350 160 120	ns
OUTPUT TRANSITION TIME	t _{TLH} , t _{THL}	5 10 15	— — —	100 50 40	200 100 80	ns
MINIMUM CLOCK PULSE WIDTH	PW _{CL}	5 10 15	— — —	165 60 50	330 120 100	ns
MAXIMUM CLOCK FREQUENCY	f _{CL}	5 10 15	1.5 4.0 5.0	3.0 8.0 10	—	MHz
MAXIMUM CLOCK RISE AND FALL TIME ¹	t _{rCL} , t _{fCL}	5 10 15	15 5 3	— — —	— — —	μs
MINIMUM SETUP TIME	t _{setup}	5 10 15	— — —	100 50 40	200 100 80	ns
MINIMUM HOLD TIME	t _{hold}	5 10 15	— — —	-25 -10 -5	0 0 0	ns
SET AND RESET OPERATION						
PROPAGATION DELAY TIME S to Q, R to Q	t _{PLH}	5 10 15	— — —	150 70 55	300 140 110	ns
MINIMUM SET AND RESET PULSE WIDTH	PW _S , PW _R	5 10 15	— — —	100 50 40	200 100 80	ns
SET AND RESET REMOVAL TIME	t _{rem}	5 10 15	— — —	0 0 0	25 10 5	ns

¹ When units are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the transition times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitive load.



Typical P-Channel
Source Current Characteristics



Typical N-Channel
Sink Current Characteristics



FEATURES

- ◆ BCD-to-Decimal or Binary-to-Octal Decoding
- ◆ Buffered Outputs go High on Selection
- ◆ Low Outputs for all Illegal Input Combinations
- ◆ Balanced Output Drive Current Specifications

DESCRIPTION

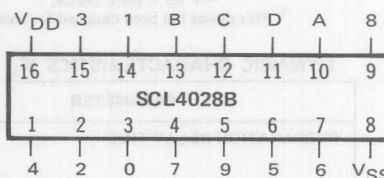
The SCL4028B types are BCD-to-Decimal or Binary-to-Octal Decoders consisting of pulse shaping circuits on all 4 inputs, decoding/logic gates, and 10 output buffers. A BCD code applied to the four inputs, A to D, results in a high level at the selected one of 10 decimal decoded outputs. Similarly, a 3-bit binary code applied to inputs A through C is decoded in octal code at output 0 to 7. A high-level signal at the D input inhibits octal decoding and causes outputs 0 through 7 to go low. If unused, the D input must be connected to V_{SS} .

Expanded decoding such as binary-to-hexadecimal (1-of-16), etc., can be achieved by using other SCL4028B devices. This part is useful for code conversion, address decoding, memory selection control, demultiplexing, and readout decoding.

TRUTH TABLE

Input				Output									
D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	1	0	0	0	0	0	0	0	0	1	0
0	0	1	0	0	0	0	0	0	0	0	1	0	0
0	0	1	1	0	0	0	0	0	0	1	0	0	0
0	1	0	0	0	0	0	0	0	1	0	0	0	0
0	1	0	1	0	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	0	1	0	0	0	0	0	0
0	1	1	1	0	0	1	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0	0	0	0	0	0	0
1	0	0	1	1	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

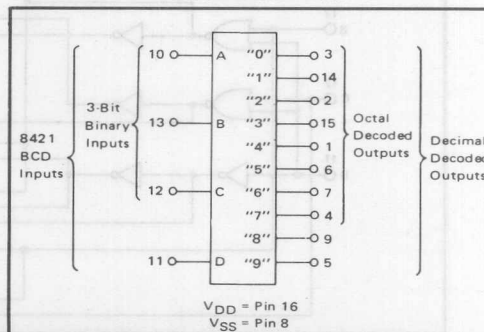
- C 16-pin Cerdip
- D 16-pin Ceramic
- E 16-pin Epoxy
- F 16-pin Flat
- H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A	-55 to +125	°C
C, D, F, H Device		-40 to +85	°C
E Device			

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS^{1, 3}

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	V _{IN} =V _{SS} or V _{DD} All valid input combinations	—	5	—	0.05	5	—	150	μAdc
			—	10	—	0.1	10	—	300	
			—	20	—	0.2	20	—	600	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

² T_{LOW} = -55°C for C, D, F, H device.

= -40°C for E device.

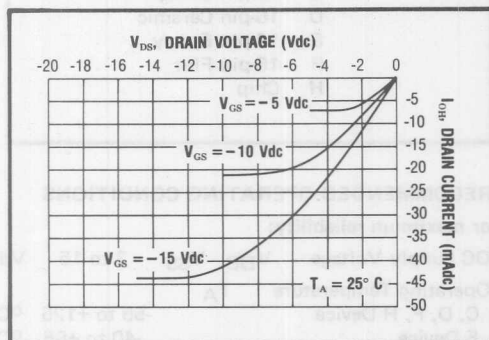
T_{HIGH} = +125°C for C, D, F, H device.

= + 85°C for E device.

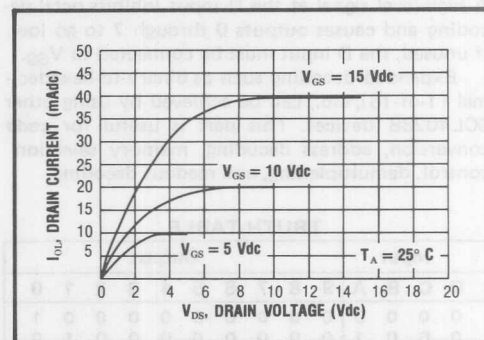
³ This device has been designed for balanced output drive current specifications. Consult Family Specifications.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V _{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME	t _{PLH} , t _{PHL}	5	—	225	450	ns
		10	—	100	200	
		15	—	70	140	
OUTPUT TRANSITION TIME	t _{TLH} , t _{THL}	5	—	100	200	ns
		10	—	50	100	
		15	—	40	80	

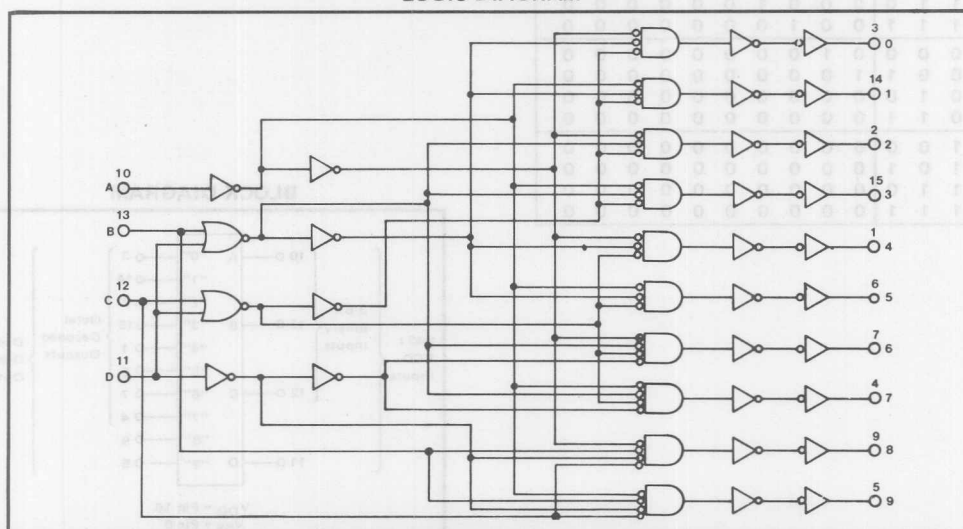


Typical P-Channel
Source Current Characteristics



Typical N-Channel
Sink Current Characteristics

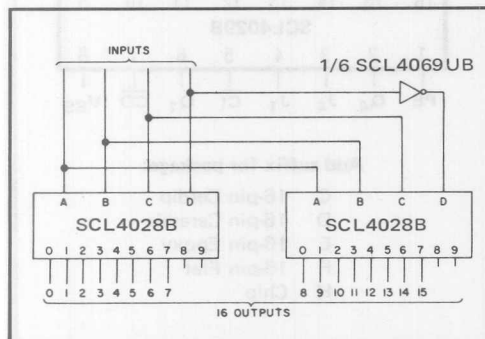
LOGIC DIAGRAM



APPLICATIONS INFORMATION

CODE CONVERSION CIRCUIT

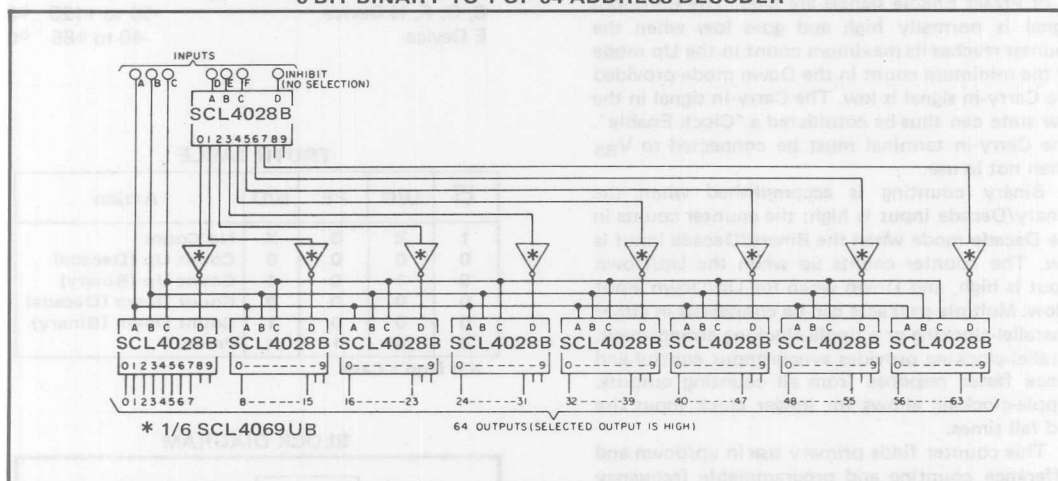
The circuit shown here converts any 4-bit code to a decimal or hexadecimal code. The table shows a number of codes and the decimal or hexadecimal number in these codes which must be applied to the input terminals of the SCL4028B to select a particular output. For example: in order to get a "high" on output No. 8 the input must be either an 8 expressed in 4-Bit Binary code, a 15 expressed in 4-Bit Gray code, or a 5 expressed in Excess-3 code.



INPUTS				INPUT CODES						OUTPUT NUMBER															
				Hexa Decimal			Decimal																		
				4BIT GRAY	4BIT GRAY	EXCESS-3 GRAY	EXCESS-3 GRAY	AIKEN	4:2:1																
D	C	B	A	4BIT GRAY	4BIT GRAY	EXCESS-3 GRAY	EXCESS-3 GRAY	AIKEN	4:2:1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	2	3	0	2	2	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	3	2	0	3	3	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	4	7	1	4	4	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	1	5	6	2	5	5	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
0	1	1	0	6	4	3	1	4	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
0	1	1	1	7	5	4	2	5	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
1	0	0	0	8	15	5			0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
1	0	0	1	9	14	6			5	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
1	0	1	0	10	12	7	9		6	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
1	0	1	1	11	13	8	5		7	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
1	1	0	0	12	8	9	5	6		0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
1	1	0	1	13	9	6	7	7		0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
1	1	1	0	14	11	8	8	8		0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
1	1	1	1	15	10	7	9	9		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Code Conversion Chart

6-BIT BINARY TO 1-OF-64 ADDRESS DECODER





CMOS PRESETTABLE UP/DOWN COUNTER

FEATURES

- ◆ Binary or Decade Up/Down Counting
- ◆ BCD Outputs in Decade Mode
- ◆ Asynchronous Preset Enable
- ◆ Internally Synchronous for High Speed
- ◆ Logic Edge-Clocked Design
- ◆ 6MHz Counting Rate @ 10Vdc
- ◆ Carry Output for Cascading Stages

DESCRIPTION

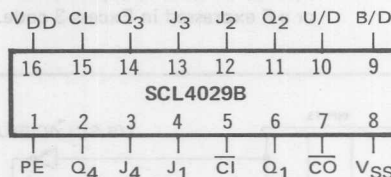
The SCL4029B consists of a four-stage Binary or BCD Decade Up/Down Counter with provisions for look-ahead carry in both counting modes. The inputs consist of a single Clock, Carry-in (Clock Enable), Binary/Decade, Up/Down, Preset Enable, and four individual Jam signals. Four separate buffered Q signals and a Carry-out signal are provided as outputs.

A high Preset Enable signal allows information on the Jam inputs to preset the counter to any state asynchronously with the Clock. A low on each Jam line, when the Preset/Enable signal is high, resets the counter to its zero count. The counter is advanced one count at the positive transition of the Clock when the Carry-in and Preset Enable signals are low. Advancement is inhibited when the Carry-in or Preset Enable signals are high. The Carry-out signal is normally high and goes low when the counter reaches its maximum count in the Up mode or the minimum count in the Down mode provided the Carry-in signal is low. The Carry-in signal in the low state can thus be considered a "Clock Enable". The Carry-in terminal must be connected to V_{SS} when not in use.

Binary counting is accomplished when the Binary/Decade input is high; the counter counts in the Decade mode when the Binary/Decade input is low. The counter counts up when the Up/Down input is high, and Down when the Up/Down input is low. Multiple packages can be connected in either a parallel-clocking or a ripple-clocking arrangement. Parallel-clocking provides synchronous control and hence faster response from all counting outputs. Ripple-clocking allows for longer clock input rise and fall times.

This counter finds primary use in up/down and difference counting and programmable frequency synthesizer applications. It is also useful in A/D and D/A conversion techniques and for magnitude and sign generation.

CONNECTION DIAGRAM (all packages)



Add suffix for package:

- C 16-pin Cerdip
- D 16-pin Ceramic
- E 16-pin Epoxy
- F 16-pin Flat
- H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

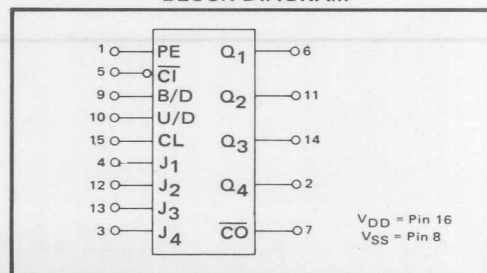
DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

TRUTH TABLE

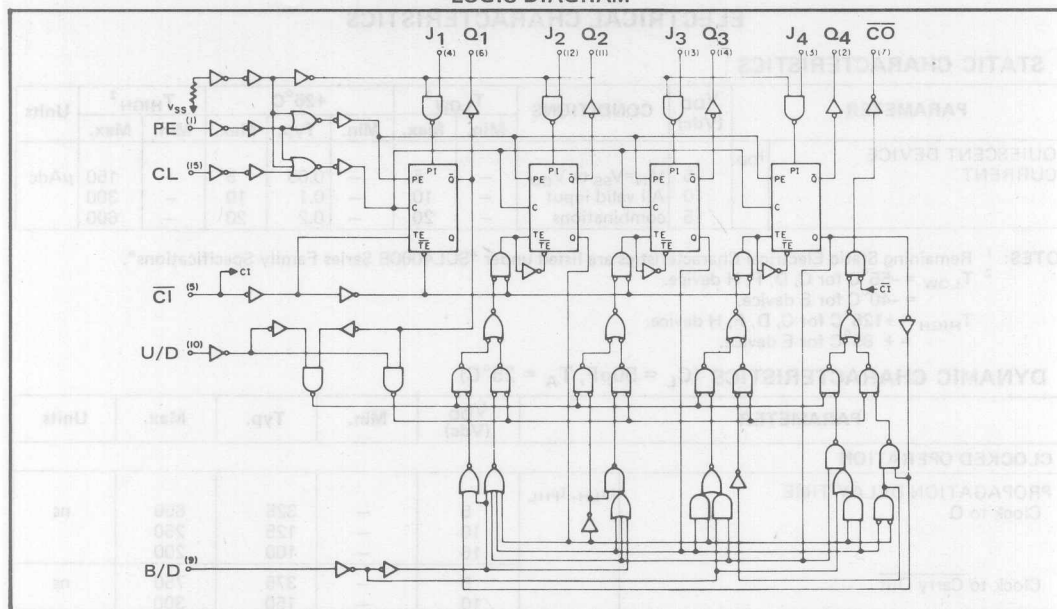
$\overline{CI}$	U/D	PE	B/D	Action
1	X	0	X	No Count
0	0	0	0	Count Up (Decade)
0	1	0	1	Count Up (Binary)
0	0	0	0	Count Down (Decade)
0	0	0	1	Count Down (Binary)
X	X	1	X	Preset

X = Don't Care

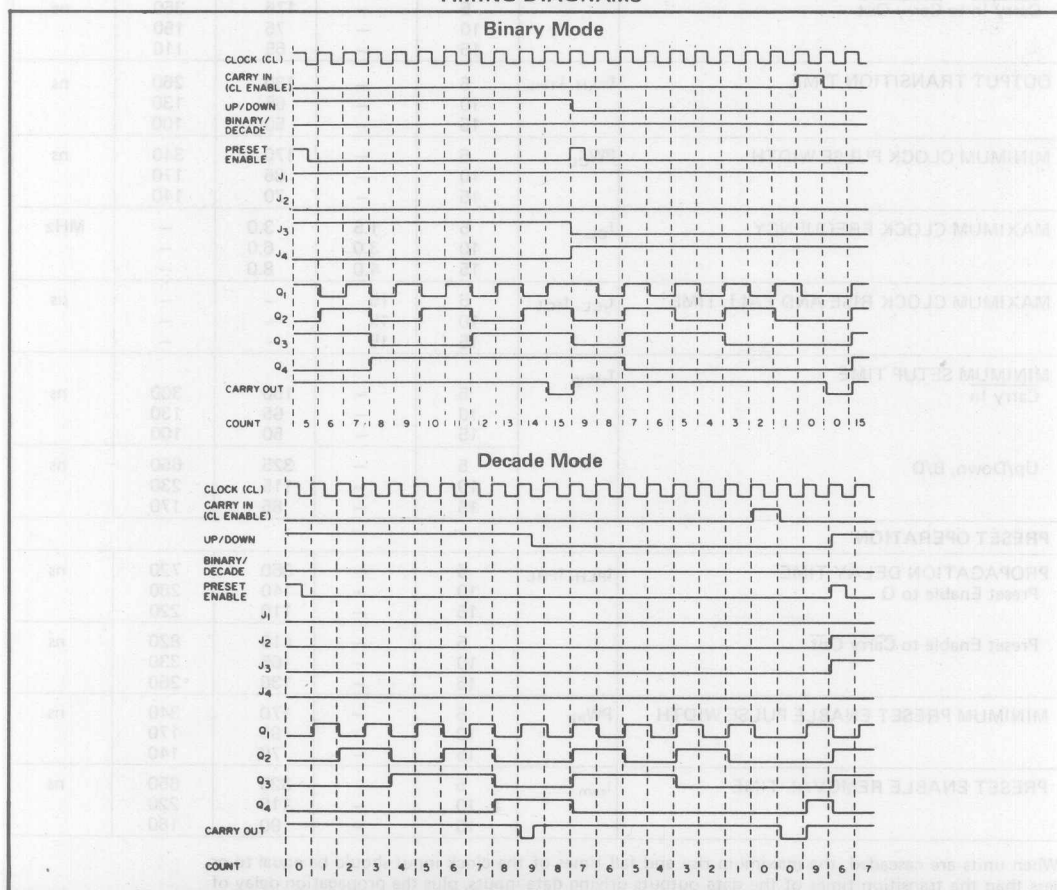
BLOCK DIAGRAM



LOGIC DIAGRAM



TIMING DIAGRAMS



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS¹

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	5	—	5	—	0.05	5	—	150	μAdc
		10	—	10	—	0.1	10	—	300	
		15	—	20	—	0.2	20	—	600	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

² T_{LOW} = -55°C for C, D, F, H device.

= -40°C for E device.

T_{HIGH} = +125°C for C, D, F, H device.

= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V _{DD} (V _{dc})	Min.	Typ.	Max.	Units		
CLOCKED OPERATION								
PROPAGATION DELAY TIME Clock to Q Clock to $\overline{\text{Carry Out}}$ $\overline{\text{Carry In}}$ to $\overline{\text{Carry Out}}$	$t_{\text{PLH}}, t_{\text{PHL}}$	5	—	325	650	ns		
		10	—	125	250			
		15	—	100	200			
		5	—	375	750	ns		
		10	—	150	300			
		15	—	120	240			
		5	—	175	350	ns		
		10	—	75	150			
		15	—	55	110			
OUTPUT TRANSITION TIME	$t_{\text{TLH}}, t_{\text{THL}}$	5	—	130	260	ns		
		10	—	65	130			
		15	—	50	100			
MINIMUM CLOCK PULSE WIDTH	PW_{CL}	5	—	170	340	ns		
		10	—	85	170			
		15	—	70	140			
MAXIMUM CLOCK FREQUENCY	f_{CL}	5	1.5	3.0	—	MHz		
		10	3.0	6.0	—			
		15	4.0	8.0	—			
MAXIMUM CLOCK RISE AND FALL TIME ¹	$t_{\text{rCL}}, t_{\text{fCL}}$	5	15	—	—	μs		
		10	15	—	—			
		15	15	—	—			
MINIMUM SETUP TIME Carry In Up/Down, B/D	t_{setup}	5	—	150	300	ns		
		10	—	65	130			
		15	—	50	100			
		5	—	325	650	ns		
		10	—	115	230			
		15	—	85	170			
		PRESET OPERATION						
		PROPAGATION DELAY TIME Preset Enable to Q Preset Enable to $\overline{\text{Carry Out}}$	$t_{\text{PLH}}, t_{\text{PHL}}$	5	—	360	720	ns
				10	—	140	280	
15	—			110	220			
5	—			410	820	ns		
10	—			165	330			
15	—			130	260			
MINIMUM PRESET ENABLE PULSE WIDTH	PW_{PE}			5	—	170	340	ns
				10	—	85	170	
				15	—	70	140	
PRESET ENABLE REMOVAL TIME	t_{rem}	5	—	325	650	ns		
		10	—	110	220			
		15	—	90	180			

¹ When units are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the transition times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitive load.

V_{D_S} (V)	I_{D_S} (mA) at $V_{G_S} = 15$ Vdc	I_{D_S} (mA) at $V_{G_S} = 10$ Vdc	I_{D_S} (mA) at $V_{G_S} = 5$ Vdc
0	0	0	0
2	10	4	2
4	16	6	3
6	20	7.5	3.5
8	21.5	8	3.8
10	22	8	4
12	22	8	4
14	22	8	4
16	22	8	4
18	22	8	4
20	22	8	4

The diagram illustrates two methods of cascading three SCL4029B counters:

- PARALLEL CLOCKING:** All three counters share a common clock signal. The clock input (CL) of each counter is connected to the common clock line. The carry-out (C.O.) of one counter is connected to the carry-in (C.I.) of the next counter. The up/down control (U/D) is connected to the UP/DOWN input, and the preset enable is connected to the PRESET ENABLE input.
- RIPPLE CLOCKING:** The clock signal is applied to the clock input (CL) of the first counter. The carry-out (C.O.) of the first counter is connected to the clock input (CL) of the second counter, and the carry-out (C.O.) of the second counter is connected to the clock input (CL) of the third counter. The up/down control (U/D) is connected to the UP/DOWN input, and the preset enable is connected to the PRESET ENABLE input.

Each SCL4029B counter has the following pins:

- U/D: Up/Down control
- PE: Preset Enable
- J₁, J₂, J₃, J₄: Preset inputs
- C.I.: Carry In
- C.O.: Carry Out
- B/D: Binary/Decade control
- CL: Clock
- Q₁, Q₂, Q₃, Q₄: Data outputs

The Up/Down control can be changed at any count. The only restriction on changing the Up/Down control is that the clock input to the first counting stage must be "high".

The diagram illustrates a BCD-to-binary converter using two SCL4029B counters. The first counter (L.S.D.) is configured as a BCD counter with its output Q4 (PE) connected to the clock of the second counter (M.S.D.). The second counter's output Q4 (PE) is connected to the clock of the first counter. The output of the first counter is f_{out} . The output of the second counter is f_{in}/n . The output of the first counter is f_{out} . The output of the second counter is f_{in}/n . The output of the first counter is f_{out} . The output of the second counter is f_{in}/n .

FEATURES

- ◆ Buffered Outputs
- ◆ Diode Protection on all Inputs
- ◆ Fully "B"-Series Compatible
- ◆ Balanced Output Drive Current Specifications
- ◆ Pin Compatible with 4070 types, MC14507, 74C86

DESCRIPTION

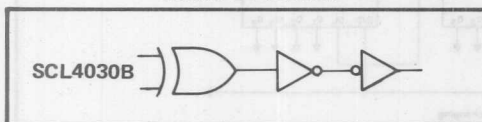
The SCL4030B contains four independent exclusive-OR gates integrated on a single monolithic silicon chip. Each exclusive-OR gate consists of five N-Channel and five P-Channel enhancement-mode transistors, plus output buffering devices.

TRUTH TABLE
(one of four gates)

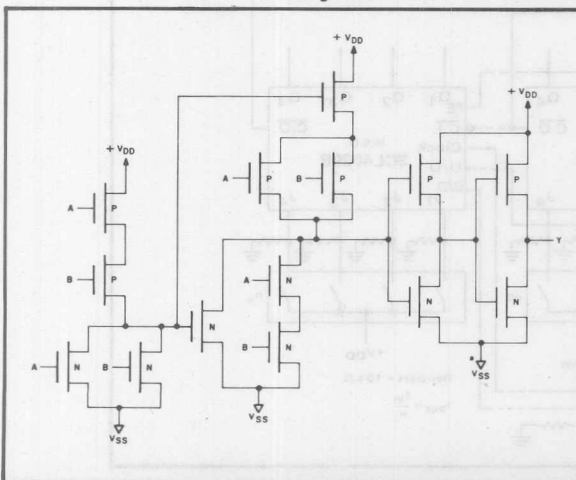
A	B	Y
0	0	0
1	0	1
0	1	1
1	1	0

Where 1 = High Level
0 = Low Level

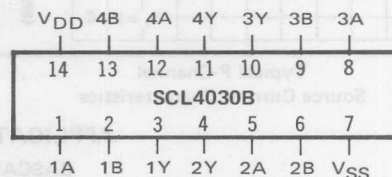
LOGIC DIAGRAM



SCHEMATIC DIAGRAM
(one of four gates)



CONNECTION DIAGRAM
(all packages)



Add suffix for package:

- C 14-pin Cerdip
- D 14-pin Ceramic
- E 14-pin Epoxy
- F 14-pin Flat
- H Chip

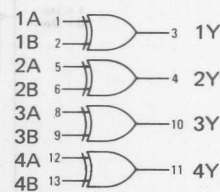
RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A	-55 to +125	°C
C, D, F, H Device		-40 to +85	°C
E Device			

Note: The SCL4030B is identical to the SCL4070B; the devices are fully interchangeable in all applications.

FUNCTION DIAGRAM



$$Y = A \oplus B$$

V_{DD} = Pin 14
 V_{SS} = Pin 7

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS^{1,3}

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	5	—	0.05	—	0.0005	0.05	—	1.5	μAdc
		10	—	0.10	—	0.001	0.10	—	3.0	
		15	—	0.20	—	0.002	0.20	—	6.0	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

² T_{LOW} = -55°C for C, D, F, H device.

= -40°C for E device.

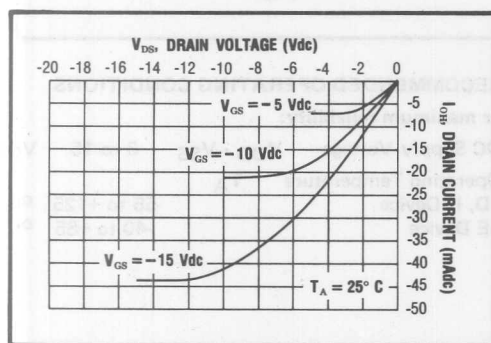
T_{HIGH} = +125°C for C, D, F, H device.

= + 85°C for E device.

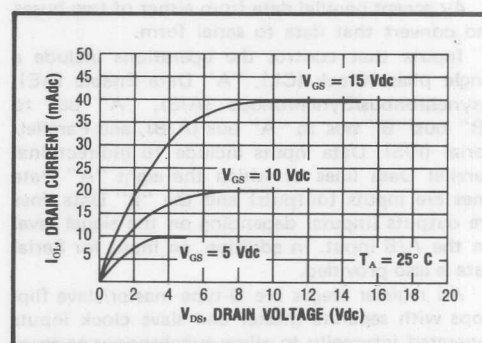
³ This device has been designed for balanced output drive current specifications. Consult Family Specifications.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

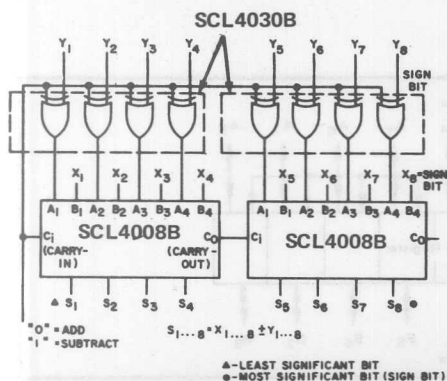
PARAMETER		V _{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME	t _{PLH} , t _{PHL}	5	—	175	350	ns
		10	—	70	140	
		15	—	50	100	
OUTPUT TRANSITION TIME	t _{TLH} , t _{THL}	5	—	100	200	ns
		10	—	50	100	
		15	—	40	80	



Typical P-Channel
Source Current Characteristics



Typical N-Channel
Sink Current Characteristics

APPLICATIONS INFORMATION
8-BIT TWO'S COMPLEMENT ADDER/SUBTRACTOR

X ₈	X ₇	X ₆	X ₅	X ₄	X ₃	X ₂	X ₁	X ₈	X ₇	X ₆	X ₅	X ₄	X ₃	X ₂	X ₁
0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0
0	0	0	0	0	0	1	0	1	1	1	1	1	1	0	1
0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0
0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	1
0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	1
0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1

Two's complement numbers and their equivalent decimal values.



CMOS 8-BIT UNIVERSAL BUS REGISTER

FEATURES

- ◆ Bidirectional Parallel Data Inputs
- ◆ Parallel or Serial Inputs/Parallel Outputs
- ◆ Asynchronous or Synchronous Parallel Data Loading
- ◆ Data Recirculation for Register Storage
- ◆ Parallel Enable on Data Lines for Bus Connection
- ◆ Static Operation - DC to 5MHz @ 10Vdc

DESCRIPTION

The SCL4034AB is a Static Eight-Stage Parallel - or Serial-Input/Parallel-Output Register. It can be used to:

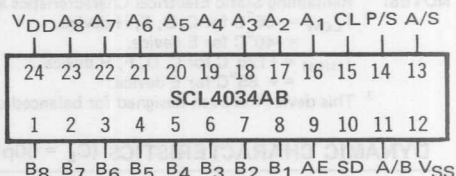
1. bidirectionally transfer parallel information between two buses,
2. convert serial data to parallel form and direct the parallel data to either of two buses,
3. store (recirculate) parallel data, or
4. accept parallel data from either of two buses and convert that data to serial form.

Inputs that control the operations include a single phase Clock (CL), "A" Data Enable (AE), Asynchronous/Synchronous (A/S), "A" bus to "B" bus/"B" bus to "A" bus (A/B), and Parallel/Serial (P/S). Data inputs include 16 bidirectional Parallel Data lines of which the eight "A" Data lines are inputs (outputs) and the "B" Data lines are outputs (inputs) depending on the signal level on the A/B input. In addition, an input for Serial data is also provided.

All register stages are D-type master/slave flip-flops with separate master and slave clock inputs generated internally to allow synchronous or asynchronous data transfer from master to slave. Isolation from external noise and the effects of loading is provided by output buffering.

Useful applications for this device include pseudo-random code generation, sample-and-hold register, frequency and phase comparators, address or buffer register, and serial/parallel input/output conversion.

CONNECTION DIAGRAM (all packages)



Add suffix for package:

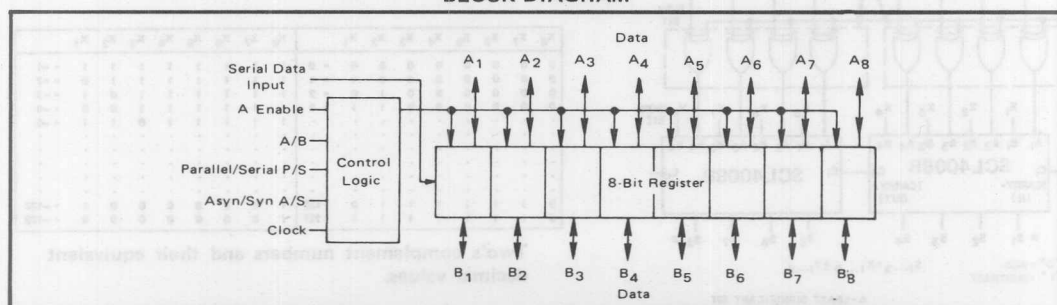
- D 24-pin Ceramic
- E 24-pin Epoxy
- H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
D, H Device		-55 to +125	°C
E Device		-40 to +85	°C

BLOCK DIAGRAM



OPERATING INFORMATION

The SCL4034AB is composed of eight register cells connected in cascade with additional control logic. Each register cell is composed of one "D" master-slave flip-flop with separate internal clocks, and two data transfer gates allowing the data to be transferred bidirectionally from bus A to bus B and from bus B to bus A, and to be memorized. Besides the single phase clock and the serial data inputs, the control logic provides four other features:

A Enable Input — When high, this input enables the bus A data lines.

A/B Input (Data A or B) — This input controls the direction of data flow: when high, the data

flows from bus A to bus B; when low, the data flows from bus B to bus A.

P/S Input (Parallel/Serail) — This input controls the data input mode (Parallel or Serial). When high, the data is transferred to the register in a parallel asynchronous mode or a parallel synchronous mode (positive clock transition). When low, the data is entered into the register in a serial synchronous mode (positive clock transition).

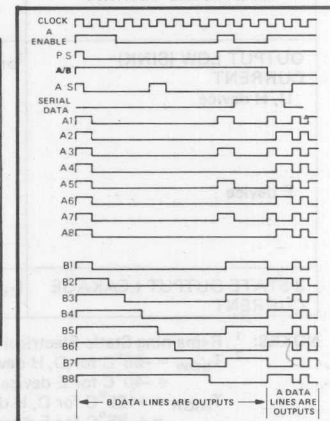
A/S Input (Asynchronous/Synchronous to the Clock) — When this input is high, the data is transferred independently from the clock rate; when low, the clock is enabled and the data is transferred synchronously.

Truth Table for Register Input-Levels and the Resulting Operation
(L = Low Level, H = High, X = Don't Care)

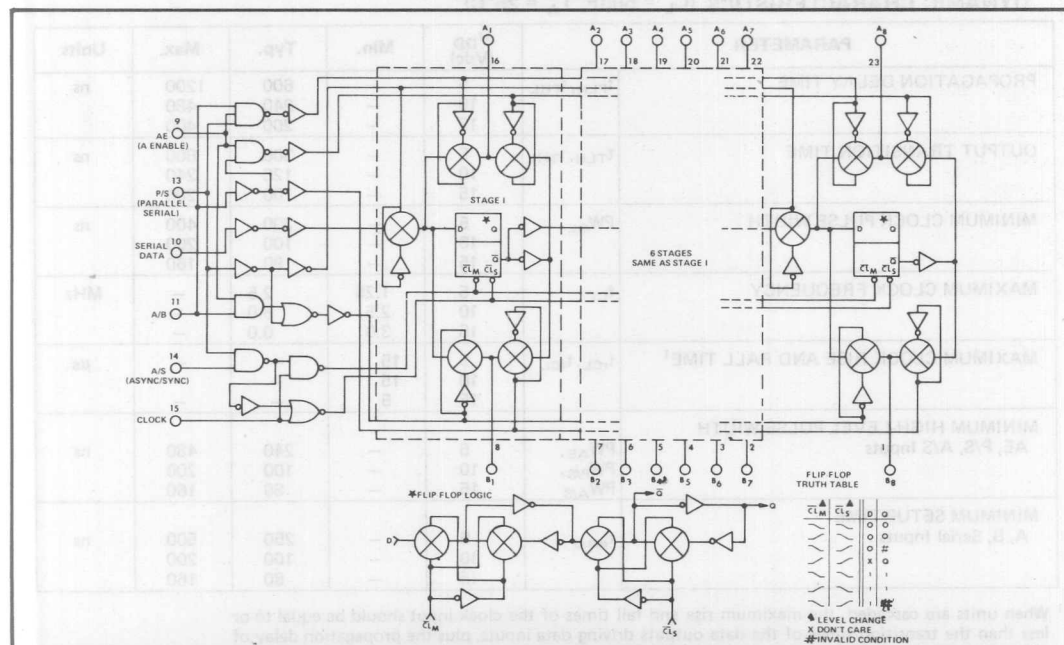
"A" Enable	P/S	A/B	A/S	Operation*
L	L	L	X	Serial Mode; Synch. Serial Data Input, "A" Parallel Data Outputs Disabled
L	L	H	X	Serial Mode; Synch. Serial Data Input, "B" Parallel Data Output
L	H	L	L	Parallel Mode; "B" Synch. Parallel Data Inputs, "A" Parallel Data Outputs Disabled
L	H	L	H	Parallel Mode; "B" Asynch. Parallel Data Inputs, "A" Parallel Data Outputs Disabled
L	H	H	L	Parallel Mode; "A" Parallel Data Inputs Disabled, "B" Parallel Data Outputs, Synch Data Recirculation
L	H	H	H	Parallel Mode; "A" Parallel Data Inputs Disabled, "B" Parallel Data Outputs, Asynch Data Recirculation
H	L	L	X	Serial Mode; Synch. Serial Data Input, "A" Parallel Data Output
H	L	H	X	Serial Mode; Synch. Serial Data Input, "B" Parallel Data Output
H	H	L	L	Parallel Mode; "B" Synch. Parallel Data Input, "A" Parallel Data Output
H	H	L	H	Parallel Mode; "B" Asynch. Parallel Data Input, "A" Parallel Data Output
H	H	H	L	Parallel Mode; "A" Synch. Parallel Data Input, "B" Parallel Data Output
H	H	H	H	Parallel Mode; "A" Asynch. Parallel Data Input, "B" Parallel Data Output

* Outputs change at positive transition of clock in the serial mode and when the A/S control input is "low" in the parallel mode.

TIMING DIAGRAM



LOGIC DIAGRAM



PARAMETER	V _{DD} (V _{dc})	CONDITIONS	T _{LOW} ¹		+25 °C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	5 V _{IN} =V _{SS} or V _{DD}	—	5	—	0.05	5	—	150	μAdc
		10 All valid inputs combinations	—	10	—	0.1	10	—	300	
		15	—	20	—	0.2	20	—	600	
OUTPUT HIGH (SOURCE) CURRENT D, H device	I _{OH}	5 V _{OH} =4.6V	-0.05	—	-0.04	-0.08	—	-0.028	—	mAdc
		10 V _{OH} =9.5V	-0.16	—	-0.125	-0.25	—	-0.88	—	
		15 V _{OH} =13.5V	-0.5	—	-0.4	-1.0	—	-0.28	—	
		V _{IN} =V _{SS} or V _{DD}								
		5 V _{OH} =4.6V	-0.048	—	-0.04	-0.08	—	-0.032	—	
		10 V _{OH} =9.5V	-0.15	—	-0.125	-0.25	—	-0.10	—	
E device		15 V _{OH} =13.5V	-0.48	—	-0.4	-1.0	—	-0.32	—	mAdc
		V _{IN} =V _{SS} or V _{DD}								
OUTPUT LOW (SINK) CURRENT D, H device	I _{OL}	5 V _{OL} =0.4V	0.125	—	0.1	0.2	—	0.07	—	mAdc
		10 V _{OL} =0.5V	0.31	—	0.25	0.5	—	0.175	—	
		15 V _{OL} =1.5V	1.44	—	1.15	2.5	—	0.81	—	
		V _{IN} =V _{SS} or V _{DD}								
		5 V _{OL} =0.4V	0.125	—	0.1	0.2	—	0.08	—	
		10 V _{OL} =0.5V	0.30	—	0.25	0.5	—	0.20	—	
E device		15 V _{OL} =1.5V	1.37	—	1.15	2.5	—	0.93	—	mAdc
		V _{IN} =V _{SS} or V _{DD}								
3-STATE OUTPUT LEAKAGE CURRENT	I _{ZL}	15	—	±0.1	—	±10 ⁻⁴	±0.1	—	±1.0	μAdc

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

² T_{LOW} = -55°C for D, H device.

= -40°C for E device.

T_{HIGH} = +125°C for D, H device.

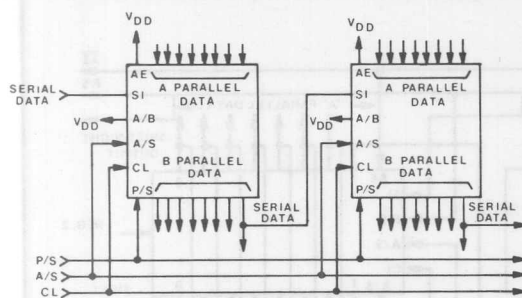
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

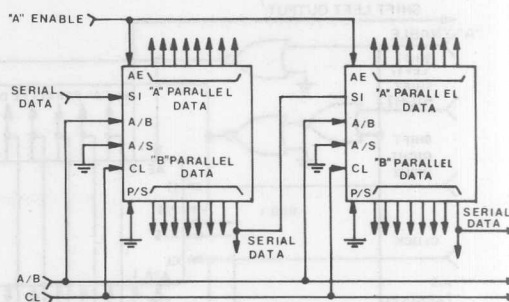
PARAMETER		V _{DD} (V _{dc})	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME	t _{PLH} , t _{PHL}	5	—	600	1200	ns
		10	—	240	480	
		15	—	200	400	
OUTPUT TRANSITION TIME	t _{TLH} , t _{THL}	5	—	300	600	ns
		10	—	120	240	
		15	—	100	200	
MINIMUM CLOCK PULSE WIDTH	PW _{CL}	5	—	200	400	ns
		10	—	100	200	
		15	—	80	160	
MAXIMUM CLOCK FREQUENCY	f _{CL}	5	1.25	2.5	—	MHz
		10	2.5	5.0	—	
		15	3.0	6.0	—	
MAXIMUM CLOCK RISE AND FALL TIME ¹	t _{rCL} , t _{fCL}	5	15	—	—	μs
		10	15	—	—	
		15	5	—	—	
MINIMUM HIGH-LEVEL PULSE WIDTH AE, P/S, A/S Inputs	PW _{AE} , PW _{P/S} , PW _{A/S}	5	—	240	480	ns
		10	—	100	200	
		15	—	80	160	
MINIMUM SETUP TIME A, B, Serial Inputs	t _{setup}	5	—	250	500	ns
		10	—	100	200	
		15	—	80	160	

¹ When units are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the transition times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitive load.

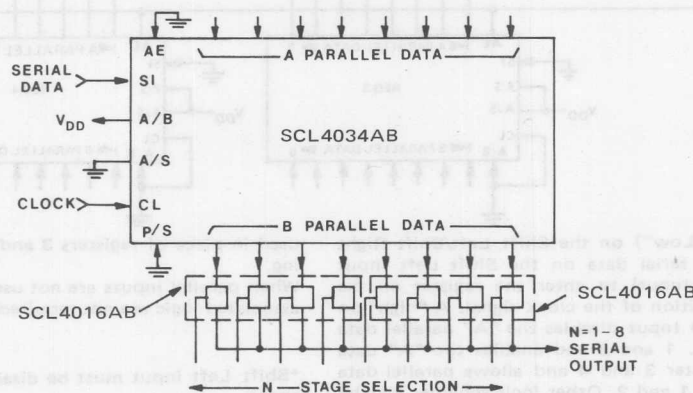
APPLICATIONS INFORMATION



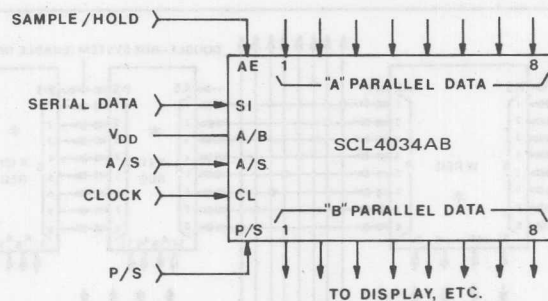
16-Bit parallel in/parallel out, parallel in/serial out, serial in/parallel out, serial in/serial out register.



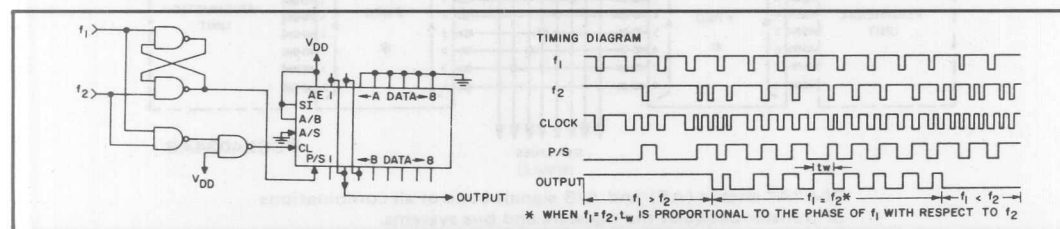
16-Bit Serial in/gated parallel out register



N-stage shift register with fixed serial output line.

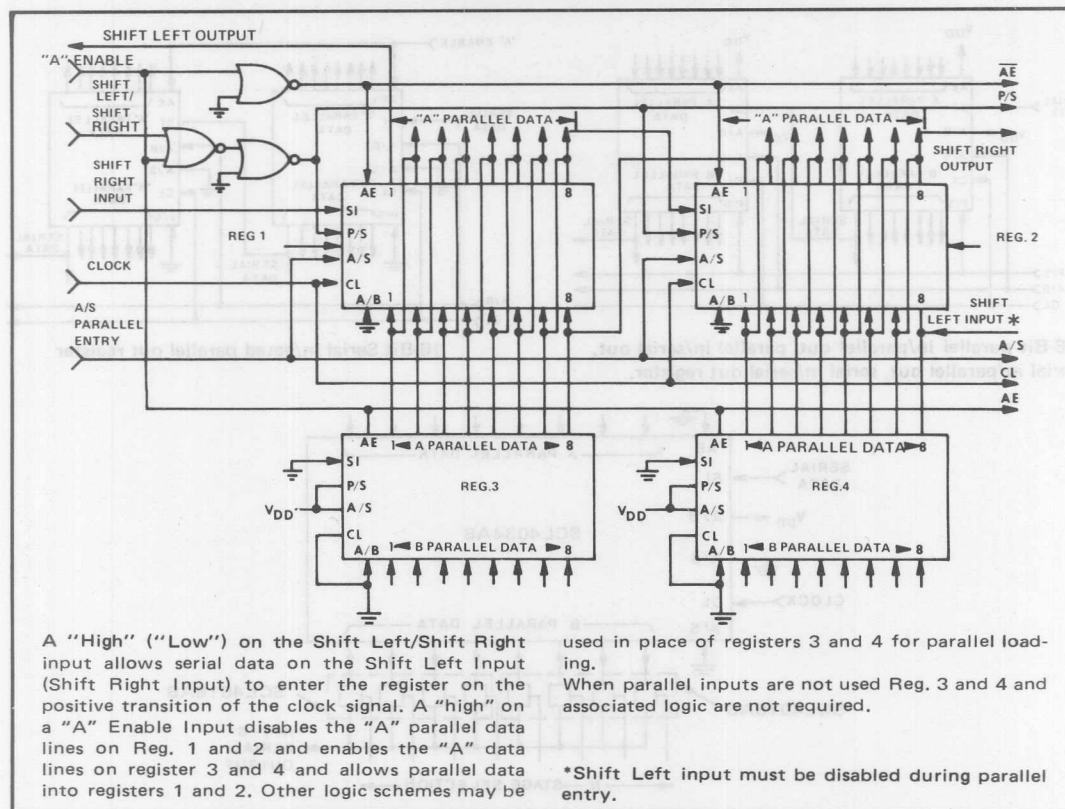


Sample and hold register — serial/parallel in parallel out.

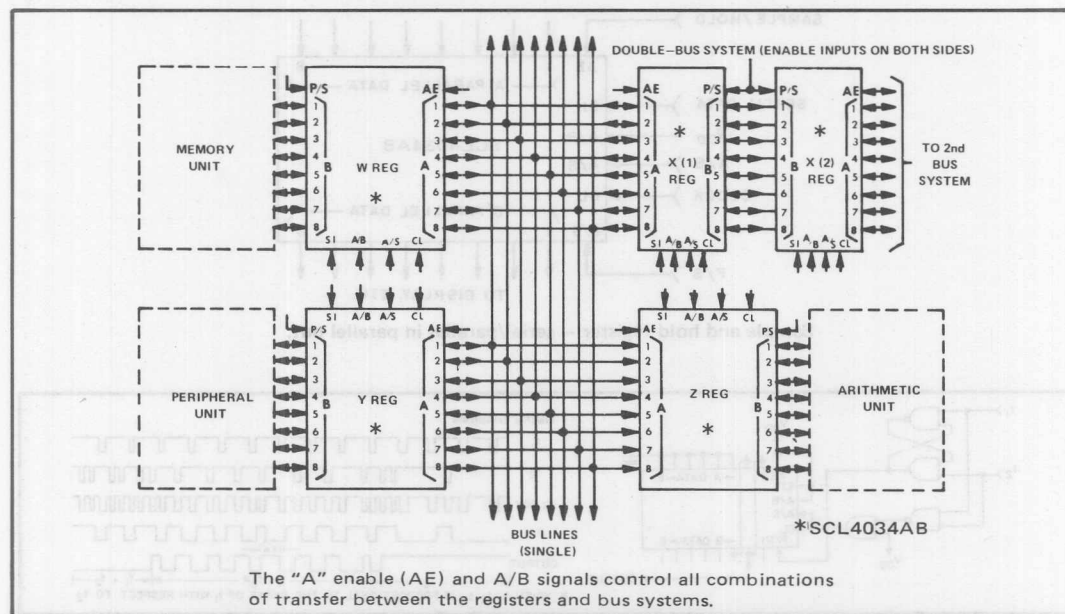


Frequency and phase comparator

APPLICATIONS INFORMATION (Continued)



Shift right/shift left with parallel inputs



Single and double-bus systems



CMOS 4-BIT PARALLEL-IN/ PARALLEL-OUT SHIFT REGISTER

FEATURES

- ◆ 4-Stage Clocked Serial-Shift Operation
- ◆ Synchronous Parallel Loading of All Stages
- ◆ J-K Serial Inputs to First Stage
- ◆ Asynchronous True/Complement Control of all Outputs
- ◆ Asynchronous Reset
- ◆ Static Operation — DC to 6MHz @ 10Vdc
- ◆ Balanced Output Drive Current Specifications

DESCRIPTION

The SCL4035B is a Four-Stage Clocked Serial Register having provisions for synchronous parallel inputs to each stage and serial inputs to the first stage via J-K logic. Register stages 2, 3, and 4 are coupled in a serial "D" flip-flop configuration when the register is in the serial mode (Parallel/Serial control low).

Parallel entry via the "D" line of each register stage is permitted only when the Parallel/Serial control is high. In the parallel or serial mode information is transferred on positive Clock transitions.

When the True/Complement control is high, the true contents of the register are available at the output terminals. When the True/Complement control is low, the outputs are the complements of the data in the register. The True/Complement control functions asynchronously with respect to the Clock signal.

J-K input logic is provided on the first stage serial input to minimize logic requirements, particularly in counting and sequence-generation applications. With J-K inputs connected together, the first stage becomes a "D" flip-flop. An asynchronous common Reset is also provided.

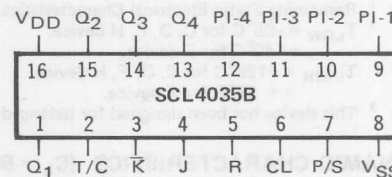
This device may be used for shift-right/shift-left registers, parallel-to-serial/serial-to-parallel conversion, sequence generation, up/down Johnson or ring counters, pseudo-random code generation, frequency and phase comparators, and sample-and-hold registers.

TRUTH TABLE

CL	t_{n-1} (Inputs)				t_n (Outputs)
	J	$\bar{K}$	R	Q_{n-1}	Q_n
	0	X	0	0	0
	1	X	0	0	1
	X	0	0	1	0
	1	0	0	Q_{n-1}	$\bar{Q}_{n-1}$ Toggle Mode
	X	1	0	1	1
	X	X	0	Q_{n-1}	Q_{n-1}
X	X	X	1	X	0

X = Don't Care

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

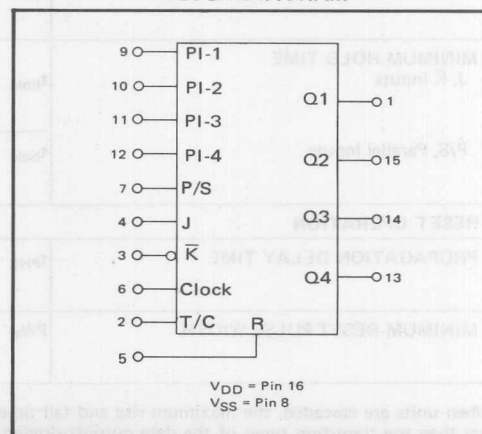
- C 16-pin Cerdip
- D 16-pin Ceramic
- E 16-pin Epoxy
- F 16-pin Flat
- H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS^{1, 3}

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	5	—	5	—	0.05	5	—	150	μAdc
		10	—	10	—	0.1	10	—	300	
		15	—	20	—	0.2	20	—	600	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

² T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.

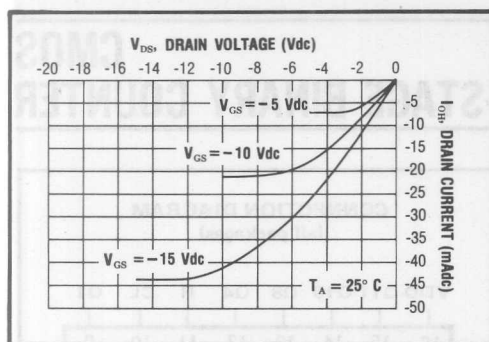
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

³ This device has been designed for balanced output drive current specifications. Consult Family Specifications.

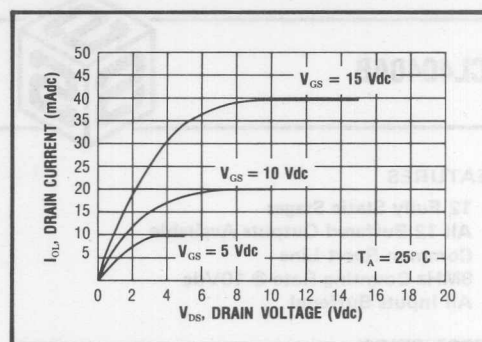
DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V _{DD} (V _{Dc})	Min.	Typ.	Max.	Units	
CLOCKED OPERATION							
PROPAGATION DELAY TIME From Clock Input	t _{PLH} , t _{PHL}	5	—	300	600	ns	
		10	—	125	250		
		15	—	95	190		
	From T/C Input	t _{PLH} , t _{PHL}	5	—	150	300	ns
		10	—	60	120		
		15	—	45	90		
OUTPUT TRANSITION TIME	t _{TLH} , t _{THL}	5	—	100	200	ns	
		10	—	50	100		
		15	—	40	80		
MINIMUM CLOCK PULSE WIDTH	PW _{CL}	5	—	165	330	ns	
		10	—	80	160		
		15	—	60	120		
MAXIMUM CLOCK FREQUENCY	f _{CL}	5	1.5	3.0	—	MHz	
		10	3.0	6.0	—		
		15	4.0	8.0	—		
MAXIMUM CLOCK RISE & FALL TIME ¹	t _{rCL} , t _{fCL}	5	15	—	—	μs	
		10	10	—	—		
		15	8	—	—		
MINIMUM SETUP TIME J, K Inputs	t _{setup}	5	—	250	500	ns	
		10	—	100	200		
		15	—	80	160		
	P/S, Parallel Inputs	t _{setup}	5	—	175	350	ns
		10	—	75	150		
		15	—	60	120		
MINIMUM HOLD TIME J, K inputs	t _{hold}	5	—	-25	25	ns	
		10	—	-10	10		
		15	—	- 5	5		
	P/S, Parallel Inputs	t _{hold}	5	—	-25	25	ns
		10	—	-10	10		
		15	—	- 5	5		
RESET OPERATION							
PROPAGATION DELAY TIME	t _{PHL}	5	—	300	600	ns	
		10	—	125	250		
		15	—	95	190		
MINIMUM RESET PULSE WIDTH	PW _R	5	—	200	400	ns	
		10	—	85	170		
		15	—	65	130		

¹ When units are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the transition times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitive load.

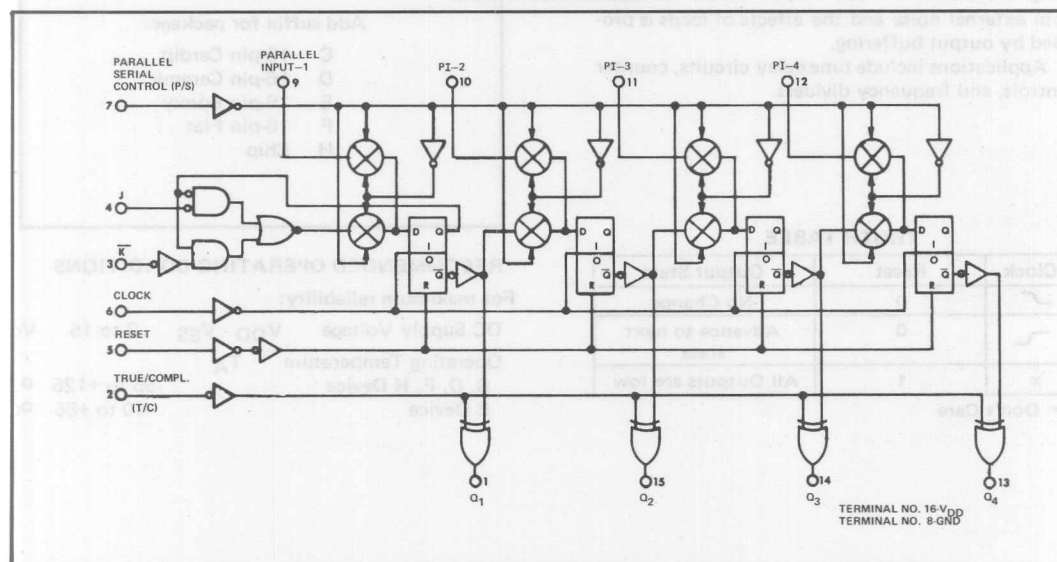


Typical P-Channel
Source Current Characteristics

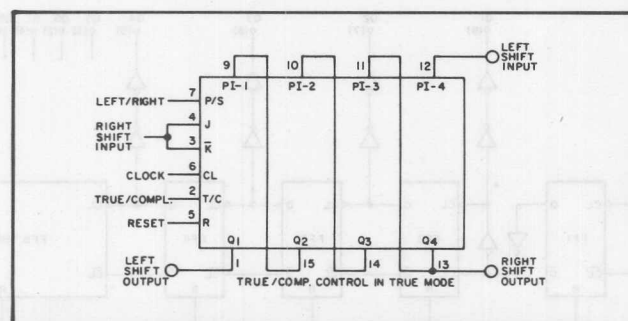


Typical N-Channel
Sink Current Characteristics

LOGIC DIAGRAM



APPLICATIONS INFORMATION



Shift Left/Shift Right Register



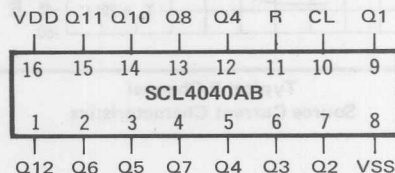
FEATURES

- ◆ 12 Fully Static Stages
- ◆ All 12 Buffered Outputs Available
- ◆ Common Reset Line
- ◆ 8MHz Counting Rate @ 10Vdc
- ◆ All Inputs Buffered

DESCRIPTION

The SCL4040AB consists of 12-ripple-carry binary counter stages with appropriate input buffers and reset circuitry. The counter is reset to its "all 0's" state by a high level on the Reset input. The counter is advanced one count on the negative-going transition of each input pulse. Isolation from external noise and the effects of loads is provided by output buffering.

Applications include time delay circuits, counter controls, and frequency dividers.

CONNECTION DIAGRAM
(all packages)

Add suffix for package:

- C 16-pin Cerdip
- D 16-pin Ceramic
- E 16-pin Epoxy
- F 16-pin Flat
- H Chip

TRUTH TABLE

Clock	Reset	Output State
	0	No Change
	0	Advance to next state
x	1	All Outputs are low

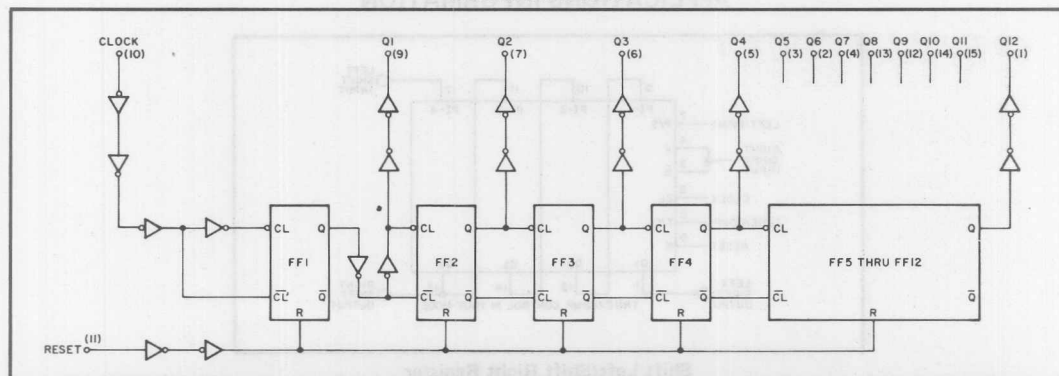
X = Don't Care

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A	-55 to +125	°C
C, D, F, H Device		-40 to +85	°C
E Device			

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS¹

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	5	—	5	—	0.05	5	—	150	μAdc
		10	—	10	—	0.1	10	—	300	
		15	—	15	—	0.2	20	—	600	
OUTPUT HIGH (SOURCE) CURRENT C, D, F, H device	I _{OH}	5	V _{OH} =4.6V	-0.15	—	-0.12	-0.5	—	-0.08	mAdc
		10	V _{OH} =9.5V	-0.37	—	-0.3	-1.15	—	-0.21	
		15	V _{OH} =13.5V V _{IN} =V _{SS} or V _{DD}	-1.25	—	-1.0	-4.5	—	-0.69	
E device	I _{OH}	5	V _{OH} =4.6V	-0.14	—	-0.12	-0.5	—	-0.10	mAdc
		10	V _{OH} =9.5V	-0.35	—	-0.3	-1.15	—	-0.25	
		15	V _{OH} =13.5V V _{IN} =V _{SS} or V _{DD}	-1.2	—	-1.0	-4.5	—	-0.85	
OUTPUT LOW (SINK) CURRENT C, D, F, H device	I _{OL}	5	V _{OL} =0.4V	0.15	—	0.12	0.5	—	0.08	mAdc
		10	V _{OL} =0.5V	0.37	—	0.3	1.0	—	0.21	
		15	V _{OL} =1.5V V _{IN} =V _{SS} or V _{DD}	1.25	—	1.0	5.8	—	0.69	
E device	I _{OL}	5	V _{OL} =0.4V	0.14	—	0.12	0.5	—	0.10	mAdc
		10	V _{OL} =0.5V	0.35	—	0.3	1.0	—	0.25	
		15	V _{OL} =1.5V V _{IN} =V _{SS} or V _{DD}	1.2	—	1.0	5.8	—	0.85	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

² T_{LOW} = -55°C for C, D, F, H device.

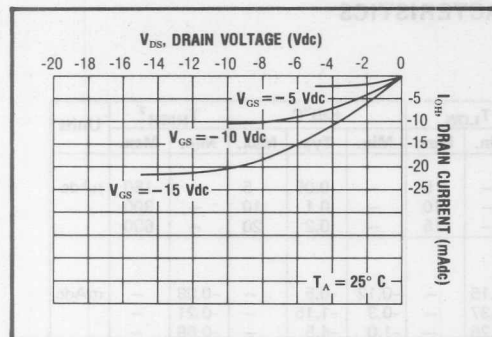
= -40°C for E device.

T_{HIGH} = +125°C for C, D, F, H device.

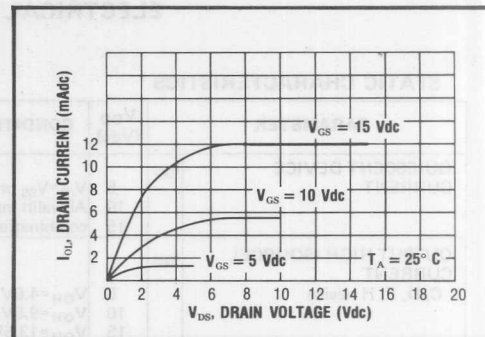
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V _{DD} (V _{Dc})	Min.	Typ.	Max.	Units
CLOCKED OPERATION						
PROPAGATION DELAY TIME Clock to Q1	t _{PLH} , t _{PHL}	5	—	200	400	ns
		10	—	100	200	
		15	—	80	160	
Q _i to Q _{i + 1}	t _{PLH} , t _{PHL}	5	—	150	300	ns
		10	—	75	150	
		15	—	60	120	
OUTPUT TRANSITION TIME	t _{TLH} , t _{THL}	5	—	180	360	ns
		10	—	90	180	
		15	—	65	130	
MINIMUM CLOCK PULSE WIDTH	PW _{CL}	5	—	100	200	ns
		10	—	50	100	
		15	—	40	80	
MAXIMUM CLOCK FREQUENCY	f _{CL}	5	2.0	4.0	—	MHz
		10	4.0	8.0	—	
		15	5.0	10.0	—	
MAXIMUM CLOCK RISE AND FALL TIME	t _{rCL} , t _{fCL}	5	15	—	—	μs
		10	15	—	—	
		15	5	—	—	
RESET OPERATION						
PROPAGATION DELAY TIME	t _{PHL}	5	—	300	600	ns
		10	—	150	300	
		15	—	120	240	
MINIMUM RESET PULSE WIDTH	PW _R	5	—	150	300	ns
		10	—	75	150	
		15	—	60	120	
RESET REMOVAL TIME	t _{rem}	5	—	250	500	ns
		10	—	125	250	
		15	—	100	200	

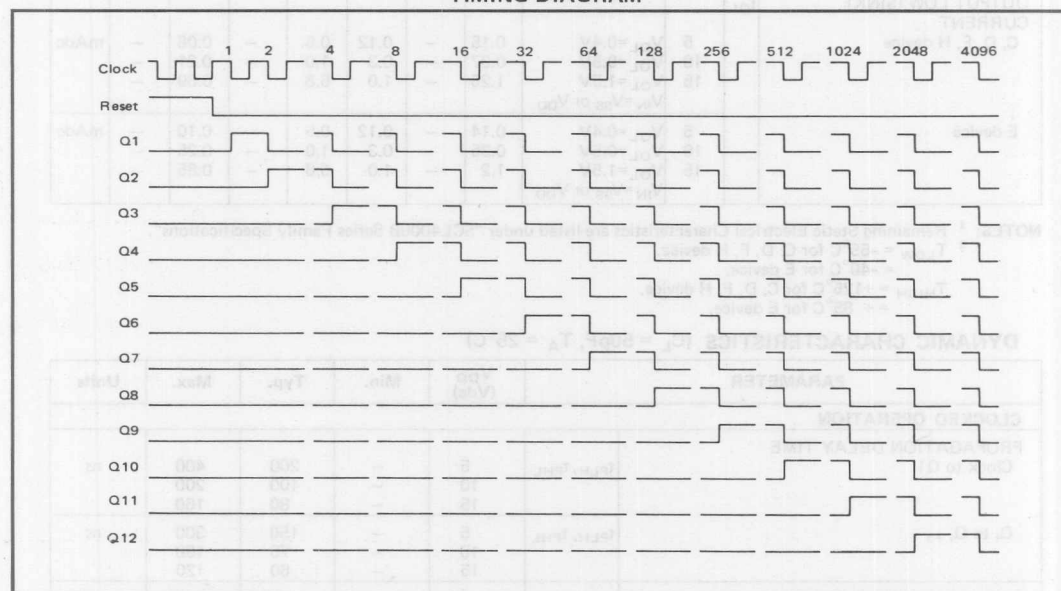


Typical P-Channel
Source Current Characteristics

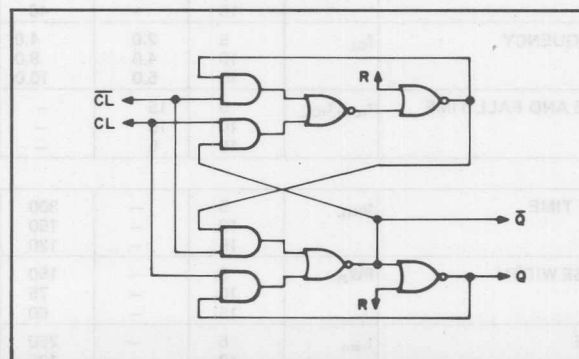


Typical N-Channel
Sink Current Characteristics

TIMING DIAGRAM



TYPICAL COUNTER STAGE





CMOS QUAD TRUE/COMPLEMENT BUFFER

FEATURES

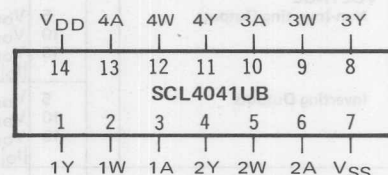
- ◆ Both True and Complement Outputs Available Simultaneously
- ◆ High Source and Sink Current
- ◆ Diode Protection on All Inputs

DESCRIPTION

The SCL4041UB Quad True/Complement Buffer is a monolithic integrated circuit constructed with P-Channel and N-Channel enhancement-mode devices. The outputs have low resistance and are capable of sinking or sourcing high currents for use in driver applications where high noise immunity and low power dissipation are required.

This device is useful as a line-driver, CMOS-to-TTL driver, low-power resistor-network driver for A/D and D/A conversion, display and clock drivers.

CONNECTION DIAGRAM (all packages)



Add suffix for package:

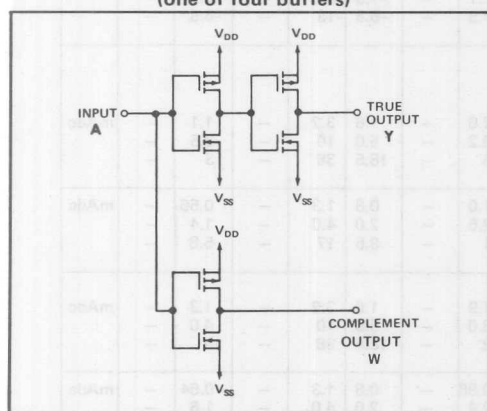
- C 14-pin Cerdip
- D 14-pin Ceramic
- E 14-pin Epoxy
- F 14-pin Flat
- H Chip

RECOMMENDED OPERATING CONDITIONS

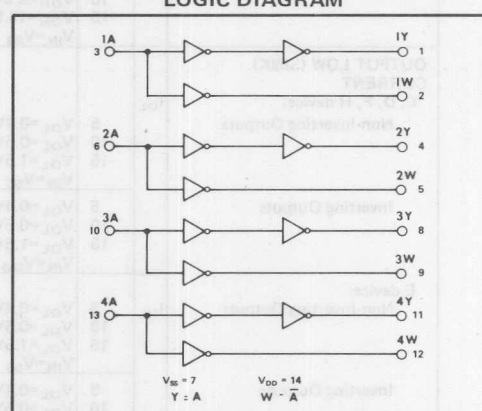
For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A	-55 to +125	°C
C, D, F, H Device		-40 to +85	°C
E Device			

SCHEMATIC DIAGRAM (one of four buffers)



LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS¹

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	5 V _{IN} =V _{SS} or V _{DD}	—	1.0	—	0.005	1.0	—	30	μAdc
		10 All valid input combinations	—	2.0	—	0.01	2.0	—	60	
		15	—	4.0	—	0.02	4.0	—	120	
MINIMUM INPUT HIGH VOLTAGE Non-Inverting Outputs	V _{IH}	5 V _{OH} =4.5V	—	3.5	—	2.75	3.5	—	3.5	Vdc
		10 V _{OH} =9.0V	—	7.0	—	5.5	7.0	—	7.0	
		15 V _{OH} =13.5V I _O ≤ 1μA	—	11.0	—	8.25	11.0	—	11.0	
		5 V _{OL} =0.5V	—	4.0	—	2.75	4.0	—	4.0	Vdc
		10 V _{OL} =1.0V	—	8.0	—	5.5	8.0	—	8.0	
		15 V _{OL} =1.5V I _O ≤ 1μA	—	12.0	—	8.25	12.0	—	12.0	
MAXIMUM INPUT LOW VOLTAGE Non-Inverting Outputs	V _{IL}	5 V _{OL} =0.5V	1.5	—	1.5	2.25	—	1.5	—	Vdc
		10 V _{OL} =1.0V	3.0	—	3.0	4.5	—	3.0	—	
		15 V _{OL} =1.5V I _O ≤ 1μA	4.0	—	4.0	6.75	—	4.0	—	
		5 V _{OH} =4.5V	1.0	—	1.0	2.25	—	1.0	—	Vdc
		10 V _{OH} =9.0V	2.0	—	2.0	4.5	—	2.0	—	
		15 V _{OH} =13.5V I _O ≤ 1μA	3.0	—	3.0	6.75	—	3.0	—	
OUTPUT HIGH (SOURCE) CURRENT C, D, F, H device: Non-Inverting Outputs	I _{OH}	5 V _{OH} =4.6V	-1.7	—	-1.4	-2.8	—	-1.0	—	mAdc
		10 V _{OH} =9.5V	-5.0	—	-4.0	-8.0	—	-2.8	—	
		15 V _{OH} =13.5V V _{IN} =V _{DD}	-16	—	-13	-26	—	-9	—	
		5 V _{OH} =4.6V	-0.75	—	-0.6	-1.0	—	-0.42	—	mAdc
		10 V _{OH} =9.5V	-2.2	—	-1.8	-3.6	—	-1.3	—	
		15 V _{OH} =13.5V V _{IN} =V _{SS}	-8.0	—	-6.5	-13	—	-4.5	—	
	I _{OH}	5 V _{OH} =4.6V	-1.6	—	-1.4	-2.8	—	-1.2	—	mAdc
		10 V _{OH} =9.5V	-4.8	—	-4.0	-8.0	—	-3.2	—	
		15 V _{OH} =13.5V V _{IN} =V _{DD}	-15	—	-13	-26	—	-11	—	
		5 V _{OH} =4.6V	-0.72	—	-0.6	-1.0	—	-0.48	—	mAdc
		10 V _{OH} =9.5V	-2.1	—	-1.8	-3.6	—	-1.5	—	
		15 V _{OH} =13.5V V _{IN} =V _{SS}	-7.5	—	-6.5	-13	—	-5.5	—	
OUTPUT LOW (SINK) CURRENT C, D, F, H device: Non-Inverting Outputs	I _{OL}	5 V _{OL} =0.4V	2.0	—	1.6	3.2	—	1.1	—	mAdc
		10 V _{OL} =0.5V	6.2	—	5.0	10	—	3.5	—	
		15 V _{OL} =1.5V V _{IN} =V _{SS}	23	—	18.5	38	—	13	—	
		5 V _{OL} =0.4V	1.0	—	0.8	1.3	—	0.56	—	mAdc
		10 V _{OL} =0.5V	2.5	—	2.0	4.0	—	1.4	—	
		15 V _{OL} =1.5V V _{IN} =V _{DD}	11	—	8.5	17	—	5.8	—	
	I _{OL}	5 V _{OL} =0.4V	1.9	—	1.6	3.2	—	1.3	—	mAdc
		10 V _{OL} =0.5V	6.0	—	5.0	10	—	4.0	—	
		15 V _{OL} =1.5V V _{IN} =V _{SS}	22	—	18.5	38	—	15	—	
		5 V _{OL} =0.4V	0.96	—	0.8	1.3	—	0.64	—	mAdc
		10 V _{OL} =0.5V	2.4	—	2.0	4.0	—	1.6	—	
		15 V _{OL} =1.5V V _{IN} =V _{DD}	10	—	8.5	17	—	7	—	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".² T_{LOW} = -55°C for C, D, F, H device.

= -40°C for E device.

T_{HIGH} = +125°C for C, D, F, H device.

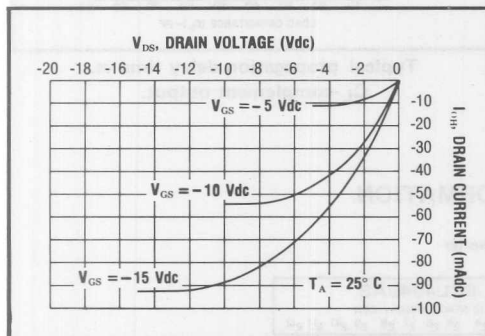
= + 85°C for E device.

ELECTRICAL CHARACTERISTICS (Continued)

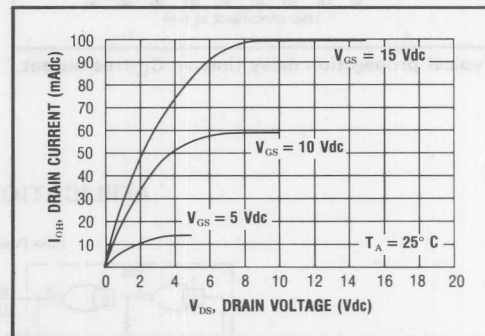
DYNAMIC CHARACTERISTICS ($C_L = 50\text{pF}$, $T_A = 25^\circ\text{C}$)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME Non-Inverting Outputs	t_{PLH} , t_{PHL}	5	—	90	180	ns
		10	—	55	110	
		15	—	45	90	
Inverting Outputs	t_{PLH} , t_{PHL}	5	—	90	180	ns
		10	—	45	90	
		15	—	35	70	
OUTPUT TRANSITION TIME Non-Inverting Outputs	t_{TLH} , t_{THL}	5	—	35	70	ns
		10	—	20	40	
		15	—	15	30	
Inverting Outputs	t_{TLH} , t_{THL}	5	—	40	80	ns
		10	—	23	45	
		15	—	16	32	
INPUT CAPACITANCE	C_{IN}	—	—	10	15	pF

NON-INVERTING (TRUE) OUTPUT

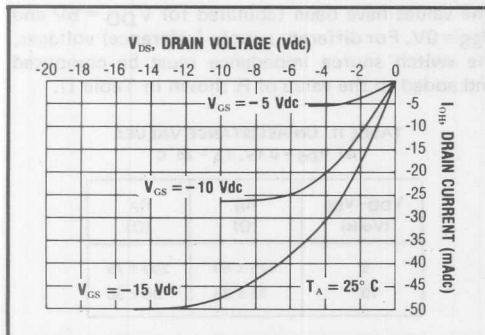


Typical P-Channel
Source Current Characteristics

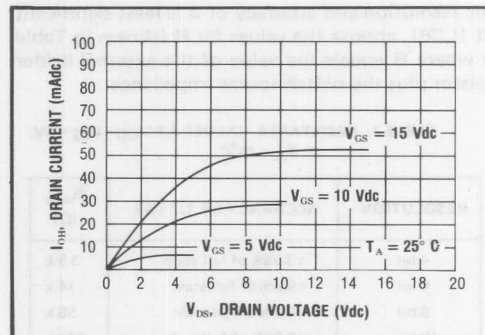


Typical N-Channel
Sink Current Characteristics

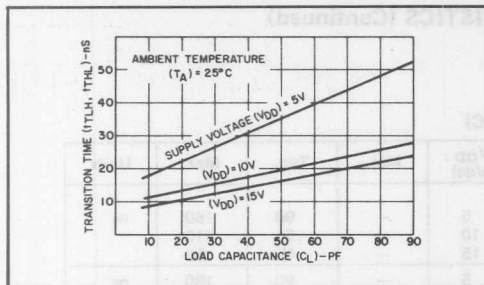
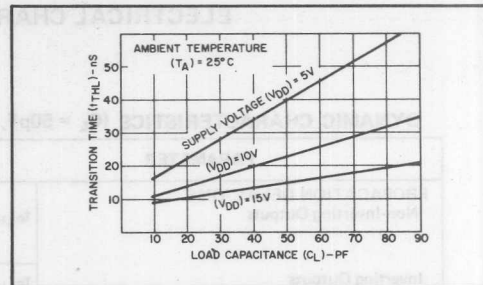
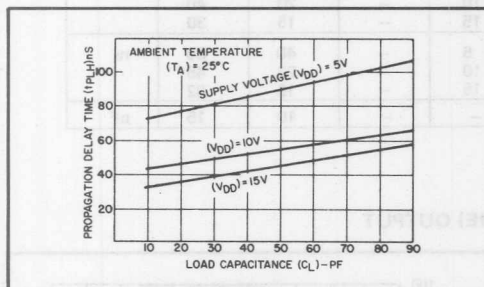
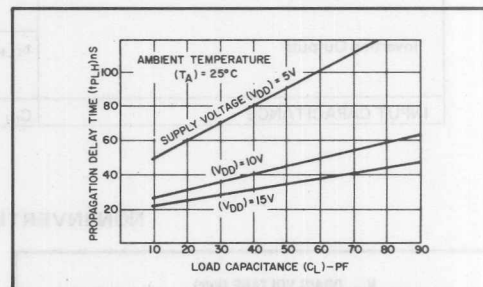
INVERTING (COMPLEMENT) OUTPUT



Typical P-Channel
Source Current Characteristics

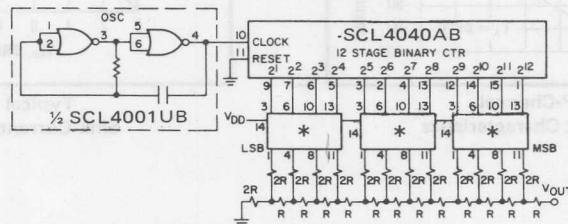


Typical N-Channel
Sink Current Characteristics

Typical transition time vs. C_L -true output.Typical transition time vs. C_L -complement output.Typical propagation delay time vs. C_L -true output.Typical propagation delay time vs. C_L -complement output.

APPLICATIONS INFORMATION

Low Power D/A Converter



* SCL4041UB

For resolution and accuracy of $\pm \frac{1}{2}$ least significant bit (LSB), choose the values for R (shown in Table I) where R equals the value of the external ladder resistor plus the switch source impedance.

TABLE I. RESISTANCE VALUES AT $V_{DD}-V_{SS} = 5V$,
 $T_A = 25^\circ C$

RESOLUTION	ACCURACY OF 1/2 LSB	R_{min} (Ω)
4 bit	$\pm 3.25\%$ of full scale	3.5 k
6 bit	$\pm 0.8\%$ of full scale	14 k
8 bit	$\pm 0.2\%$ of full scale	56 k
10 bit	$\pm 0.05\%$ of full scale	224 k
12 bit	$\pm 0.0125\%$ of full scale	896 k

The values have been tabulated for $V_{DD} = 5V$ and $V_{SS} = 0V$. For different supply (reference) voltages, the switch source impedance must be computed and added to the value of R shown in Table I).

TABLE II. ON RESISTANCE VALUES
AT $V_{DS} = 0.1V$, $T_A = 25^\circ C$

$V_{DD}-V_{SS}$ (Volts)	R_N (Ω)	R_P (Ω)
5	175 ± 50	200 ± 75
10	75 ± 25	90 ± 30



FEATURES

- ◆ Common Clock
- ◆ Positive- or Negative-Edge Clocking
- ◆ Q and $\bar{Q}$ Outputs Available from Each Latch

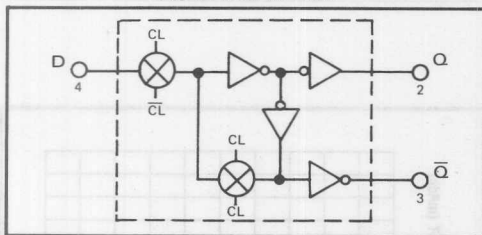
DESCRIPTION

SCL4042B devices contain four Latch circuits, each strobed by a common Clock. Complementary buffered outputs are available from each circuit.

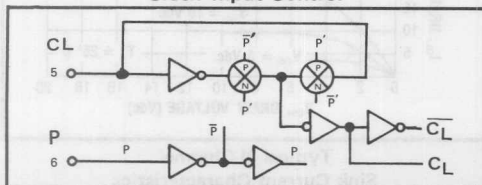
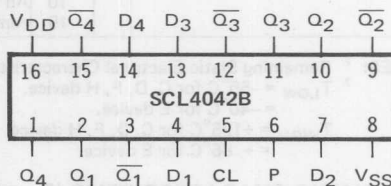
Information present at the Data input is transferred to outputs Q and $\bar{Q}$ during the Clock level which is programmed by the Polarity input. For Polarity = 0 the transfer occurs during the 0 Clock level and for Polarity = 1 the transfer occurs during the 1 Clock level. The outputs follow the Data inputs providing the Clock and Polarity levels defined above are present. When a Clock transition occurs (positive for Polarity = 0 and negative for Polarity = 1) the information present at the input during the Clock transition is retained at the outputs until an opposite Clock transition occurs.

TRUTH TABLE

CLOCK	POLARITY	Q
0	0	D
	0	LATCH
1	1	D
	1	LATCH

LOGIC DIAGRAMS
One of four latches

Clock Input Control

CONNECTION DIAGRAM
(all packages)

Add suffix for package:

- C 16-pin Cerdip
- D 16-pin Ceramic
- E 16-pin Epoxy
- F 16-pin Flat
- H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

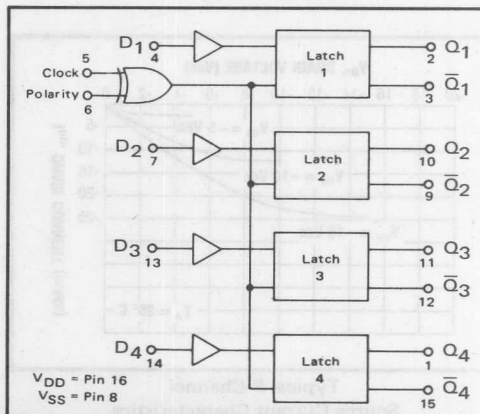
DC Supply Voltage $V_{DD} - V_{SS}$ 3 to 15 Vdc

Operating Temperature T_A

C, D, F, H Device -55 to +125 °C

E Device -40 to +85 °C

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS¹

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	V _{IN} =V _{SS} or V _{DD} All valid input combinations	—	1.0	—	0.005	1.0	—	30	μAdc
			—	2.0	—	0.01	2.0	—	60	
			—	4.0	—	0.02	4.0	—	120	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

² T_{LOW} = -55°C for C, D, F, H device.

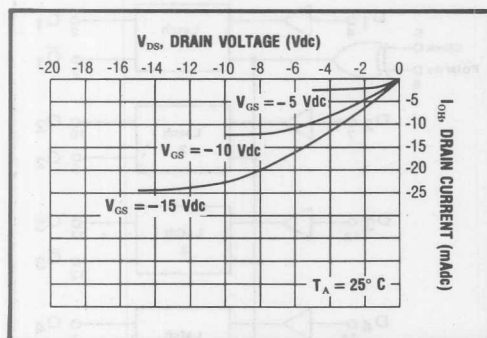
= -40°C for E device.

T_{HIGH} = +125°C for C, D, F, H device.

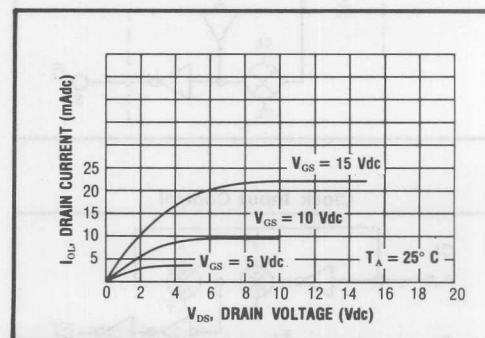
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V _{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME From Data Inputs	t _{PLH} , t _{PHL}	5	—	150	300	ns
		10	—	75	150	
		15	—	60	120	
	t _{PLH} , t _{PHL}	5	—	175	350	ns
		10	—	85	170	
		15	—	70	140	
OUTPUT TRANSITION TIME	t _{TLH} , t _{THL}	5	—	100	200	ns
		10	—	50	100	
		15	—	40	80	
MINIMUM CLOCK PULSE WIDTH	PW _{CL}	5	—	125	250	ns
		10	—	40	80	
		15	—	30	60	
MAXIMUM CLOCK RISE AND FALL TIME	t _{rCL} , t _{fCL}	5	15	—	—	μs
		10	5	—	—	
		15	3	—	—	
MINIMUM DATA INPUT SETUP TIME	t _{setup}	5	—	-20	50	ns
		10	—	-10	30	
		15	—	-5	25	
MINIMUM DATA INPUT HOLD TIME	t _{hold}	5	—	0	100	ns
		10	—	0	50	
		15	—	0	40	



Typical P-Channel
Source Current Characteristics



Typical N-Channel
Sink Current Characteristics

SCL4043AB NOR-Type SCL4044AB NAND-Type



CMOS QUAD 3-STATE R-S LATCHES

FEATURES

- ◆ Separate Set and Reset Inputs for each Latch
- ◆ Active-High (SCL4043AB) or Active-Low (SCL4044AB) Inputs
- ◆ 3-State Outputs with Common Enable

DESCRIPTION

SCL4043AB types are Quad cross-coupled 3-state CMOS NOR Latches, and the SCL4044AB types are Quad cross-coupled 3-state CMOS NAND Latches. Each latch has a separate Q output and individual Set and Reset inputs. The Q outputs are gated through transmission gates controlled by a common Enable input. A logic "1" or "high" on the Enable input connects the latch states to the Q outputs. A logic "0" or "low" on the Enable input disconnects the latch states from the Q outputs, resulting in an open circuit condition on the Q outputs. The open circuit feature allows common bussing of the outputs. The logic operation of the latches is summarized in the truth table below.

TRUTH TABLES

SCL4043AB

S	R	E	Q
X	X	0	OC*
0	0	1	NC+
1	0	1	1
0	1	1	0
1	1	1	Δ

* OPEN CIRCUIT

+ NO CHANGE

Δ DOMINATED BY S = 1 INPUT

SCL4044AB

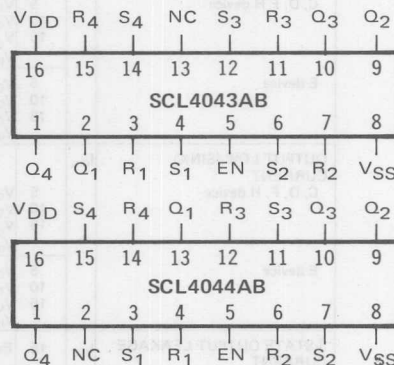
S	R	E	Q
X	X	X	OC*
1	1	1	NC+
0	1	1	1
1	0	1	0
0	0	1	ΔΔ

* OPEN CIRCUIT

+ NO CHANGE

ΔΔ DOMINATED BY R = 0 INPUT

CONNECTION DIAGRAMS (all packages)



Add suffix for package:

C	16-pin Cerdip	F	16-pin Flat
D	16-pin Ceramic	H	Chip
E	16-pin Epoxy		

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

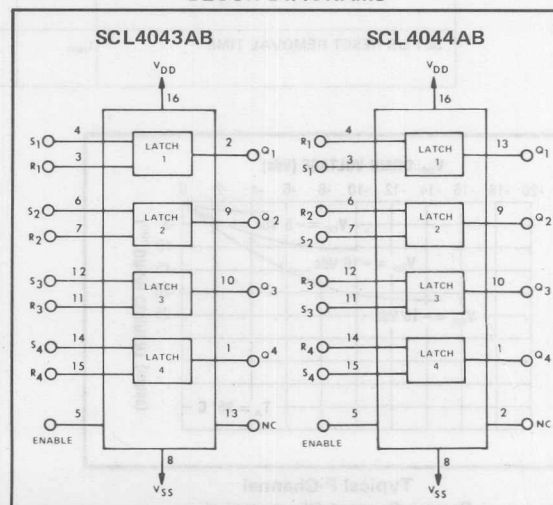
DC Supply Voltage $V_{DD} - V_{SS}$ 3 to 15 Vdc

Operating Temperature T_A

C, D, F, H Device -55 to +125 °C

E Device -40 to +85 °C

BLOCK DIAGRAMS



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS¹

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	5	—	1.0	—	0.005	1.0	—	30	μA _{dc}
		10	—	2.0	—	0.01	2.0	—	60	
		15	—	4.0	—	0.02	4.0	—	120	
OUTPUT HIGH (SOURCE) CURRENT C, D, F, H device	I _{OH}	5	V _{OH} =4.6V	-0.2	—	-0.16	-0.5	—	-0.11	mA _{dc}
		10	V _{OH} =9.5V	-0.5	—	-0.4	-1.1	—	-0.28	
		15	V _{OH} =13.5V V _{IN} =V _{SS} or V _{DD}	-1.5	—	-1.2	-4.5	—	-0.84	
E device		5	V _{OH} =4.6V	-0.19	—	-0.16	-0.5	—	-0.13	mA _{dc}
		10	V _{OH} =9.5V	-0.48	—	-0.4	-1.1	—	-0.32	
		15	V _{OH} =13.5V V _{IN} =V _{SS} or V _{DD}	-1.4	—	-1.2	-4.5	—	-1.0	
OUTPUT LOW (SINK) CURRENT C, D, F, H device	I _{OL}	5	V _{OL} =0.4V	0.25	—	0.2	0.5	—	0.14	mA _{dc}
		10	V _{OL} =0.5V	0.62	—	0.5	1.0	—	0.35	
		15	V _{OL} =1.5V V _{IN} =V _{SS} or V _{DD}	1.9	—	1.5	5.9	—	1.1	
E device		5	V _{OL} =0.4V	0.24	—	0.2	0.5	—	0.16	mA _{dc}
		10	V _{OL} =0.5V	0.6	—	0.5	1.0	—	0.41	
		15	V _{OL} =1.5V V _{IN} =V _{SS} or V _{DD}	1.8	—	1.5	5.9	—	1.2	
3-STATE OUTPUT LEAKAGE CURRENT	I _{ZL}	15	Enable = V _{SS}	—	±0.1	—	±10 ⁻⁴	±0.1	—	±1.0 μA _{dc}

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".² T_{LOW} = -55°C for C, D, F, H device.

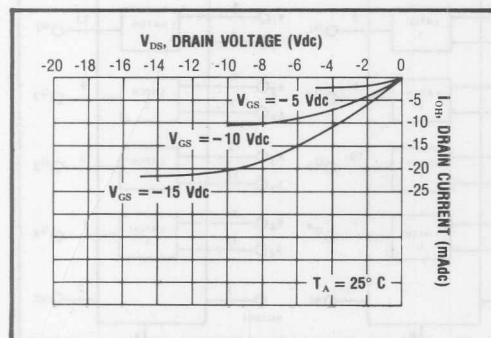
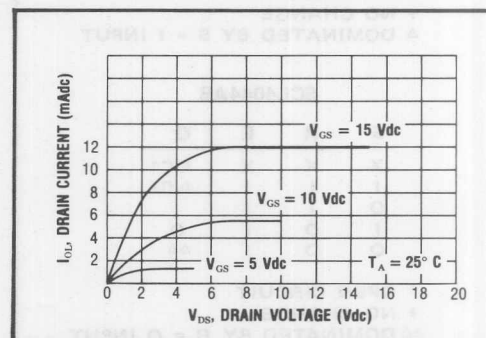
= -40°C for E device.

T_{HIGH} = +125°C for C, D, F, H device.

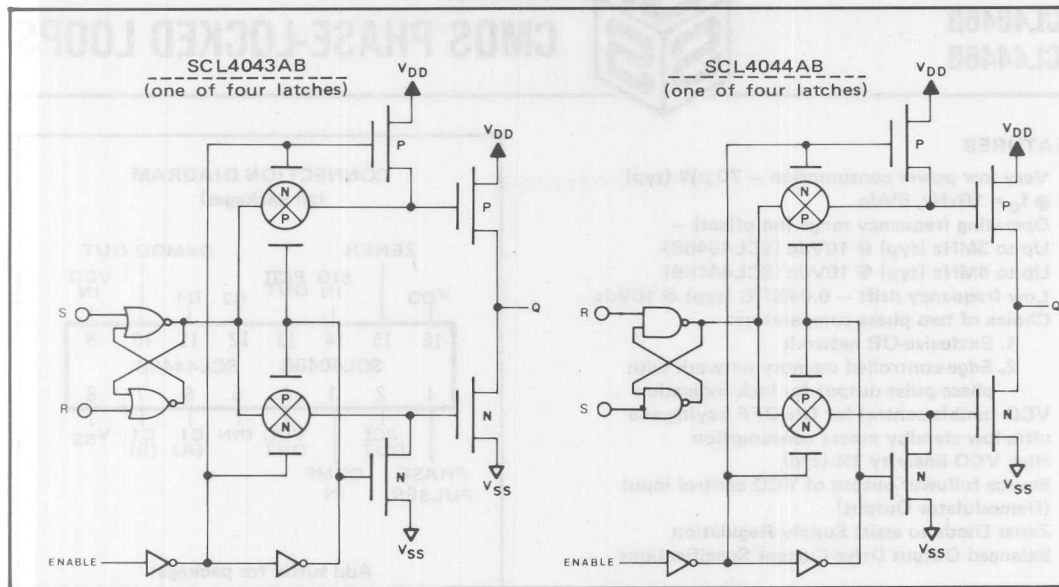
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

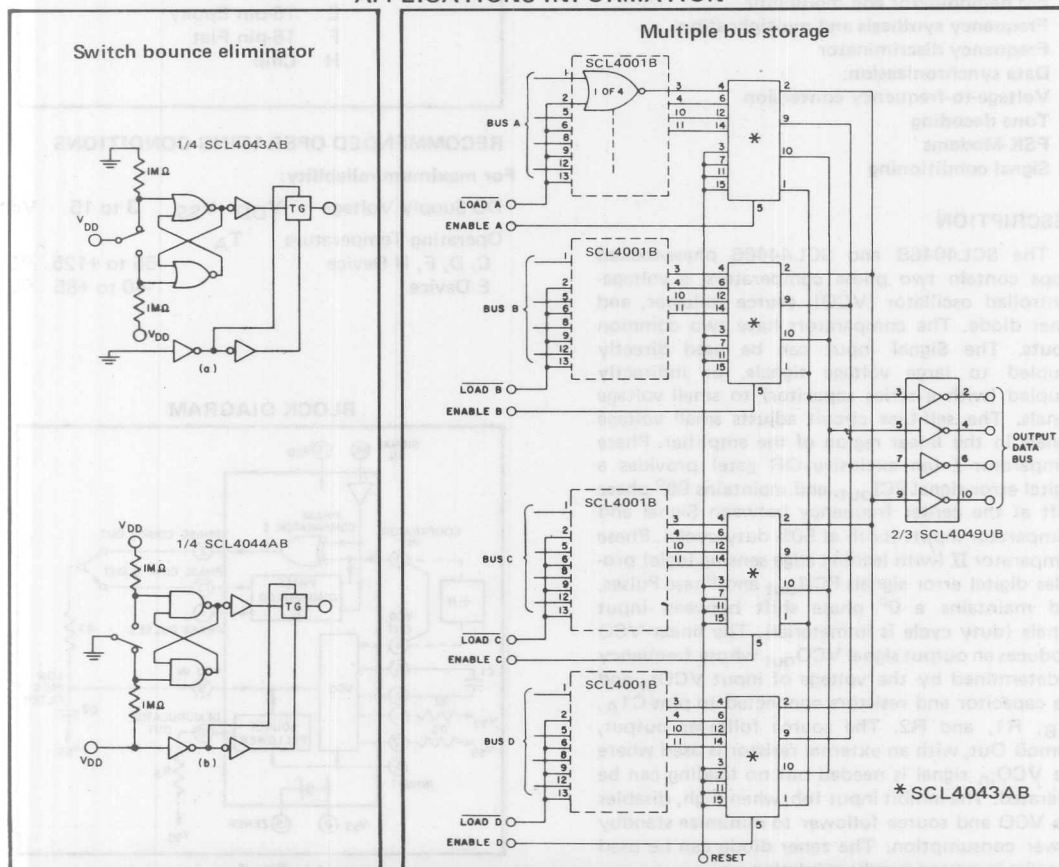
PARAMETER	V _{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME From S or R Inputs	t _{PLH} , t _{PHL}	5	—	175	ns
		10	—	85	
		15	—	70	
From Enable Input	t _{PHZ} , t _{PLZ}	5	—	70	ns
	t _{PZH} , t _{PZL}	10	—	35	
		15	—	30	
OUTPUT TRANSITION TIME	t _{TLH} , t _{THL}	5	—	180	ns
		10	—	90	
		15	—	65	
MINIMUM SET OR RESET PULSE WIDTH	PW _S , PW _R	5	—	100	ns
		10	—	50	
		15	—	40	
SET OR RESET REMOVAL TIME	t _{rem}	5	—	25	ns
		10	—	15	
		15	—	10	

Typical P-Channel
Source Current CharacteristicsTypical N-Channel
Sink Current Characteristics

LOGIC DIAGRAMS



APPLICATIONS INFORMATION



SCL4046B SCL4446B



CMOS PHASE-LOCKED LOOPS

FEATURES

- ◆ Very low power consumption – 70 μ W (typ)
@ $f_o = 10$ kHz, 5Vdc
- ◆ Operating frequency range (no offset) –
Up to 3MHz (typ) @ 10Vdc (SCL4046B)
Up to 4MHz (typ) @ 10Vdc (SCL4446B)
- ◆ Low frequency drift – 0.04%/°C (typ) @ 10Vdc
- ◆ Choice of two phase comparators:
 1. Exclusive-OR network
 2. Edge-controlled memory network with phase-pulse output for lock indication
- ◆ VCO Inhibit control for ON-OFF keying and ultra-low standby power consumption
- ◆ High VCO linearity 1% (typ)
- ◆ Source-follower output of VCO control input (Demodulator Output)
- ◆ Zener Diode to assist Supply Regulation
- ◆ Balanced Output Drive Current Specifications

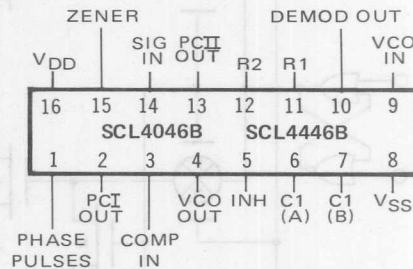
APPLICATIONS

- ◆ FM demodulator and modulator
- ◆ Frequency synthesis and multiplication
- ◆ Frequency discriminator
- ◆ Data synchronization
- ◆ Voltage-to-frequency conversion
- ◆ Tone decoding
- ◆ FSK-Modems
- ◆ Signal conditioning

DESCRIPTION

The SCL4046B and SCL4446B phase-locked loops contain two phase comparators, a voltage-controlled oscillator (VCO), source follower, and zener diode. The comparators have two common inputs. The Signal input can be used directly coupled to large voltage signals, or indirectly coupled (with a series capacitor) to small voltage signals. The self-bias circuit adjusts small voltage signals in the linear region of the amplifier. Phase comparator I (an exclusive-OR gate) provides a digital error signal PCI_{out} , and maintains 90° phase shift at the center frequency between Signal and Comparator inputs (both at 50% duty cycle). Phase comparator II (with leading edge sensing logic) provides digital error signals $PCII_{out}$ and Phase Pulses, and maintains a 0° phase shift between input signals (duty cycle is immaterial). The linear VCO produces an output signal VCO_{out} whose frequency is determined by the voltage of input VCO_{in} and the capacitor and resistors connected to pins C1A, C1B, R1, and R2. The source follower output, Demod Out, with an external resistor is used where the VCO_{in} signal is needed but no loading can be tolerated. The inhibit input Inh , when high, disables the VCO and source follower to minimize standby power consumption. The zener diode can be used to assist in power supply regulation.

CONNECTION DIAGRAM (all packages)



Add suffix for package:

- C 16-pin Cerdip
- D 16-pin Ceramic
- E 16-pin Epoxy
- F 16-pin Flat
- H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A	-55 to +125	°C
C, D, F, H Device		-40 to +85	°C
E Device			

BLOCK DIAGRAM

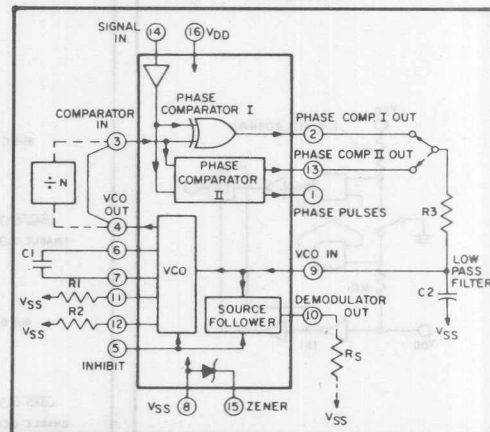


Fig. 1

VCO SECTION

The VCO requires one external capacitor (C1) and one to two external resistors (R1 or R1 and R2). Resistor R1 and capacitor C1 determine the frequency range of the VCO and resistor R2 enables the VCO to have a frequency offset if required. The high input impedance ($10^{12}\Omega$) of the VCO simplifies the design of low-pass filters by permitting the designer a wide choice of resistor-to-capacitor ratios. In order not to load the low-pass filter, a source-follower output of the VCO input voltage is provided at terminal 10 (DEMODULA-

TOR OUTPUT). If this terminal is used, a load resistor (R_S) of $50k\Omega$ or more should be connected from this terminal to V_{SS} . If unused, this terminal should be left open. The VCO can be connected directly or through frequency dividers to the comparator input of the phase comparators. A full CMOS logic swing is available at the output of the VCO. A logic 0 on the INHIBIT input "enables" the VCO and the source follower, while a logic 1 "turns off" both to minimize stand-by power consumption.

PHASE COMPARATORS

The phase-comparator signal input (terminal 14) can be direct-coupled provided the signal swing is within CMOS logic levels [logic "0" $\leq 30\% (V_{DD} - V_{SS})$, logic "1" $\geq 70\% (V_{DD} - V_{SS})$]. For smaller swings the signal must be capacitively coupled to the self-biasing amplifier at the signal input.

Phase comparator I is an exclusive-OR network; it operates analogously to an over-driven balanced mixer. To maximize the lock range, the signal and comparator-input frequencies must have a 50% duty cycle. With no signal or noise on the signal input, this phase comparator has an average output voltage equal to $V_{DD}/2$. The low-pass filter connected to the output of phase comparator I supplies the averaged voltage to the VCO input, and causes the VCO to oscillate at the center frequency (f_0).

The frequency range of input signals on which the PLL will lock, if it was initially out of lock, is defined as the frequency capture range ($2f_c$).

The frequency range of input signals on which the loop will stay locked if it was initially in lock is defined as the frequency lock range ($2f_L$). The capture range can not exceed the lock range.

With phase comparator I, the range of frequencies over which the PLL can acquire lock (capture range) is dependent on the low-pass-filter characteristics, and can be made as large as the lock range. Phase-comparator I enables a PLL system to remain in lock in spite of high amounts of noise in the input signal.

One characteristic of this type of phase comparator is that it may lock onto input frequencies that are close to harmonics of the VCO center-frequency. A second characteristic is that the phase angle between the signal and the comparator input varies between 0° and 180° , and is 90° at the center frequency. Figure 2 shows the (typical) triangular phase-to-output response characteristic of phase-comparator I. Typical waveforms for a CMOS phase-locked-loop employing phase comparator I in locked condition is shown in Figure 3.

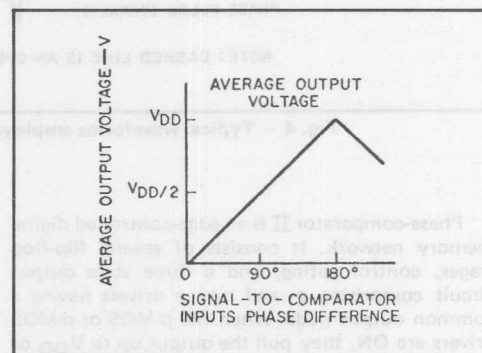


Fig. 2 — Phase-comparator I characteristics at low-pass filter output.

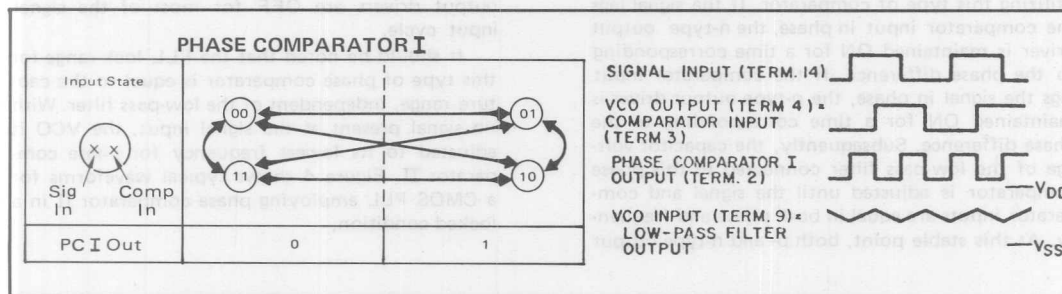


Fig. 3 — Typical waveforms employing phase comparator I in locked condition

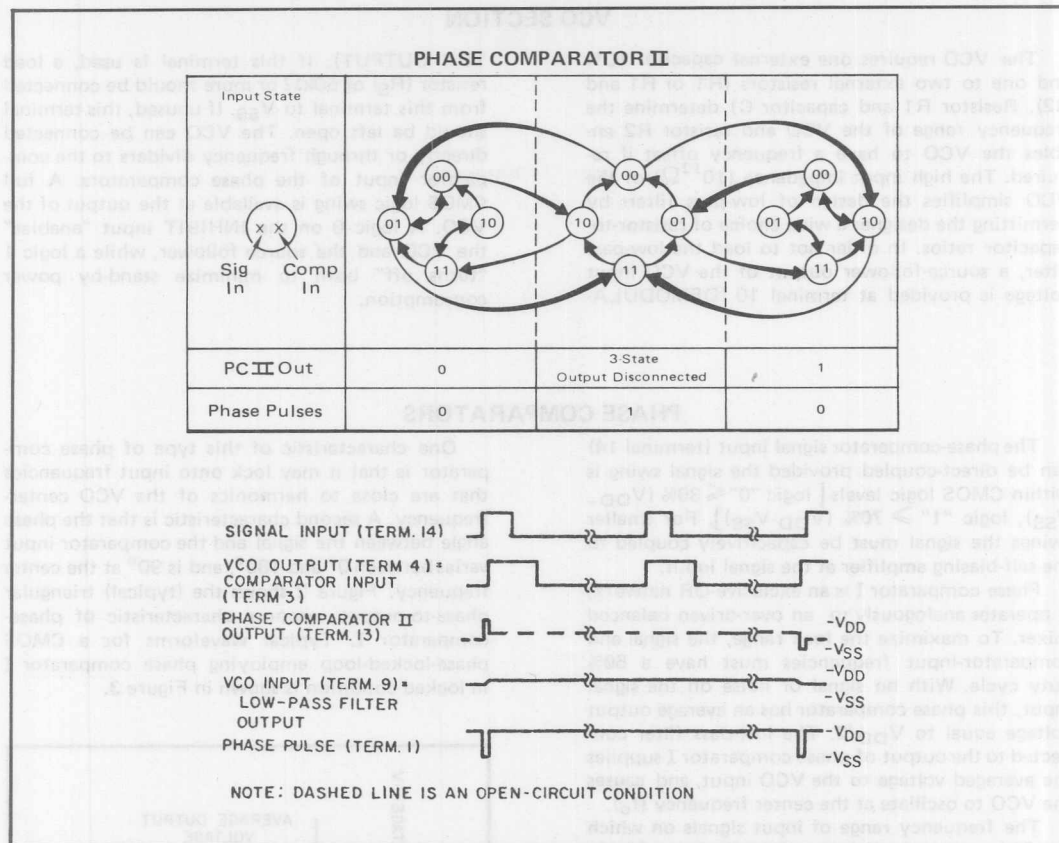


Fig. 4 — Typical waveforms employing phase comparator II in locked condition.

Phase-comparator II is an edge-controlled digital memory network. It consists of several flip-flop stages, control gating, and a three state output circuit comprising p- and n-type drivers having a common output node. When the p-MOS or n-MOS drivers are ON, they pull the output up to V_{DD} or down to V_{SS} , respectively. This type of phase comparator acts only on the positive edges of the signal and comparator inputs. The duty cycles of the signal and comparator inputs are not important since positive transitions control the PLL system utilizing this type of comparator. If the signal lags the comparator input in phase, the n-type output driver is maintained ON for a time corresponding to the phase difference. If the comparator input lags the signal in phase, the p-type output driver is maintained ON for a time corresponding to the phase difference. Subsequently, the capacitor voltage of the low-pass filter connected to this phase comparator is adjusted until the signal and comparator inputs are equal in both phase and frequency. At this stable point, both p- and n-type output

drivers remain OFF. Thus, the phase comparator output becomes an open circuit and holds the voltage on the capacitor of the low-pass filter constant. Moreover, the signal at the "phase pulses" output is a high level which can be used for indicating a locked condition. Thus, for phase comparator II, no phase difference exists between signal and comparator input over the full VCO frequency range. Moreover, the power dissipation due to the low-pass filter is reduced when this type of phase comparator is used because both the p- and n-type output drivers are OFF for most of the signal input cycle.

It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range, independent of the low-pass filter. With no signal present at the signal input, the VCO is adjusted to its lowest frequency for phase comparator II. Figure 4 shows typical waveforms for a CMOS PLL employing phase comparator II in a locked condition.

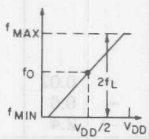
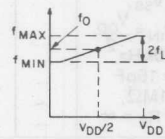
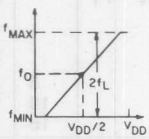
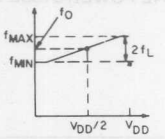
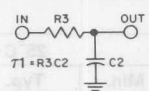
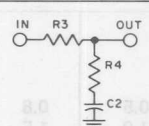
DESIGN INFORMATION

This information is a guide for approximating the values of external components for the SCL4046B and SCL4446B in a Phase-Locked Loop system. The selected external components must be within the following ranges:

$$R1, R2 \geq 2k\Omega, R_S \geq 10k\Omega$$

$$C1 \geq 15pF$$

In addition to the given design information refer to Figure 5 for R1, R2, and C1 component selections.

CHARACTERISTICS	USING PHASE COMPARATOR I		USING PHASE COMPARATOR II	
	VCO WITHOUT OFFSET $R_2 = \infty$	VCO WITH OFFSET	VCO WITHOUT OFFSET $R_2 = \infty$	VCO WITH OFFSET
VCO Frequency				
For No Signal Input	VCO in PLL system will adjust to center frequency, f_0		VCO in PLL system will adjust to lowest operating frequency, f_{min}	
Frequency Lock Range, $2f_L$	$2f_L = \text{full VCO frequency range}$ $2f_L = f_{max} - f_{min}$			
Frequency Capture Range, $2f_C$	 $T1 = R3C2$ $2f_C \approx \frac{1}{\pi} \sqrt{\frac{2\pi f_L}{T1}}$		$f_C = f_L$	
Loop Filter Component Selection	 For $2f_C$, see Ref.			
Phase Angle between Signal and Comparator	90° at center frequency (f_0), approximating 0° and 180° at ends of lock range ($2f_L$)		Always 0° in lock	
Locks on Harmonics of Center Frequency	Yes		No	
Signal Input Noise Rejection	High		Low	
VCO Component Selection	- Given: f_0 - Use f_0 with Fig.5a to determine R1 and C1	- Given: f_0 and f_L - Calculate f_{min} from the equation $f_{min} = f_0 - f_L$ - Use f_{min} with Fig. 5b to determine R2 and C1 - Calculate $\frac{f_{max}}{f_{min}}$ from the equation $\frac{f_{max}}{f_{min}} = \frac{f_0 + f_L}{f_0 - f_L}$ - Use $\frac{f_{max}}{f_{min}}$ with Fig.5c to determine ratio R2/R1 to obtain R1	- Given: f_{max} - Calculate f_0 from the equation $f_0 = \frac{f_{max}}{2}$ - Use f_0 with Fig.5a to determine R1 and C1	- Given: f_{min} & f_{max} - Use f_{min} with Fig.5b to determine R2 and C1 - Calculate $\frac{f_{max}}{f_{min}}$ - Use $\frac{f_{max}}{f_{min}}$ with Fig.5c to determine ratio R2/R1 to obtain R1

REF. G. S. Moschytz, "Miniaturized RC Filters Using Phase-Locked Loop", BSTJ, May, 1965.

ELECTRICAL CHARACTERISTICS^{1, 3}

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	Inhibit = V _{DD}	—	5	—	0.05	5	—	150	μAdc
		Signal Input = V _{DD}	—	10	—	0.01	10	—	300	
			—	20	—	0.2	20	—	600	
TOTAL POWER DISSIPATION	P _T	Inh = V _{SS} , VCO _{IN} = $\frac{V_{DD}}{2}$								mW
		f _o = 10kHz, C _L = 15pF	—	—	—	0.07	—	—	—	
		R ₁ = 1MΩ, R ₂ = R _S = ∞	—	—	—	0.6	—	—	—	
			—	—	—	2.4	—	—	—	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

² T_{LOW} = -55°C for C, D, F, H device.

= -40°C for E device.

T_{HIGH} = +125°C for C, D, F, H device.

= + 85°C for E device.

³ VCO output (pin 4) and Phase Comparator Outputs (pins 2 and 13) have been designed for balanced output drive current specifications. Consult Family Specifications.

PARAMETER	CONDITIONS	V _{DD}	25°C			UNIT						
			Min.	Typ.	Max.							
VCO SECTION												
MAXIMUM OPERATING FREQUENCY SCL4046B	f _{max}	R2 = ∞ VCO _{IN} = V _{DD}	R1 C1									
			10k 50pF	5 10 15	0.5 1.0 1.3	0.8 1.5 1.9	— — —	MHz				
			5k 50pF	5 10 15	0.6 1.4 1.8	1.0 2.1 2.7	— — —	MHz				
			2k 50pF	5 10 15	— — —	1.3 2.9 3.8	— — —	MHz				
			SCL4446B	R2 = ∞ VCO _{IN} = V _{DD}	R1 C1							
					10k 50pF	5 10 15	0.7 1.3 1.9	1.0 2.0 2.8	— — —	MHz		
					5k 50pF	5 10 15	0.9 1.9 2.6	1.3 2.9 3.9	— — —	MHz		
					2k 50pF	5 10 15	— — —	1.8 3.9 5.4	— — —	MHz		
					LINEARITY		R2 = ∞ VCO _{IN} = 2.5±0.3V, R1 ≥10kΩ	5	—	1	—	%
							VCO _{IN} = 5.0±2.5V, R1 ≥400kΩ	10	—	1	—	
							VCO _{IN} = 7.5±5.0V, R1 ≥1MΩ	15	—	1	—	

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER		CONDITIONS	V _{DD}	+25°C			UNIT
				Min.	Typ.	Max.	
VCO SECTION (Continued)							
TEMPERATURE-FREQUENCY STABILITY	No Offset	R2 = ∞	5	—	0.12-0.24	—	% / °C
			10	—	0.04-0.08	—	
			15	—	0.015-0.03	—	
	With Offset	R2 ≤ 10X R1	5	—	0.06-0.12	—	% / °C
			10	—	0.05-0.1	—	
			15	—	0.03-0.06	—	
INPUT RESISTANCE (VCO _{IN})	R _{IN}		5, 10, 15	—	10 ⁶	—	MΩ
OUTPUT DUTY CYCLE		All valid input combinations and voltages		—	50	—	%
OUTPUT TRANSITION TIME	t _{TLH} , t _{THL}	C _L = 50pF	5	—	100	200	ns
			10	—	50	100	
			15	—	40	80	
			PHASE COMPARATORS				
INPUT RESISTANCE Signal Input	R _{IN}		5	1	3	—	MΩ
			10	0.2	0.7	—	
			15	0.1	0.3	—	
Comparator Input	R _{IN}		5, 10, 15	—	10 ⁶	—	MΩ
AC-COUPLED INPUT SENSITIVITY Signal Input	V _{IN}		5	—	200	400	mV
			10	—	400	800	
			15	—	700	1400	
			OUTPUT TRANSITION TIME				
PCI, PCII Outputs	t _{TLH} , t _{THL}	C _L = 50pF	5	—	100	200	ns
			10	—	50	100	
			15	—	40	80	
Phase Pulses Output	t _{TLH} , t _{THL}		5	—	130	260	ns
			10	—	65	130	
			15	—	50	100	
DEMODULATOR OUTPUT							
OFFSET VOLTAGE	VCO _{IN} - V _{DEM}	R _S ≥ 50kΩ	5	—	1.4	2.2	Vdc
			10	—	1.6	2.2	
			15	—	1.8	2.2	
LINEARITY		R _S ≥ 50kΩ VCO _{IN} = 2.5±0.3V VCO _{IN} = 5.0±2.5V VCO _{IN} = 7.5±5.0V	5	—	0.1	—	%
			10	—	0.6	—	
			15	—	0.8	—	
			ZENER DIODE				
ZENER VOLTAGE	V _Z	I _Z = 50μA	—	6.3	7.0	7.7	V
DYNAMIC RESISTANCE	R _Z	I _Z = 1mA	—	—	100	—	Ω

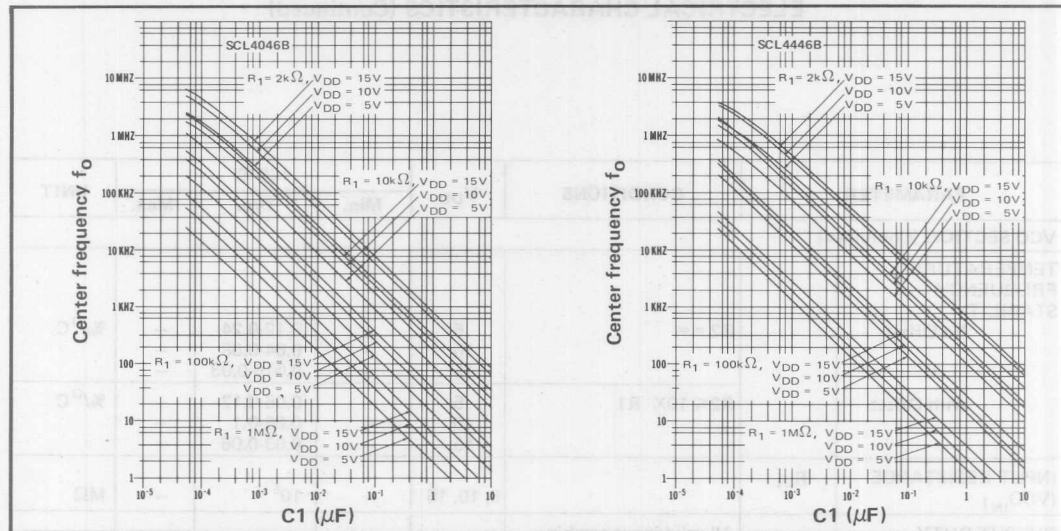


Fig. 5 (a) Typical center frequency (f_0) vs C_1 ($R_2 = \infty$, $V_{COIN} = \frac{V_{DD}}{2}$, $T_A = 25^\circ C$)

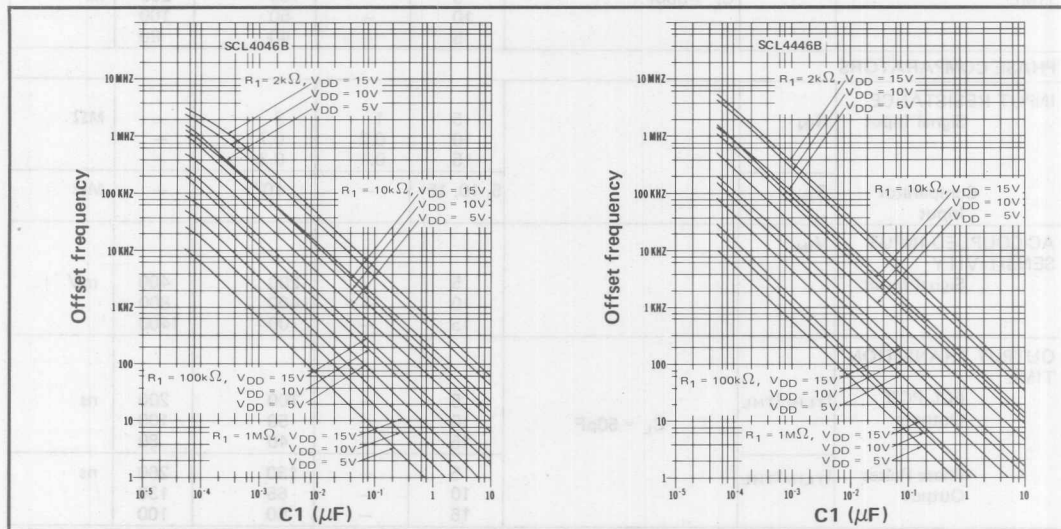


Fig. 5 (b) Typical frequency offset vs C_1 ($V_{COIN} = V_{SS}$, $T_A = 25^\circ C$)

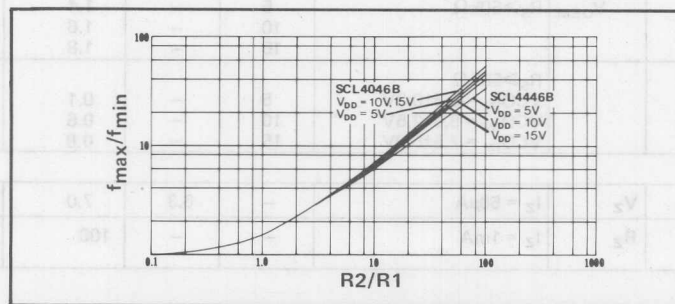


Fig. 5 (c) Typical f_{max}/f_{min} vs R_2/R_1

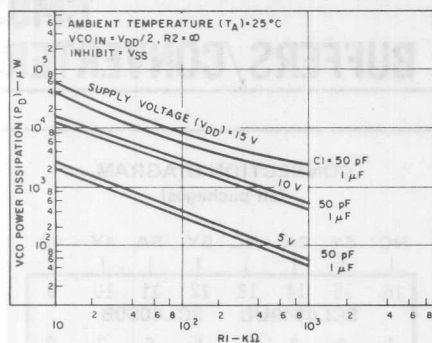


Fig. 6 (a) - Typical VCO power dissipation at center frequency vs R1.

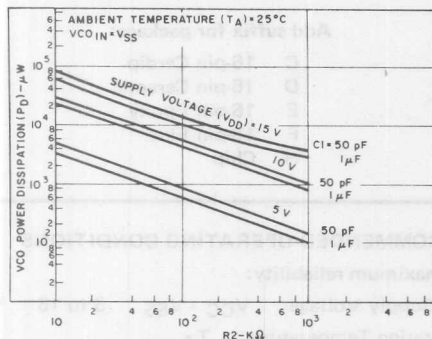


Fig. 6 (b) - Typical VCO power dissipation at $f_{\min}$ vs R2.

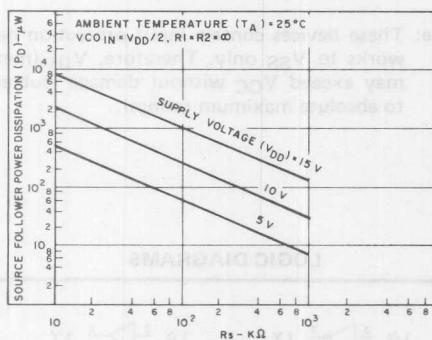


Fig. 6 (c) - Typical source follower power dissipation vs R_S .

NOTE: To obtain approximate total power dissipation of PLL system for no-signal input

$$P_D (\text{Total}) = P_D (f_o) + P_D (f_{\min}) + P_D (R_S) \\ \text{— Phase Comparator I}$$

$$P_D (\text{Total}) = P_D (f_{\min}) \\ \text{— Phase Comparator II}$$

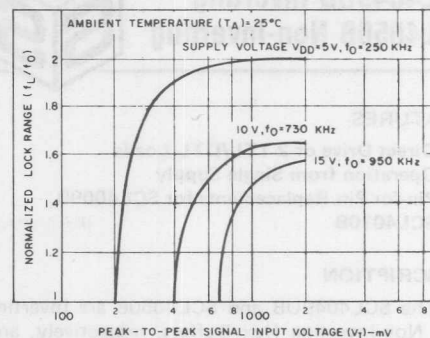


Fig. 7 - Typical lock range vs signal input amplitude

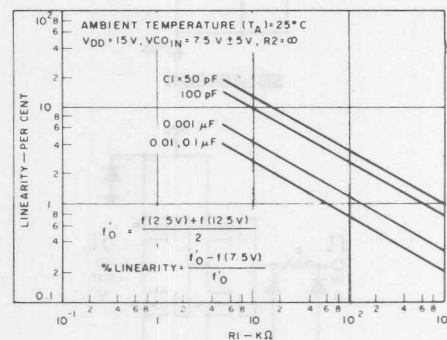
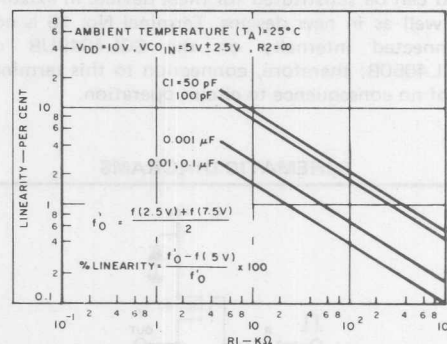


Fig. 8(a, b) - Typical VCO linearity vs R1 and C1

SCL4049UB Inverting SCL4050B Non-Inverting



CMOS HEX BUFFERS/CONVERTERS

FEATURES

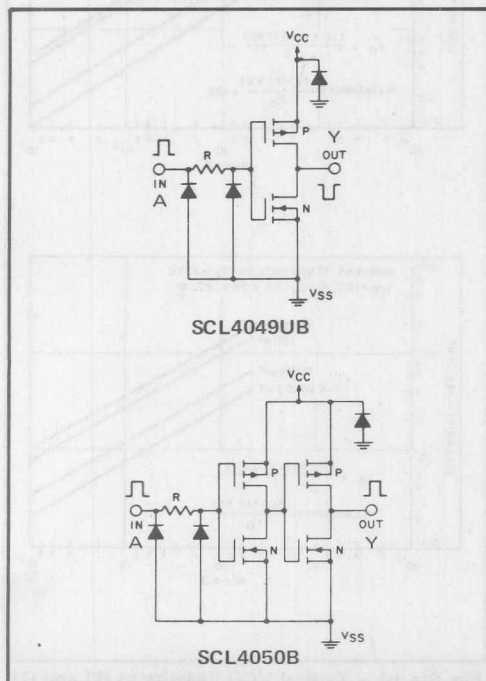
- ◆ Direct Drive of 2 TTL/DTL Loads
- ◆ Operation from Single Supply
- ◆ Pin-for Pin Replacements for SCL4009B, SCL4010B

DESCRIPTION

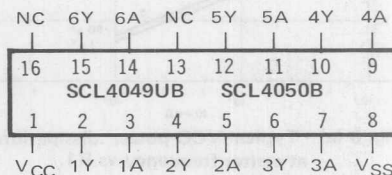
The SCL4049UB and SCL4050B are Inverting and Non-Inverting Hex Buffers, respectively, and feature logic-level conversion using only one supply voltage (V_{CC}). The Input-signal high level (V_{IH}) can exceed the V_{CC} supply voltage when these devices are used for logic-level conversions. These devices are intended for use as CMOS-to-DTL/TTL converters and can drive directly two DTL/TTL Loads.

The SCL4049UB and SCL4050B are interchangeable with SCL4009UB and SCL4010B devices, respectively. In these applications the SCL4049UB and SCL4050B are pin-compatible with the SCL4009UB and SCL4010B, respectively, and can be substituted for these devices in existing as well as in new designs. Terminal No. 16 is not connected internally on the SCL4049UB or SCL4050B; therefore, connection to this terminal is of no consequence to circuit operation.

SCHEMATIC DIAGRAMS



CONNECTION DIAGRAM (all packages)



Add suffix for package:

- C 16-pin Cerdip
- D 16-pin Ceramic
- E 16-pin Epoxy
- F 16-pin Flat
- H Chip

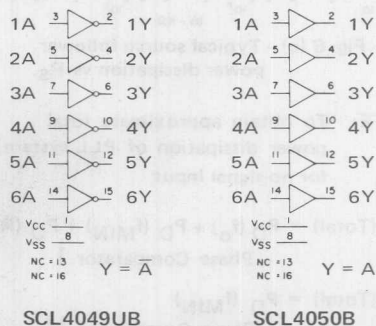
RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{CC} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

Note: These devices contain input protection networks to V_{SS} only. Therefore, V_{IH} (max) may exceed V_{CC} without damage (subject to absolute maximum ratings).

LOGIC DIAGRAMS



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS^{1,3}

PARAMETER		V _{CC} (V _{Dc})	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{CC}	5	V _{IN} =V _{SS} or V _{DD}	—	1.0	—	0.005	1.0	—	30	μAdc
		10	All valid input combinations	—	2.0	—	0.01	2.0	—	60	
		15		—	4.0	—	0.02	4.0	—	120	
MINIMUM INPUT HIGH VOLTAGE SCL4049UB	V _{IH}	5	V _{OL} =0.5V	—	4.0	—	2.75	4.0	—	4.0	Vdc
		10	V _{OL} =1.0V	—	8.0	—	5.5	8.0	—	8.0	
		15	V _{OL} =1.5V	—	12.0	—	8.25	12.0	—	12.0	
MAXIMUM INPUT LOW VOLTAGE SCL4049UB	V _{IL}	5	V _{OH} =3.6V	1.0	—	1.0	2.25	—	1.0	—	Vdc
		10	V _{OH} =7.2V	2.0	—	2.0	4.5	—	2.0	—	
		15	V _{OH} =10.8V	3.0	—	3.0	6.75	—	3.0	—	
OUTPUT LOW (SINK) CURRENT C, D, F, H devices	I _{OL}	5	V _{OL} =0.4V	4.0	—	3.2	6.4	—	2.4	—	mAdc
		10	V _{OL} =0.5V	10	—	8.0	16	—	5.6	—	
		15	V _{OL} =1.5V	30	—	24.0	40	—	16.8	—	
E device			V _{IN} =V _{SS} or V _{DD}								
		5	V _{OL} =0.4V	3.8	—	3.2	6.4	—	2.6	—	mAdc
		10	V _{OL} =0.5V	9.6	—	8.0	16	—	6.4	—	
15	V _{OL} =1.5V	28	—	24.0	40	—	19	—			
			V _{IN} =V _{SS} or V _{DD}								

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

² T_{LOW} = -55°C for C, D, F, H device.

= -40°C for E device.

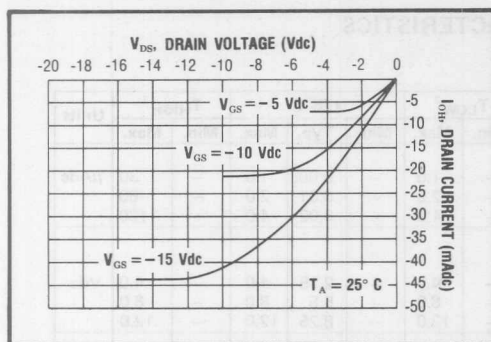
T_{HIGH} = +125°C for C, D, F, H device.

= + 85°C for E device.

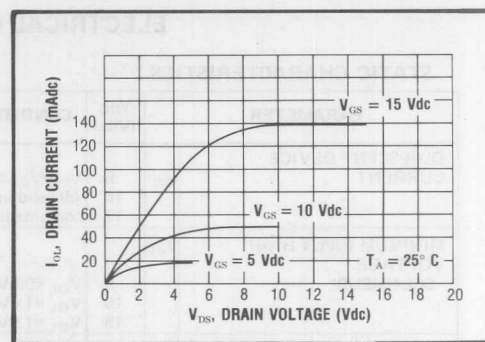
³ These devices have been designed to meet the balanced output drive current specifications for Output High (Source) Current. Consult Family Specifications.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

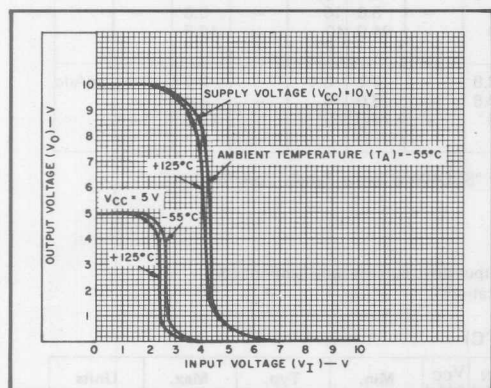
PARAMETER		V _{IN} (V _{dc})	V _{CC} (V _{dc})	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME SCL4049UB	t _{PLH}	5	5	—	60	120	ns
		10	10	—	32	65	
		15	15	—	25	50	
		10	5	—	45	90	ns
		15	5	—	45	90	
SCL4050B		5	5	—	70	140	ns
		10	10	—	40	80	
		15	15	—	30	60	
		10	5	—	45	90	ns
		15	5	—	40	80	
SCL4049UB	t _{PHL}	5	5	—	32	65	ns
		10	10	—	20	40	
		15	15	—	15	30	
		10	5	—	15	30	ns
		15	5	—	10	20	
SCL4050B		5	5	—	55	110	ns
		10	10	—	27	55	
		15	15	—	15	30	
		10	5	—	50	100	ns
		15	5	—	50	100	
OUTPUT TRANSITION TIME	t _{TLH}	5	5	—	80	160	ns
		10	10	—	40	80	
		15	15	—	30	60	
	t _{THL}	5	5	—	30	60	ns
		10	10	—	20	40	
		15	15	—	15	30	
INPUT CAPACITANCE SCL4049UB	C _{IN}	—	—	—	15	22.5	pF



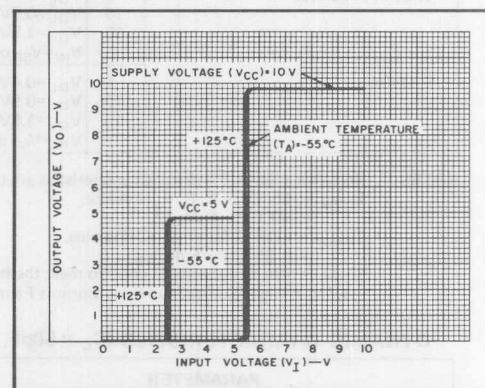
Typical P-Channel
Source Current Characteristics



Typical N-Channel
Sink Current Characteristics



Typical voltage transfer characteristics as a function
of temperature for SCL4049UB.



Typical voltage transfer characteristics as a function
of temperature for SCL4050B.

SCL4051B, SCL4052B SCL4053B



CMOS ANALOG MULTIPLEXERS /DEMULTIPLEXERS

FEATURES

- ◆ Wide Range of Digital and Analog Signal Levels: Digital-3 to 15V, Analog-to 15V_{p-p}
- ◆ Low ON-Resistance: 80Ω (typ.) over entire 15V_{p-p} Signal-Input Range for V_{DD}-V_{EE} = 15V
- ◆ High OFF-Resistance: Input Leakage ± 10pA (typ) @ V_{DD}-V_{EE} = 10V
- ◆ Logic-Level Conversion for Digital Addressing Signals of 3 to 15V (V_{DD}-V_{SS} = 3V to 15V) to Switch Analog Signals to 15V_{p-p} (V_{DD}-V_{EE} = 15V)
- ◆ Matched Switch Characteristics: ΔRON = 5Ω (typ.) for V_{DD}-V_{EE} = 18V
- ◆ Very Low Quiescent Power Dissipation under all Digital Control Input and Supply Conditions: 1μW typ. @ V_{DD}-V_{SS} = V_{DD}-V_{EE} = 10V
- ◆ Binary Address Decoding on Chip

DESCRIPTION

The SCL4051B, SCL4052B, and SCL4053B are Digitally-Controlled Analog Switches having low ON-impedance and very low OFF leakage current. Control of analog signals up to 15V_{p-p} can be achieved by digital signal amplitudes of 3 to 15V. For example, if V_{DD} = +5V, V_{SS} = 0V, and V_{EE} = -5V, analog signals from -5V to +5V can be controlled by digital inputs of 0 to 5V. The multiplexer circuits dissipate extremely low quiescent power over the full V_{DD} - V_{SS} and V_{DD} - V_{EE} supply-voltage ranges, independent of the logic state of the control signals. When a logic "1" is present at the Inhibit input terminal all channels are OFF.

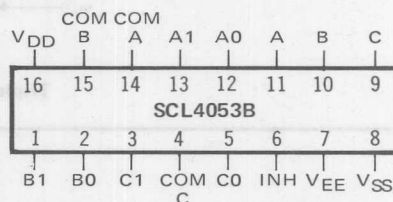
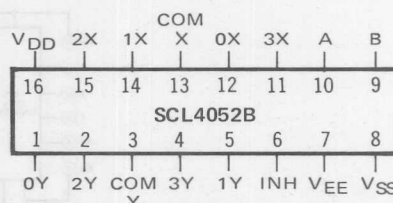
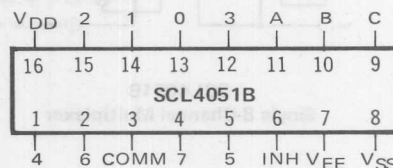
SCL4051B is a Single 8-Channel Multiplexer having three binary Control inputs, A, B, and C, and an Inhibit input. The three binary signals select 1 of 8 channels to be turned ON and connect the input to the output.

SCL4052B is a Differential 4-Channel Multiplexer having two binary Control inputs, A and B, and an Inhibit input. The two binary input signals select 1 of 4 pairs of channels to be turned on and connect the differential analog inputs to the differential outputs.

SCL4053B is a Triple 4-Channel Multiplexer having three separate digital Control inputs, A, B, and C and an Inhibit input. Each control input selects one of a pair of channels which are connected in a single-pole double-throw configuration.

When the devices are used as demultiplexers, the "CHANNEL IN/OUT" terminals are the outputs and the "COMMON OUT/IN" terminal(s) is (are) the input(s).

CONNECTION DIAGRAMS (all packages)



Add suffix for package:

- C 16-pin Cerdip
- D 16-pin Ceramic
- E 16-pin Epoxy
- F 16-pin Flat
- H Chip

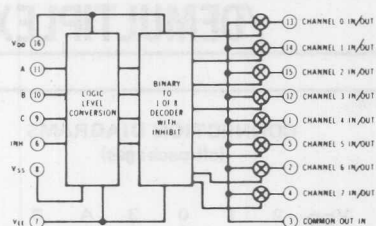
RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

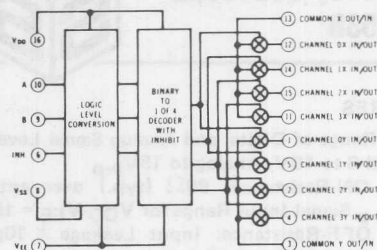
DC Supply Voltage	V _{DD} - V _{SS}	3 to 15	V _{dc}
	V _{DD} - V _{EE}	3 to 15	V _{dc}
Operating Temperature	T _A		
	C, D, F, H Device	-55 to +125	°C
	E Device	-40 to +85	°C

NOTE: There are no restrictions on the relative magnitudes of V_{SS} and V_{EE}, providing Absolute Maximum Ratings are observed.

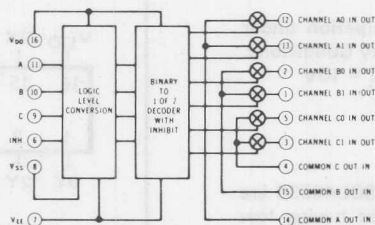
LOGIC DIAGRAMS



SCL4051B
Single 8-Channel Multiplexer



SCL4052B
Differential 4-Channel Multiplexer



SCL4053B
Triple 2-Channel Multiplexer

TRUTH TABLE

INPUT STATES				"ON" CHANNELS		
INHIBIT	C	B	A	4051	4052	4053
0	0	0	0	0	Ox, Oy	cx, bx, ax
0	0	0	1	1	1x, 1y	cx, bx, ay
0	0	1	0	2	2x, 2y	cx, by, ax
0	0	1	1	3	3x, 3y	cx, by, ay
0	1	0	0	4		cy, bx, ax
0	1	0	1	5		cy, bx, ay
0	1	1	0	6		cy, by, ax
0	1	1	1	7		cy, by, ay
1	*	*	*	NONE	NONE	NONE

* = Don't care

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS^{1,3}

PARAMETER	CONDITIONS	V _{SS} (Vdc)	V _{DD} (Vdc)	V _{EE} (Vdc)	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
					Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD} V _{IN} =V _{SS} or V _{DD} All valid input combinations	0	+5	0	—	5	—	0.05	5	—	150	μAdc
		0	+10	0	—	10	—	0.1	10	—	300	
			+5	-5								
		0	+15	0	—	20	—	0.2	20	—	600	
MINIMUM INPUT HIGH VOLTAGE (Control and Inhibit Inputs)	V _{IN} V _{is} =V _{EE} V _{os} =V _{DD} I _{os} =10μA	0	5	0	—	3.5	—	2.75	3.5	—	3.5	Vdc
		0	10	0	—	7.0	—	5.5	7.0	—	7.0	
		0	15	0	—	11.0	—	8.25	11.0	—	11.0	
MAXIMUM INPUT LOW VOLTAGE (Control and Inhibit Inputs)	V _{IL} V _{is} =V _{EE} V _{os} =V _{DD} I _{os} =10μA	0	5	0	1.5	—	1.5	2.25	—	1.5	—	Vdc
		0	10	0	3.0	—	3.0	4.5	—	3.0	—	
		0	15	0	4.0	—	4.0	6.75	—	4.0	—	
SWITCH INPUT/ OUTPUT LEAKAGE Any channel OFF	I _{OFF} V _{IN} =V _{SS} or V _{DD} V _{is} =±7.5Vdc	0	+7.5	-7.5	—	±100	—	±0.01	±100	—	±500	nAdc
	All channels OFF I _{OFF} V _{IN} =7.5Vdc V _{is} =±7.5Vdc SCL4051B	0	+7.5	-7.5	—	±400	—	±0.08	±400	—	±1000	nAdc
ON-RESISTANCE C, D, F, H device	R _{ON} V _{IN} =V _{SS} or V _{DD} V _{EE} ≤V _{is} ≤V _{DD} R _L =10kΩ	-7.5	+7.5	-7.5	—	—	—	—	—	—	—	Ω
		0	+15	0	—	220	—	125	280	—	400	
		-5	+5	-5	—	310	—	180	400	—	580	
		0	+10	0	—	—	—	—	—	—	—	
		-2.5	+2.5	-2.5	—	2000	—	470	2500	—	3500	
		0	+5	0	—	—	—	—	—	—	—	
	E device R _{ON} V _{IN} =V _{SS} or V _{DD} V _{EE} ≤V _{is} ≤V _{DD} R _L =10kΩ	-7.5	+7.5	-7.5	—	230	—	125	280	—	360	Ω
		0	+15	0	—	—	—	—	—	—	—	
		-5	+5	-5	—	330	—	180	400	—	520	
		0	+10	0	—	—	—	—	—	—	—	
		-2.5	+2.5	-2.5	—	2100	—	470	2500	—	3200	
		0	+5	0	—	—	—	—	—	—	—	
ON-RESISTANCE MATCH (Same Package)	ΔR _{ON} V _{IN} =V _{SS} or V _{DD} V _{EE} ≤V _{is} ≤V _{DD} R _L =10kΩ	-7.5	+7.5	-7.5	—	—	—	5	—	—	—	Ω
		0	+15	0	—	—	—	—	—	—	—	
		-5	+10	-5	—	—	—	10	—	—	—	
		0	+10	0	—	—	—	—	—	—	—	
		-2.5	+2.5	-2.5	—	—	—	50	—	—	—	
		0	+5	0	—	—	—	—	—	—	—	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

² T_{LOW} = -55°C for C, D, F, H device.

= -40°C for E device.

T_{HIGH} = +125°C for C, D, F, H device.

= + 85°C for E device.

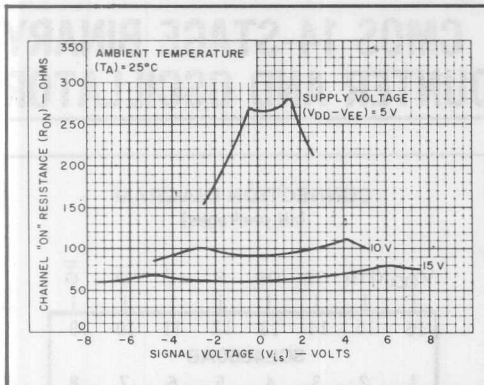
³ These devices have been designed for balanced output drive current specifications. Consult Family Specifications.

ELECTRICAL CHARACTERISTICS (Continued)

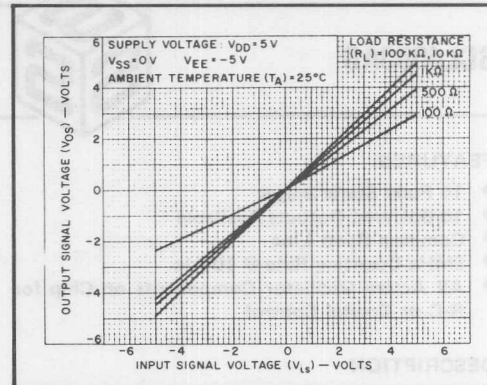
DYNAMIC CHARACTERISTICS ($C_L = 50\text{pF}$, $T_A = 25^\circ\text{C}$)

PARAMETER	CONDITIONS	V_{SS} (Vdc)	V_{DD} (Vdc)	V_{EE} (Vdc)	Min.	Typ.	Max.	Units
SIGNAL INPUTS (V_{is}) AND OUTPUTS (V_{os})								
PROPAGATION DELAY TIME	t_{PLH} t_{PHL}	Inh = V_{SS} $V_{IN} = V_{SS}$ or V_{DD} V_{is} = Square Wave $R_L = 10\text{k}\Omega$	0 0 0	5 10 15	0 0 0	— — —	30 15 12.5	60 30 25 ns
BANDWIDTH (–3dB) (Sine Wave)	BW	Inh = V_{SS} $V_{IN} = V_{SS}$ or V_{DD} $V_{is} = 5V_{p-p}$ centered @ 0.0Vdc	R_L $1\text{k}\Omega$ $10\text{k}\Omega$ $100\text{k}\Omega$ $1\text{M}\Omega$	0 +5 –5	– – – – –	54 40 38 37	— — — —	MHz
INSERTION LOSS ($= 20 \log_{10} \frac{V_{os}}{V_{is}}$)		Inh = V_{SS} $V_{IN} = V_{SS}$ or V_{DD} $V_{is} = 5V_{p-p}$ centered @ 0.0Vdc	R_L $1\text{k}\Omega$ $10\text{k}\Omega$ $100\text{k}\Omega$ $1\text{M}\Omega$	0 +5 –5	– – – – –	2.3 0.2 0.1 0.05	— — — —	dB
SIGNAL DISTORTION (Sine Wave)		Inh = V_{SS} $V_{IN} = V_{SS}$ or V_{DD} $V_{is} = 5V_{p-p}$ centered @ 0.0Vdc $f_{is} = 1.0\text{kHz}$ $R_L = 10\text{k}\Omega$	–7.5 –5 –2.5	+7.5 +5 +2.5	–7.5 –5 –2.5	— — —	0.1 0.2 1.0	— — — %
FEEDTHROUGH (–40dB)		Inh = V_{SS} $V_{IN} = V_{SS}$ or V_{DD} $V_{is} = 5V_{p-p}$ centered @ 0.0Vdc	R_L $1\text{k}\Omega$ $10\text{k}\Omega$ $100\text{k}\Omega$ $1\text{M}\Omega$	0 +5 –5	– – – – –	1250 140 18 2	— — — —	kHz
CROSSTALK (–40dB) Between two switches		Inh = V_{SS} $V_{IN} = V_{SS}$ or V_{DD} $V_{is} = 5V_{p-p}$ centered @ 0.0Vdc $R_L = 1.0\text{k}\Omega$		0 +5 –5	– – –	1.0	—	MHz
CAPACITANCE Input	C_{is}	Inh = V_{DD}	0	+5	–5	—	5	pF
Common	C_{os}	SCL4051B SCL4052B SCL4053B	0	+5	–5	—	30 18 10	pF
Feedthrough	C_{ios}		0	+5	–5	—	0.2	pF
CONTROL INPUTS								
PROPAGATION DELAY TIME ¹	t_{PLH} t_{PHL}	Inh = V_{SS} $V_{EE} \leq V_{is} \leq V_{DD}$ $R_L = 10\text{k}\Omega$	0 0 0 0 –2.5 0	+7.5 +15 +5 +10 +2.5 +5	–7.5 0 –5 0 –2.5 0	— — — — — —	160 120 225 160 400 360	320 240 450 320 800 720 ns
INHIBIT INPUT								
PROPAGATION DELAY TIME	t_{PLH} t_{PHL}	$V_{IN} = V_{SS}$ or V_{DD} $V_{is} = V_{DD}$ $R_L = 10\text{k}\Omega$	0 0 0 0 –2.5 0	+7.5 +15 +5 +10 +2.5 +5	–7.5 0 –5 0 –2.5 0	— — — — — —	160 120 200 160 400 360	320 240 400 320 800 720 ns
INHIBIT RECOVERY TIME ²	t_{rel}	$V_{IN} = V_{SS}$ or V_{DD} $V_{EE} \leq V_{is} \leq V_{DD}$ $R_L = 10\text{k}\Omega$	0 0 0 0 –2.5 0	+7.5 +15 +5 +10 +2.5 +5	–7.5 0 –5 0 –2.5 0	— — — — — —	150 80 200 105 300 225	300 160 400 210 600 450 ns

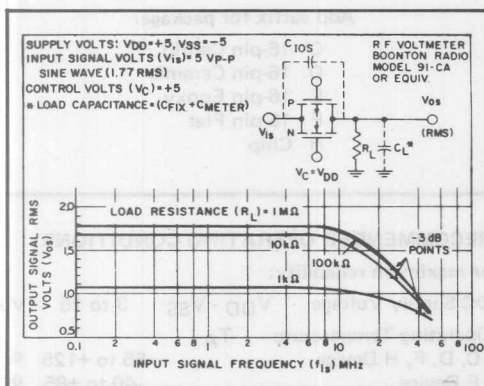
Notes: ¹ Channel Overlap time — interval following change of control input during which two channels may be ON simultaneously.² Interval following removal of Inhibit during which channel information is invalid.



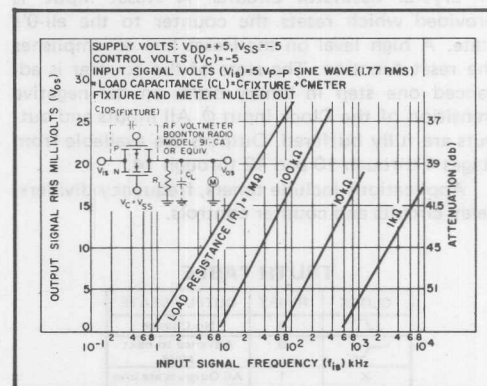
Typical Channel "ON" resistance vs. signal voltage



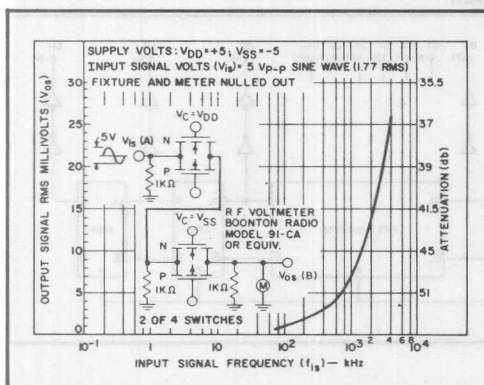
Typical "ON" characteristics



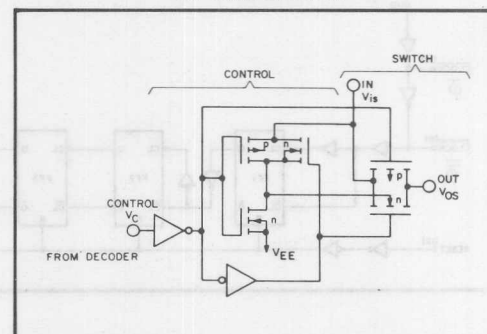
Typ. switch frequency response-switch "ON"



Typ. feedthru vs. freq. — switch "OFF"



Typ. crosstalk between switch circuits in the same package

SCHEMATIC DIAGRAM
OF ONE SWITCH

SCL4060AB



CMOS 14-STAGE BINARY COUNTER AND OSCILLATOR

FEATURES

- ◆ 14 Fully Static Stages
- ◆ 10 Buffered Outputs Available
- ◆ Common Reset Line
- ◆ 8MHz Counting Rate @ 10Vdc
- ◆ All Active Oscillator Components on Chip for R-C or Crystal Control

DESCRIPTION

The SCL4060AB consists of an oscillator section and 14 ripple-carry binary counter stages. The oscillator configuration allows design of either R-C or crystal oscillator circuits. A Reset input is provided which resets the counter to the all-0's state. A high level on the Reset line accomplishes the reset function. The state of the counter is advanced one step in binary order on the negative transition of the Clock input ϕ . All inputs and outputs are fully buffered. Outputs are available from stages 4 through 10 and 12 through 14.

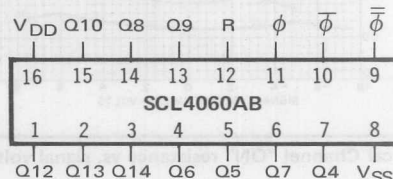
Applications include timers, frequency dividers, delay circuits and counter controls.

TRUTH TABLE

CLOCK	RESET	OUTPUT STATE
	0	No Change
	0	Advance to next state
X	1	All Outputs are low

X = Don't Care

CONNECTION DIAGRAM (all packages)



Add suffix for package:

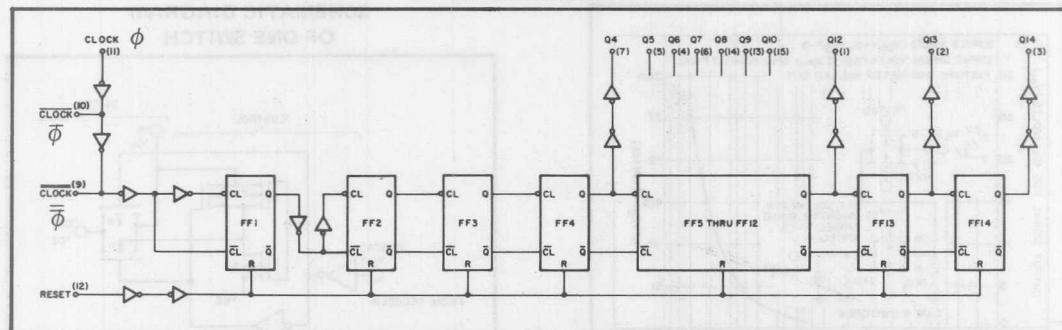
- C 16-pin Cerdip
- D 16-pin Ceramic
- E 16-pin Epoxy
- F 16-pin Flat
- H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A	-55 to +125	°C
C, D, F, H Device		-40 to +85	°C
E Device			

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS¹

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	5 V _{IN} =V _{SS} or V _{DD}	—	5	—	0.05	5	—	150	μAdc
		10 All valid input combinations	—	10	—	0.1	10	—	300	
		15	—	15	—	0.2	20	—	600	
OUTPUT HIGH (SOURCE) CURRENT C, D, F, H device	I _{OH}	5 V _{OH} =4.6V	-0.15	—	-0.12	-0.5	—	-0.08	—	mAdc
		10 V _{OH} =9.5V	-0.37	—	-0.3	-1.15	—	-0.21	—	
		15 V _{OH} =13.5V	-1.25	—	-1.0	-4.5	—	-0.69	—	
		V _{IN} =V _{SS} or V _{DD}								
		5 V _{OH} =4.6V	-0.14	—	-0.12	-0.5	—	-0.10	—	
		10 V _{OH} =9.5V	-0.35	—	-0.3	-1.15	—	-0.25	—	
E device		15 V _{OH} =13.5V	-1.2	—	-1.0	-4.5	—	-0.85	—	mAdc
		V _{IN} =V _{SS} or V _{DD}								
OUTPUT LOW (SINK) CURRENT C, D, F, H device	I _{OL}	5 V _{OL} =0.4V	0.15	—	0.12	0.5	—	0.08	—	mAdc
		10 V _{OL} =0.5V	0.37	—	0.3	1.0	—	0.21	—	
		15 V _{OL} =1.5V	1.25	—	1.0	5.8	—	0.69	—	
		V _{IN} =V _{SS} or V _{DD}								
		5 V _{OL} =0.4V	0.14	—	0.12	0.5	—	0.10	—	mAdc
		10 V _{OL} =0.5V	0.35	—	0.3	1.0	—	0.25	—	
E device		15 V _{OL} =1.5V	1.2	—	1.0	5.8	—	0.85	—	
		V _{IN} =V _{SS} or V _{DD}								

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

² T_{LOW} = -55°C for C, D, F, H device.

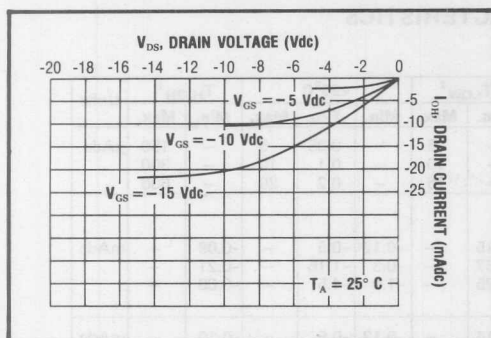
= -40°C for E device.

T_{HIGH} = +125°C for C, D, F, H device.

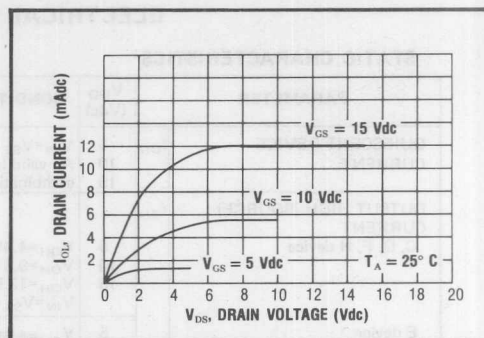
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V _{DD} (Vdc)	Min.	Typ.	Max.	Units	
CLOCKED OPERATION							
PROPAGATION DELAY TIME Clock to Q4	t _{PLH} , t _{PHL}	5	—	650	1300	ns	
		10	—	325	650		
		15	—	260	520		
	Q _i to Q _i + 1	t _{PLH} , t _{PHL}	5	—	150	300	ns
			10	—	75	150	
			15	—	60	120	
OUTPUT TRANSITION TIME	t _{TLH} , t _{THL}	5	—	180	360	ns	
		10	—	90	180		
		15	—	65	130		
MINIMUM CLOCK PULSE WIDTH	PW _{CL}	5	—	100	200	ns	
		10	—	50	100		
		15	—	40	80		
MAXIMUM CLOCK FREQUENCY	f _{CL}	5	2.0	4.0	—	MHz	
		10	4.0	8.0	—		
		15	5	10	—		
MAXIMUM CLOCK RISE AND FALL TIME	t _{rCL} , t _{fCL}	5	15	—	—	μs	
		10	15	—	—		
		15	5	—	—		
RESET OPERATION							
PROPAGATION DELAY TIME	t _{PHL}	5	—	300	600	ns	
		10	—	150	300		
		15	—	120	240		
MINIMUM RESET PULSE WIDTH	PW _R	5	—	150	300	ns	
		10	—	75	150		
		15	—	60	120		
RESET REMOVAL TIME	t _{rem}	5	—	250	500	ns	
		10	—	125	250		
		15	—	100	200		

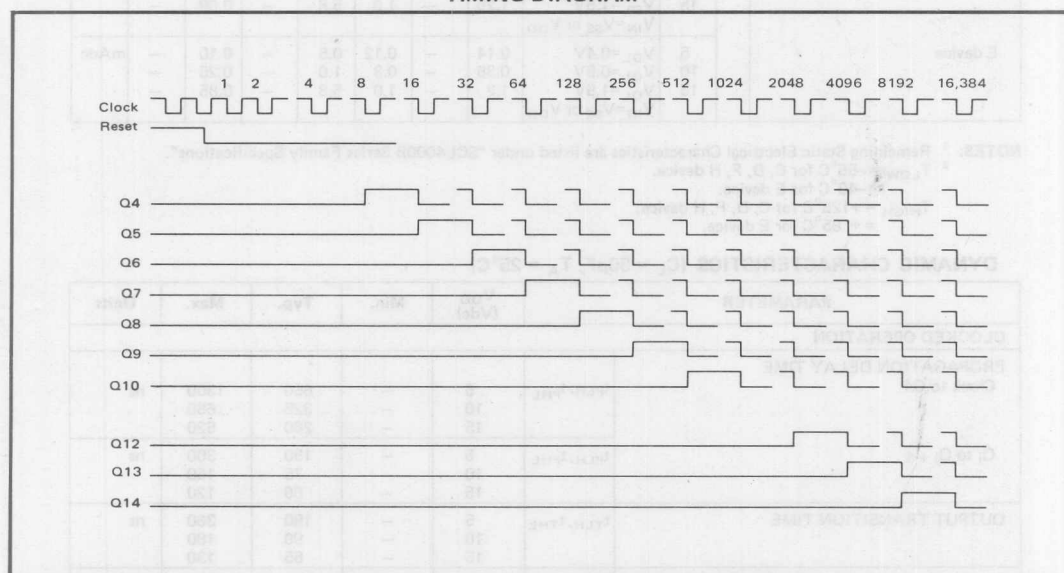


Typical P-Channel
Source Current Characteristics

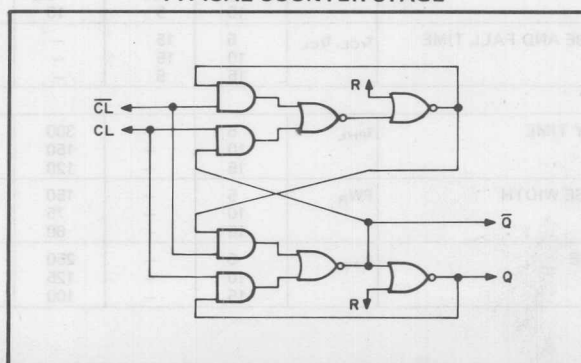


Typical N-Channel
Sink Current Characteristics

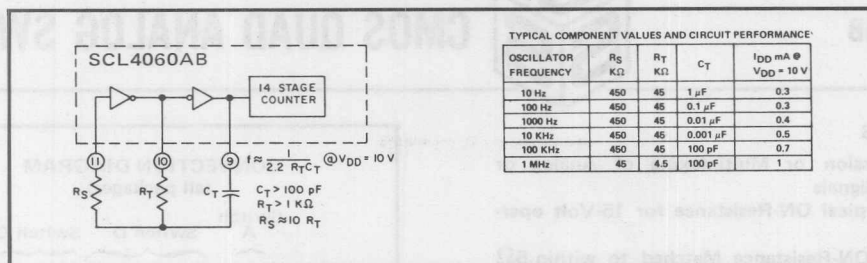
TIMING DIAGRAM



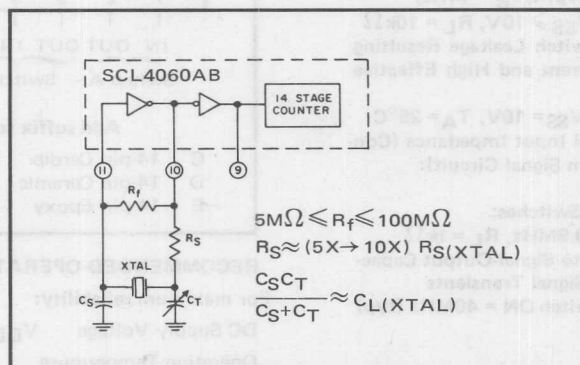
TYPICAL COUNTER STAGE



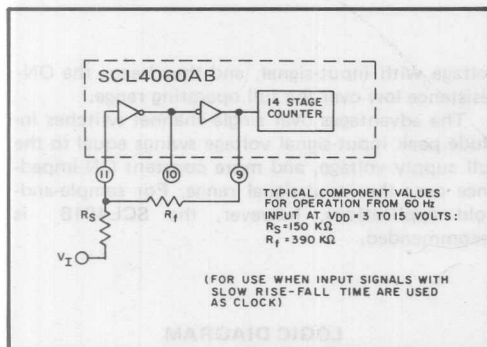
APPLICATIONS INFORMATION



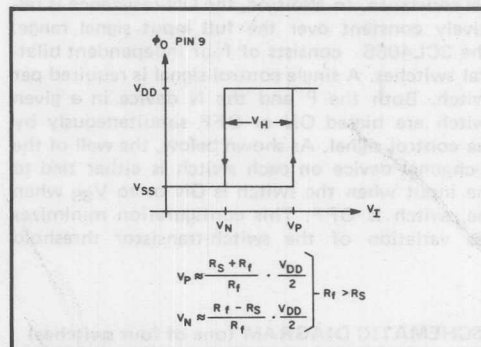
Typical RC oscillator circuit



Typical crystal oscillator circuit



Input pulse-shaping circuit (Schmitt trigger)



Input circuit characteristics for pulse-shaping circuit.



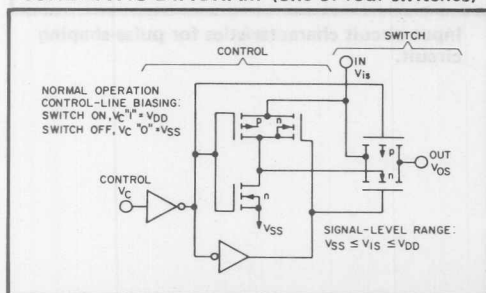
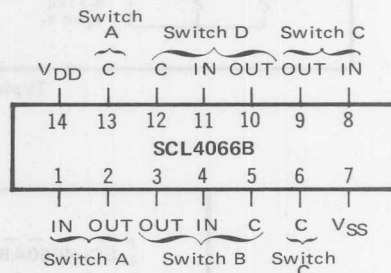
FEATURES

- ◆ Transmission or Multiplexing of Analog or Digital Signals
- ◆ 80Ω Typical ON-Resistance for 15-Volt operation
- ◆ Switch ON-Resistance Matched to within 5Ω over 15-Volt Signal-Input Range
- ◆ ON-Resistance Flat over Full Peak-to-Peak Signal Range
- ◆ High Degree of Linearity:
 $\leq 0.5\%$ Distortion (typ) @ $f_{is} = 1\text{kHz}$,
 $V_{is} = 5V_{p-p}$, $V_{DD} - V_{SS} \geq 10V$, $R_L = 10k\Omega$
- ◆ Extremely Low OFF switch Leakage Resulting in very Low Offset Current and High Effective OFF Resistance:
 $10pA$ (typ) @ $V_{DD} - V_{SS} = 10V$, $T_A = 25^\circ C$
- ◆ Extremely High Control Input Impedance (Control Circuit Isolated from Signal Circuit):
 $10^{12}\Omega$ (typ)
- ◆ Low Crosstalk between Switches:
 $-50dB$ (typ) @ $f_{is} = 0.9MHz$, $R_L = 1k\Omega$
- ◆ Matched Control-Input to Signal-Output Capacitance Reduces Output Signal Transients
- ◆ Frequency Response, Switch ON = $40MHz$ (typ)

DESCRIPTION

The SCL4066B is a Quad Bilateral Switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with the SCL4016B, but exhibits a much lower ON-resistance. In addition, the ON-resistance is relatively constant over the full input signal range. The SCL4066 consists of four independent bilateral switches. A single control signal is required per switch. Both the P and the N device in a given switch are biased ON or OFF simultaneously by the control signal. As shown below, the well of the N-channel device on each switch is either tied to the input when the switch is ON or to V_{SS} when the switch is OFF. This configuration minimizes the variation of the switch-transistor threshold

SCHEMATIC DIAGRAM (one of four switches)

CONNECTION DIAGRAM
(all packages)

Add suffix for package:

C	14-pin Cerdip	F	14-pin Flat
D	14-pin Ceramic	H	Chip
E	14-pin Epoxy		

RECOMMENDED OPERATING CONDITIONS

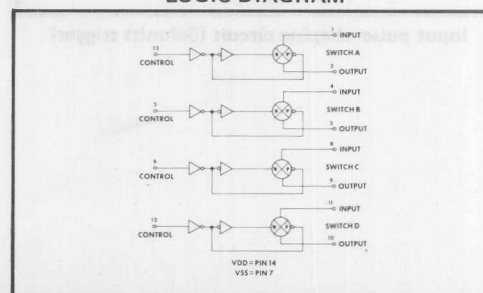
For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A	-55 to +125	$^\circ C$
C, D, F, H Device		-40 to +85	$^\circ C$
E Device			

voltage with input-signal, and thus keeps the ON-resistance low over the full operating range.

The advantages over single-channel switches include peak input-signal voltage swings equal to the full supply voltage, and more constant ON-impedance over the input-signal range. For sample-and-hold applications, however, the SCL4016 is recommended.

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS^{1, 3}

PARAMETER		CONDITIONS	V _{SS} (Vdc)	V _{DD} (Vdc)	T _{LOW} ²		25°C			T _{HIGH} ²		Units
					Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	V _{IN} = V _{SS} or V _{DD} All valid input combinations	0	5	—	0.05	—	0.0005	0.05	—	1.5	μAdc
			0	10	—	0.1	—	0.001	0.1	—	3.0	
			0	15	—	0.2	—	0.002	0.2	—	6.0	
MINIMUM INPUT HIGH VOLTAGE (Control Input)	V _{IH}	V _{IS} = V _{SS} V _{OS} = V _{DD} I _{OS} = 10μA	0	5	—	4.0	—	2.75	4.0	—	4.0	Vdc
			0	10	—	8.0	—	5.5	8.0	—	8.0	
			0	15	—	12.0	—	8.25	12.0	—	12.0	
MAXIMUM INPUT LOW VOLTAGE (Control Input)	V _{IL}	V _{IS} = V _{SS} V _{OS} = V _{DD} I _{OS} = 10μA	0	5	1.0	—	1.0	2.25	—	1.0	—	Vdc
			0	10	2.0	—	2.0	4.5	—	2.0	—	
			0	15	3.0	—	3.0	6.75	—	3.0	—	
SWITCH INPUT/OUTPUT LEAKAGE	I _{OFF}	V _C = V _{SS} V _{IS} = ±7.5Vdc	-7.5	+7.5	—	±100	—	±0.01	±100	—	±200	nAdc
ON-RESISTANCE C,D,F,H device	R _{ON}	V _C = V _{DD} V _{SS} ≤ V _{IS} ≤ V _{DD} R _L = 10kΩ	-7.5	+7.5	—	220	—	80	280	—	320	Ω
			-5	+5	—	310	—	120	400	—	550	Ω
			-2.5	+2.5	—	2000	—	270	2500	—	3500	Ω
E device	R _{ON}	V _C = V _{DD} V _{SS} ≤ V _{IS} ≤ V _{DD} R _L = 10kΩ	-7.5	+7.5	—	250	—	80	280	—	300	Ω
			-5	+5	—	330	—	120	400	—	520	Ω
			-2.5	+2.5	—	2100	—	270	2500	—	3200	Ω
ON-RESISTANCE MATCH (Same package)	ΔR _{ON}	V _C = V _{DD} V _{SS} ≤ V _{IS} ≤ V _{DD} R _L = 10kΩ	-7.5	+7.5	—	—	—	5	—	—	—	Ω
			-5	+5	—	—	—	10	—	—	—	Ω
			-2.5	+2.5	—	—	—	10	—	—	—	Ω

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

² T_{LOW} = -55°C for C, D, F, H device.

= -40°C for E device.

T_{HIGH} = +125°C for C, D, F, H device.

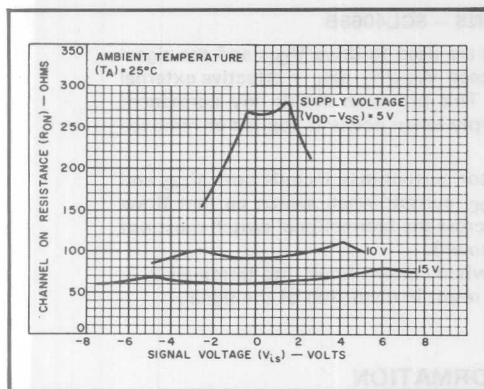
= + 85°C for E device.

³ This device has been designed for balanced output drive current specifications. Consult Family Specifications.

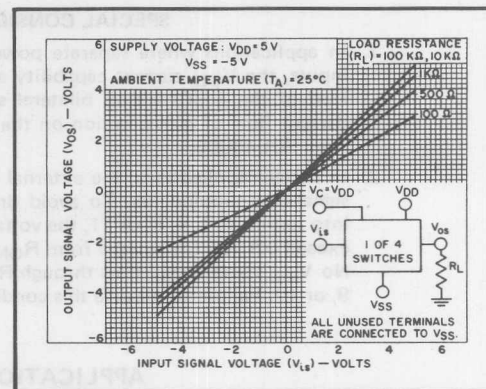
ELECTRICAL CHARACTERISTICS (Continued)

DYNAMIC CHARACTERISTICS ($C_L = 50\text{pF}$, $T_A = 25^\circ\text{C}$)

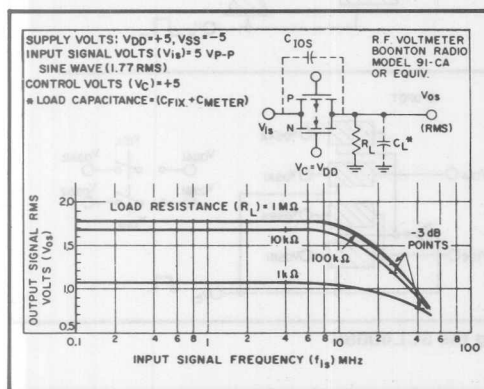
PARAMETER	CONDITIONS	V_{SS} (Vdc)	V_{DD} (Vdc)	Min.	Typ.	Max.	Units
SIGNAL INPUTS (V_{is}) AND OUTPUTS (V_{os})							
PROPAGATION DELAY TIME Signal Input to Signal Output	t_{PLH} , t_{PHL} $V_c = V_{DD}$ $V_{is} = \text{Square Wave}$ $R_L = 10\text{k}\Omega$	0 0 0	5 10 15	— — —	20 10 7.5	40 20 15	ns
BANDWIDTH (~3dB) (Sine Wave)	BW $V_c = V_{DD}$ $V_{is} = 5V_{p-p}$ centered @ 0.0Vdc R_L	— — — — —	— +5 — — —	— — — — —	— 54 40 38 37	— — — — —	MHz
INSERTION LOSS $(= 20 \log_{10} \frac{V_{os}}{V_{is}})$	$V_c = V_{DD}$ $V_{is} = 5V_{p-p}$ centered @ 0.0Vdc R_L	— — — — —	— +5 — — —	— — — — —	— 2.3 0.2 0.1 0.05	— — — — —	dB
SIGNAL DISTORTION (Sine Wave)	$V_c = V_{DD}$ $V_{is} = 5V_{p-p}$ centered @ 0.0Vdc $f_{is} = 1.0\text{kHz}$ $R_L = 10\text{k}\Omega$	— — — — —	— +5 — — —	— — — — —	— 0.16 — — —	— — — — —	%
FEEDTHROUGH (~50dB)	$V_c = V_{SS}$ $V_{is} = 5V_{p-p}$ centered @ 0.0Vdc R_L	— — — — —	— +5 — — —	— — — — —	— 1250 140 18 2	— — — — —	kHz
CROSSTALK (~50dB) Between two switches	$V_c(A) = V_{DD}$ $V_c(B) = V_{SS}$ $V_{is}(A) = 5V_{p-p}$ centered @ 0.0Vdc $R_L = 10\text{k}\Omega$	— — — — —	— +5 — — —	— — — — —	— 0.9 — — —	— — — — —	MHz
CAPACITANCE Input	C_{is}	— — —	— +5 —	— — —	— 8 —	— — —	pF
Output Feedthrough	C_{os} C_{ios} $V_c = V_{SS}$	— — —	— +5 —	— — —	— 8 0.5	— — —	pF
CONTROL INPUT (V_c)							
PROPAGATION DELAY TIME Turn on	t_{PC} $V_{SS} \leq V_{is} \leq V_{DD}$ $R_L = 10\text{k}\Omega$	0 0 0	5 10 15	— — —	50 25 20	100 50 40	ns
MAXIMUM INPUT FREQUENCY	f_c $V_{SS} \leq V_{is} \leq V_{DD}$ $R_L = 1.0\text{k}\Omega$	0 0 0	5 10 15	— — —	5 10 12	— — —	MHz
CROSSTALK (To signal port)	$V_c = \text{Square Wave}$ $R_L = 10\text{k}\Omega$ $R_{in} = 1.0\text{k}\Omega$	0 0 0	5 10 15	— — —	30 50 100	— — —	mV



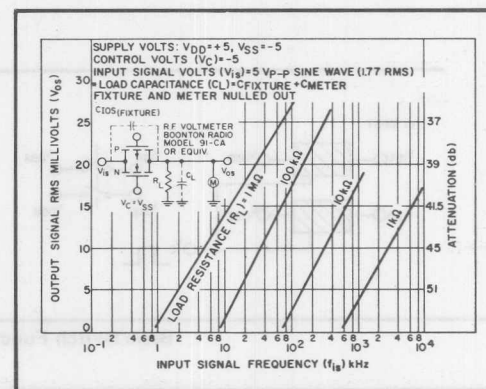
Typical channel ON resistance vs. signal voltage for three values of supply voltage ($V_{DD}-V_{SS}$)



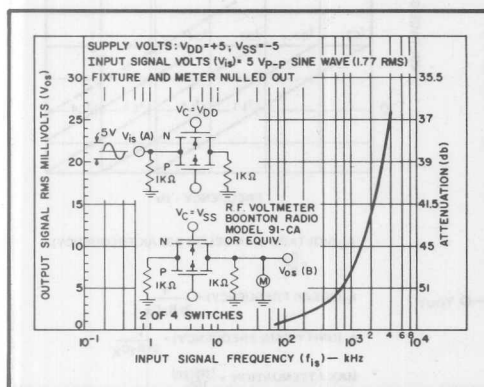
Typical ON characteristics for 1 of 4 channels.



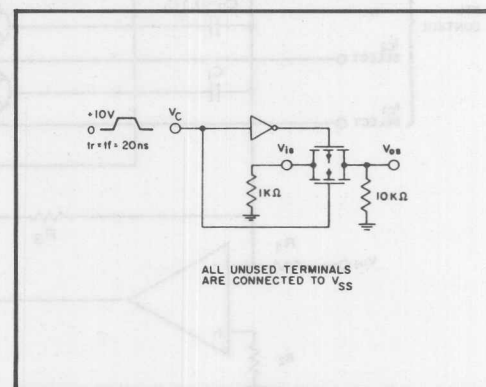
Typ. switch frequency response - switch "ON"



Typ. feedthru vs. freq. - switch "OFF"



Typ. crosstalk between switch circuits in the same package

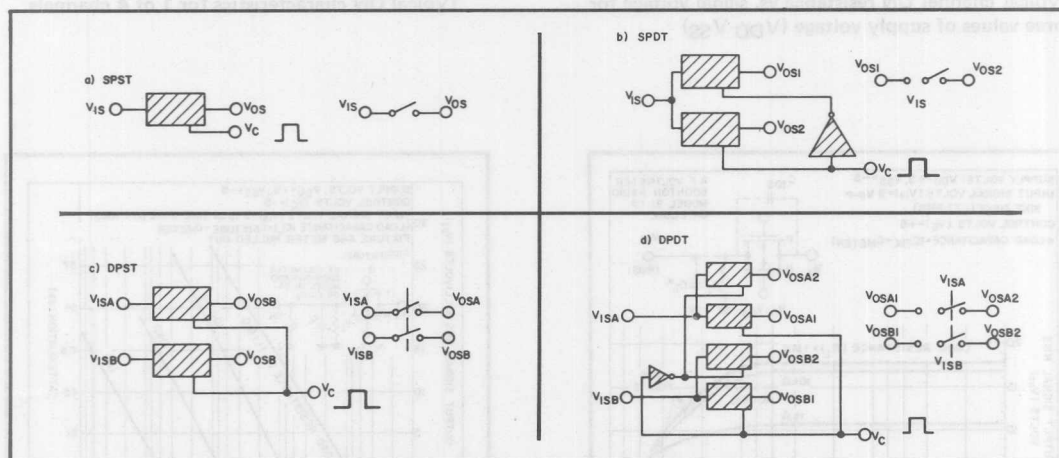


Test circuit, crosstalk-control input to signal output

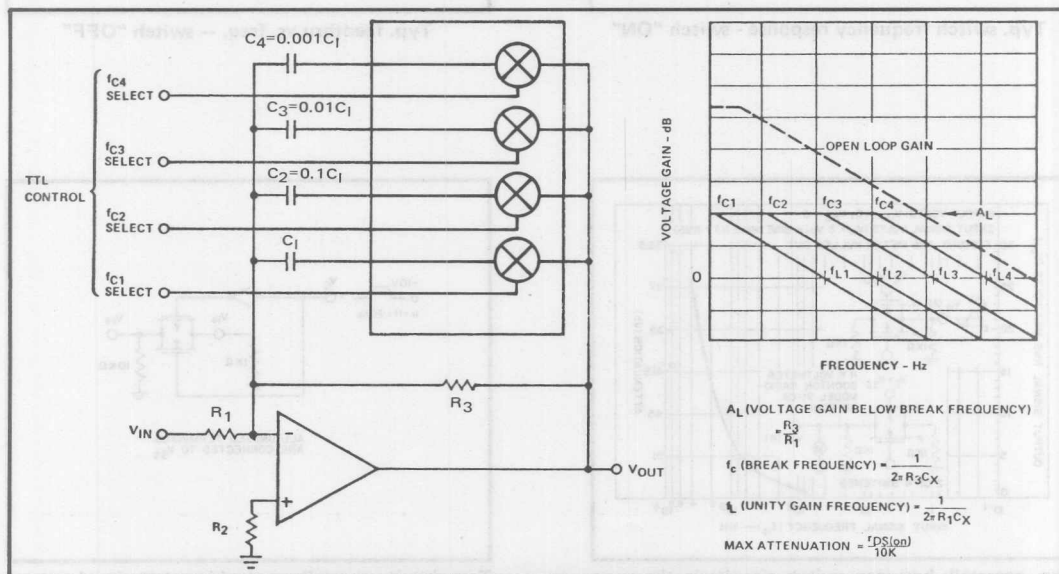
SPECIAL CONSIDERATIONS – SCL4066B

1. In applications where separate power sources are used to drive V_{DD} and the signal inputs, the V_{DD} current capability should exceed V_{DD}/R_L (R_L = effective external load of the 4 SCL4066B bilateral switches). This provision avoids any permanent current flow or clamp action on the V_{DD} supply when power is applied or removed from SCL4066B.
2. In certain applications, the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into terminals 1, 4, 8, or 11, the voltage drop across the bidirectional switch must not exceed 0.8 volt (calculated from R_{ON} values shown). No V_{DD} current will flow through R_L if the switch current flows into terminals 2, 3, 9, or 10. Failure to observe this condition may result in distortion of the signal.

APPLICATIONS INFORMATION



Basic Switch Functions using the SCL4066B



Active Low Pass Filter with Digitally Selected Break Frequency



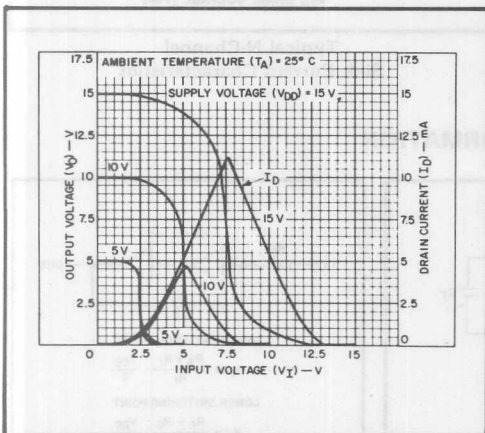
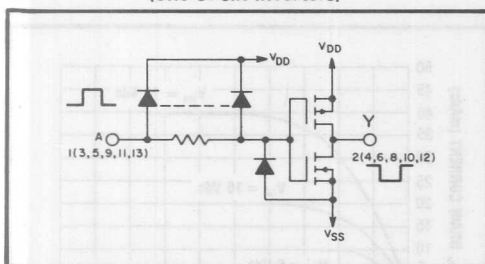
FEATURES

- ◆ Fully "B"-Series Compatible
- ◆ Diode Protection on all Inputs
- ◆ Balanced Output Drive Current Specifications
- ◆ Pin Compatible with 74C04

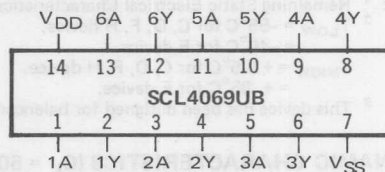
DESCRIPTION

The SCL4069UB consists of six CMOS inverter circuits. The device is intended for general-purpose inverter applications where the higher output drive and level-shifting feature of the SCL4009UB and SCL4049UB are not required.* The SCL4069UB is particularly useful for quasi-linear circuits such as oscillators (See Applications Information).

*For pin-to-pin compatibility with the SCL4009UB and SCL4049UB, the SCL4449UB is available.

SCHEMATIC DIAGRAM
(one of six inverters)

Typical current and voltage transfer characteristics

CONNECTION DIAGRAM
(all packages)

Add suffix for package:

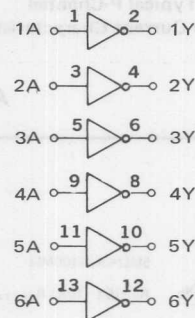
- C 14-pin Cerdip
- D 14-pin Ceramic
- E 14-pin Epoxy
- F 14-pin Flat
- H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

LOGIC DIAGRAM



$V_{SS} = 7$
 $V_{DD} = 14$

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS^{1,3}

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	V _{IN} =V _{SS} or V _{DD} All valid input combinations	—	0.05	—	0.0005	0.05	—	1.5	μAdc
			—	0.10	—	0.001	0.10	—	3.0	
			—	0.20	—	0.002	0.20	—	6.0	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

² T_{LOW} = -55°C for C, D, F, H device.

= -40°C for E device.

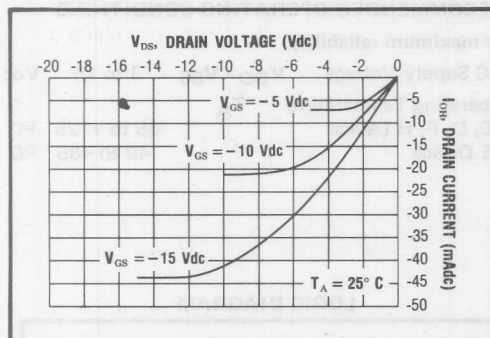
T_{HIGH} = +125°C for C, D, F, H device.

= + 85°C for E device.

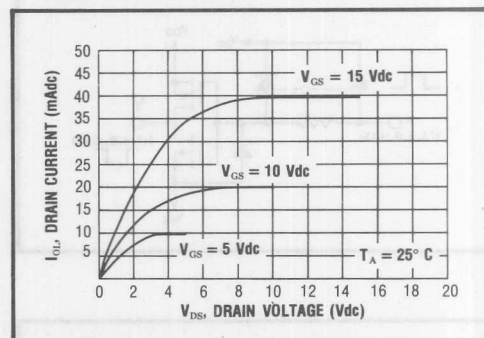
³ This device has been designed for balanced output drive current specifications. Consult Family Specifications.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V _{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME	t _{PLH} , t _{PHL}	5	—	60	120	ns
		10	—	30	60	
		15	—	25	50	
OUTPUT TRANSITION TIME	t _{TLH} , t _{THL}	5	—	100	200	ns
		10	—	50	100	
		15	—	40	80	

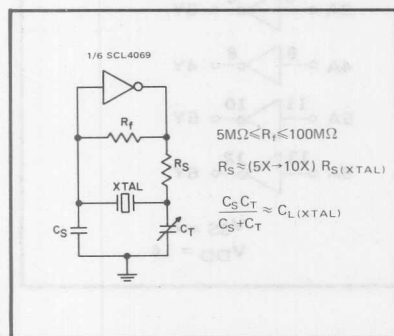


Typical P-Channel
Source Current Characteristics

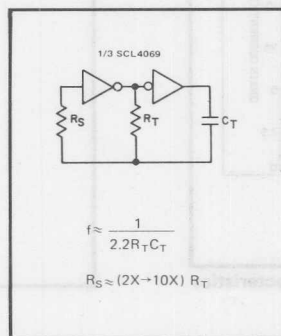


Typical N-Channel
Sink Current Characteristics

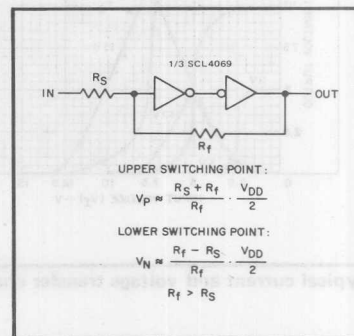
APPLICATIONS INFORMATION



Typical crystal oscillator circuit



Typical RC oscillator circuit



Input pulse shaping circuit (Schmitt
Trigger)



CMOS QUAD EXCLUSIVE-OR GATE

FEATURES

- ◆ Buffered Outputs
- ◆ Diode Protection on all Inputs
- ◆ Fully "B"-Series Compatible
- ◆ Balanced Output Drive Current Specifications
- ◆ Pin Compatible with 4030 types, MC14507, 74C86

DESCRIPTION

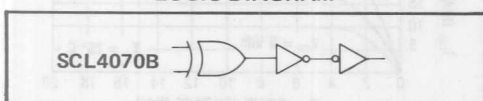
The SCL4070B contains four independent exclusive-OR gates integrated on a single monolithic silicon chip. Each exclusive-OR gate consists of five N-channel and five P-channel enhancement-mode transistors, plus output buffering devices.

TRUTH TABLE
(one of four gates)

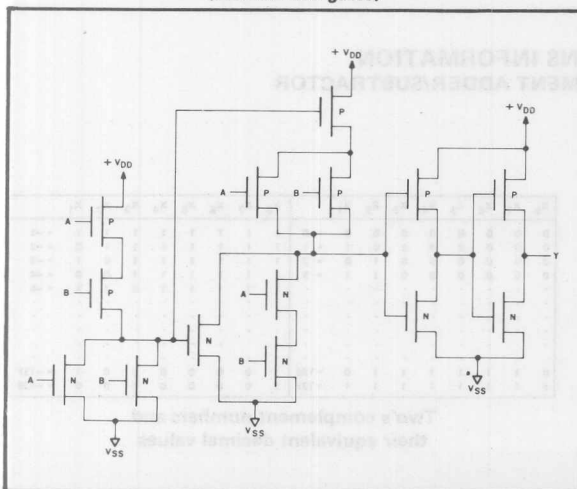
A	B	Y
0	0	0
1	0	1
0	1	1
1	1	0

Where 1 = High Level
0 = Low Level

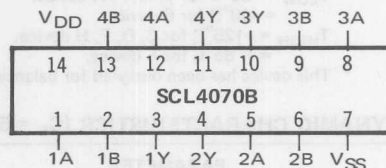
LOGIC DIAGRAM



SCHEMATIC DIAGRAM
(one of four gates)



CONNECTION DIAGRAM
(all packages)



Add suffix for package:

- C 14-pin Cerdip
- D 14-pin Ceramic
- E 14-pin Epoxy
- F 14-pin Flat
- H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage $V_{DD} - V_{SS}$ 3 to 15 Vdc

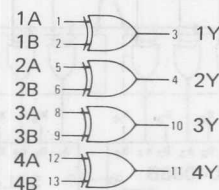
Operating Temperature T_A

C, D, F, H Device -55 to +125 °C

E Device -40 to +85 °C

Note: The SCL4070B is identical to the SCL4030B; the devices are fully interchangeable in all applications.

FUNCTION DIAGRAM



$$Y = A \oplus B$$

V_{DD} = Pin 14

V_{SS} = Pin 7

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS^{1,3}

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	5	—	0.05	—	0.0005	0.05	—	1.5	μAdc
		10	—	0.10	—	0.001	0.10	—	3.0	
		15	—	0.20	—	0.002	0.20	—	6.0	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

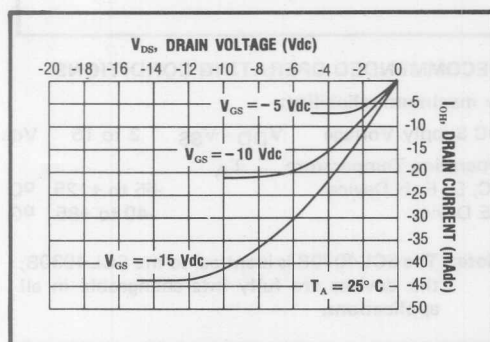
² T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.

T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

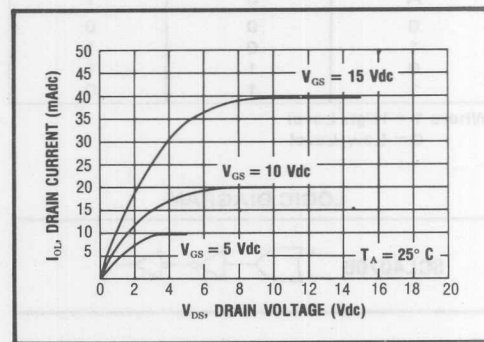
³ This device has been designed for balanced output drive current specifications. Consult Family Specifications.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

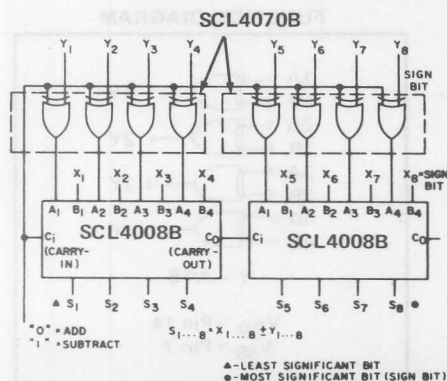
PARAMETER		V _{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME	t _{PLH} , t _{PHL}	5	—	175	350	ns
		10	—	70	140	
		15	—	50	100	
OUTPUT TRANSITION TIME	t _{TLH} , t _{THL}	5	—	100	200	ns
		10	—	50	100	
		15	—	40	80	



Typical P-Channel
Source Current Characteristics



Typical N-Channel
Sink Current Characteristics

APPLICATIONS INFORMATION
8-BIT TWO'S COMPLEMENT ADDER/SUBTRACTOR

X ₈	X ₇	X ₆	X ₅	X ₄	X ₃	X ₂	X ₁	X ₈	X ₇	X ₆	X ₅	X ₄	X ₃	X ₂	X ₁
0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0
0	0	0	0	0	0	1	0	1	1	1	1	1	1	0	1
0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0
0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	1
0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	1
0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0

Two's complement numbers and
their equivalent decimal values

SCL4071B, SCL4072B SCL4075B



CMOS OR GATES

SCL4071B - Quad 2-Input OR
SCL4072B - Dual 4-Input OR
SCL4075B - Triple 3-Input OR

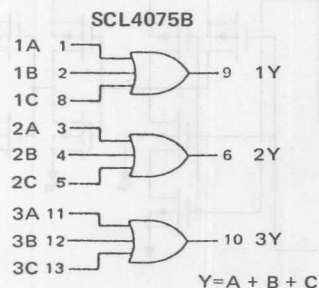
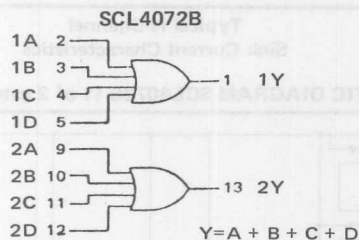
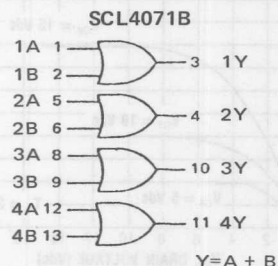
FEATURES

- ◆ Buffered Outputs
- ◆ Diode Protection on all Inputs
- ◆ Fully "B"-Series Compatible
- ◆ Balanced Output Drive Current Specifications

TRUTH TABLE

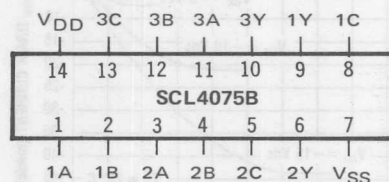
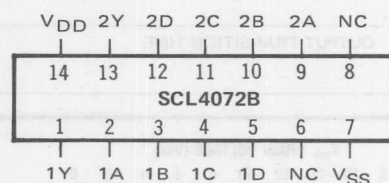
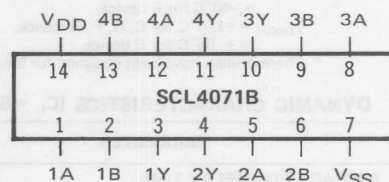
Inputs	Output
00 . . . 0	0
All other combinations	1

FUNCTION DIAGRAMS



V_{DD} = Pin 14
 V_{SS} = Pin 7
for all Devices

CONNECTION DIAGRAMS (all packages)



Add suffix for package:

- C 14-pin Cerdip
- D 14-pin Ceramic
- E 14-pin Epoxy
- F 14-pin Flat
- H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	V _{dc}
Operating Temperature	T_A	-55 to +125	°C
C, D, F, H Device		-40 to +85	°C
E Device			

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS^{1,3}

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	V _{IN} =V _{SS} or V _{DD}	—	0.05	—	0.0005	0.05	—	1.5	μAdc
	10	All valid input combinations	—	0.10	—	0.001	0.10	—	3.0	
	15		—	0.20	—	0.002	0.20	—	6.0	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

² T_{LOW} = -55°C for C, D, F, H device.

= -40°C for E device.

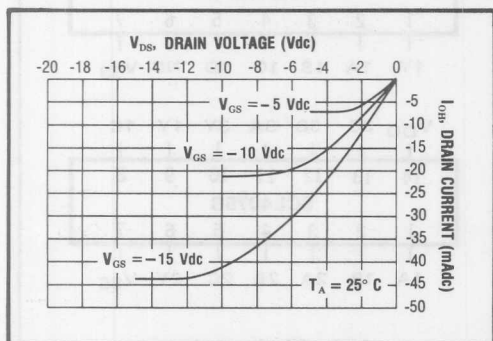
T_{HIGH} = +125°C for C, D, F, H device.

= + 85°C for E device.

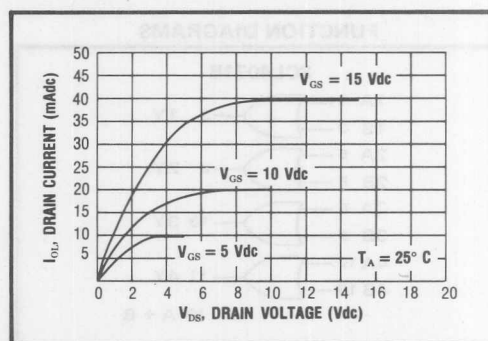
³ These devices have been designed for balanced output drive current specifications. Consult Family Specifications.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V _{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME	t _{PLH} , t _{PHL}	5	—	150	300	ns
		10	—	65	130	
		15	—	50	100	
OUTPUT TRANSITION TIME	t _{TLH} , t _{THL}	5	—	100	200	ns
		10	—	50	100	
		15	—	40	80	

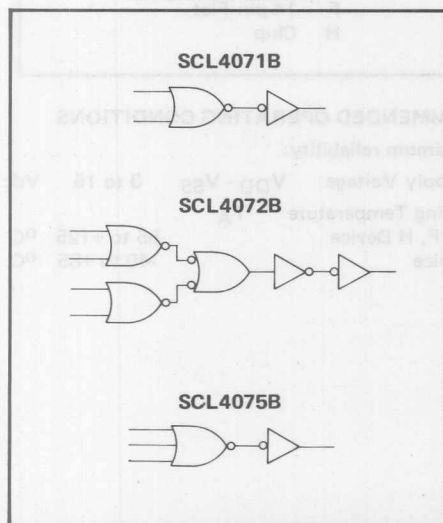


Typical P-Channel
Source Current Characteristics

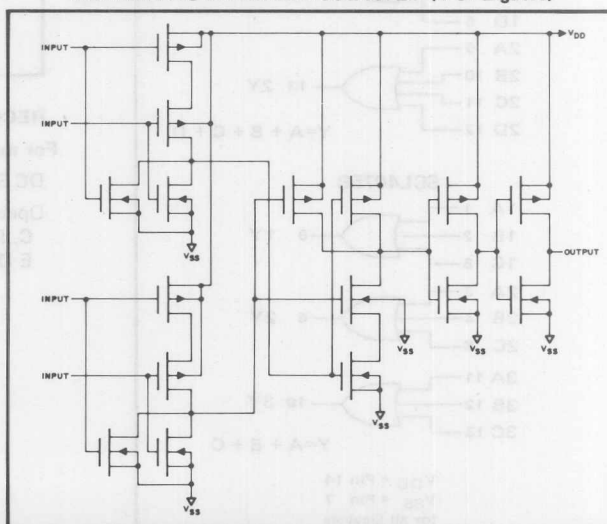


Typical N-Channel
Sink Current Characteristics

LOGIC DIAGRAMS



SCHEMATIC DIAGRAM SCL4072B (1 of 2 gates)





FEATURES

- ◆ 3-State Outputs with Gated Control Lines
- ◆ Fully Independent Clock
- ◆ Asynchronous Reset
- ◆ Fully Static Operation - DC to 12MHz @ 10Vdc
- ◆ Balanced Output Drive Current Specifications

DESCRIPTION

The SCL4076B 4-bit Register consists of four D-Type flip-flops operating synchronously from a common Clock. OR-gated Output Disable inputs force the outputs into a high-impedance state for use in bus-organized systems. OR-gated Data Disable inputs cause the Q outputs to be fed back to the D inputs of the flip-flops. Thus, they are inhibited from changing state while the clocking process remains undisturbed. An asynchronous Master Reset is provided to clear all four flip-flops simultaneously independent of the Clock or Disable inputs.

TRUTH TABLE

Reset	Clock	Data Input Disable		Data D	Next State Output Q	
		G1	G2			
1	X	X	X	X	0	
0	0	X	X	X	Q	NC
0		1	X	X	Q	NC
0		X	1	X	Q	NC
0		0	0	1	1	
0		0	0	0	0	
0	1	X	X	X	Q	NC
0		X	X	X	Q	NC

When either Output Disable M or N is high, the outputs are disabled (high impedance state); however sequential operation of the flip-flops is not affected.

1 $\equiv$ High Level

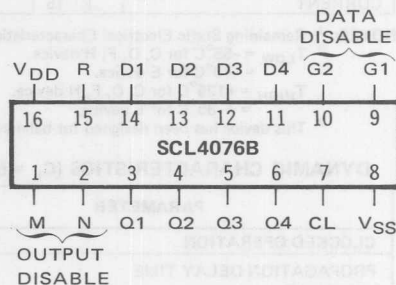
0 $\equiv$ Low Level

X = Don't Care

NC = No Change

CONNECTION DIAGRAM

(all packages)



Add suffix for package:

- C 16-pin Cerdip
- D 16-pin Ceramic
- E 16-pin Epoxy
- F 16-pin Flat
- H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

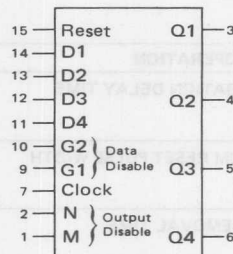
DC Supply Voltage $V_{DD} - V_{SS}$ 3 to 15 Vdc

Operating Temperature T_A

C, D, F, H Device -55 to +125 °C

E Device -40 to +85 °C

BLOCK DIAGRAM



V_{DD} = Pin 16
 V_{SS} = Pin 8

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS^{1, 3}

PARAMETER		V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	5	V _{IN} =V _{SS} or V _{DD} All valid input combinations	—	5	—	0.05	5	—	150	μAdc
		10		—	10	—	0.1	10	—	300	
		15		—	20	—	0.2	20	—	600	
3-STATE OUTPUT LEAKAGE CURRENT	I _{ZL}	15		—	±0.1	—	±10 ⁻⁴	±0.1	—	±1.0	μAdc

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

² T_{LOW} = -55°C for C, D, F, H device.

= -40°C for E device.

T_{HIGH} = +125°C for C, D, F, H device.

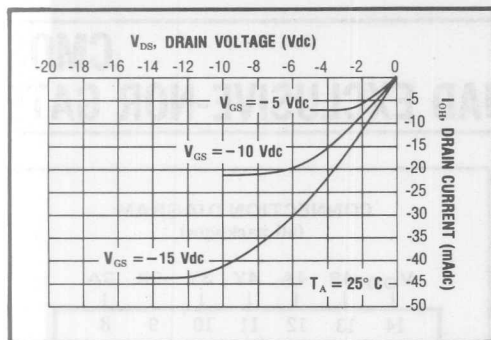
= + 85°C for E device.

³ This device has been designed for balanced output drive current specifications. Consult Family Specifications.

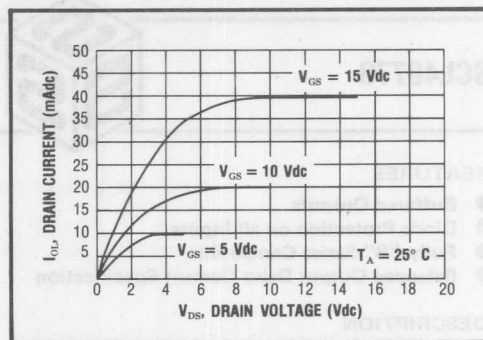
DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V _{DD} (Vdc)	Min.	Typ.	Max.	Units	
CLOCKED OPERATION							
PROPAGATION DELAY TIME Clock to Q	t _{PLH} , t _{PHL}	5	—	150	300	ns	
		10	—	70	140		
		15	—	45	90		
	Output Disable to Q	t _{PHZ} , t _{PLZ}	5	—	75	150	ns
			10	—	40	80	
			15	—	30	60	
		t _{PZH} , t _{PZL}	5	—	80	160	ns
			10	—	35	70	
			15	—	25	50	
OUTPUT TRANSITION TIME	t _{TLH} , t _{THL}	5	—	100	200	ns	
		10	—	50	100		
		15	—	40	80		
MINIMUM CLOCK PULSE WIDTH	PW _{CL}	5	—	80	160	ns	
		10	—	40	80		
		15	—	30	60		
MAXIMUM CLOCK FREQUENCY	f _{CL}	5	3.0	6.0	—	MHz	
		10	6.0	12	—		
		15	8.0	16	—		
MAXIMUM CLOCK RISE & FALL TIME ¹	t _{rCL} , t _{fCL}	5	15	—	—	μs	
		10	15	—	—		
		15	15	—	—		
MINIMUM SETUP TIME Data Inputs	t _{setup}	5	—	75	150	ns	
		10	—	40	80		
		15	—	30	60		
	Data Disable Inputs	t _{setup}	5	—	100	200	ns
			10	—	60	120	
			15	—	45	90	
MINIMUM HOLD TIME All Inputs	t _{hold}	5	—	75	150	ns	
		10	—	35	70		
		15	—	30	60		
RESET OPERATION							
PROPAGATION DELAY TIME	t _{PHL}	5	—	200	400	ns	
		10	—	100	200		
		15	—	75	150		
MINIMUM RESET PULSE WIDTH	PW _R	5	—	75	150	ns	
		10	—	40	80		
		15	—	30	60		
RESET REMOVAL TIME	t _{rem}	5	—	100	200	ns	
		10	—	60	120		
		15	—	45	90		

¹ When units are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the transition times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitive load.

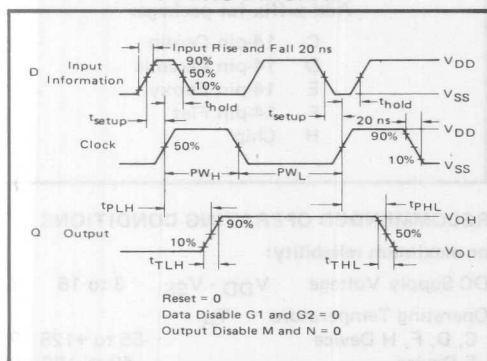


Typical P-Channel
Source Current Characteristics

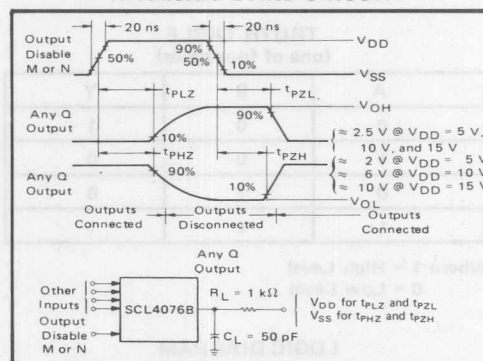


Typical N-Channel
Sink Current Characteristics

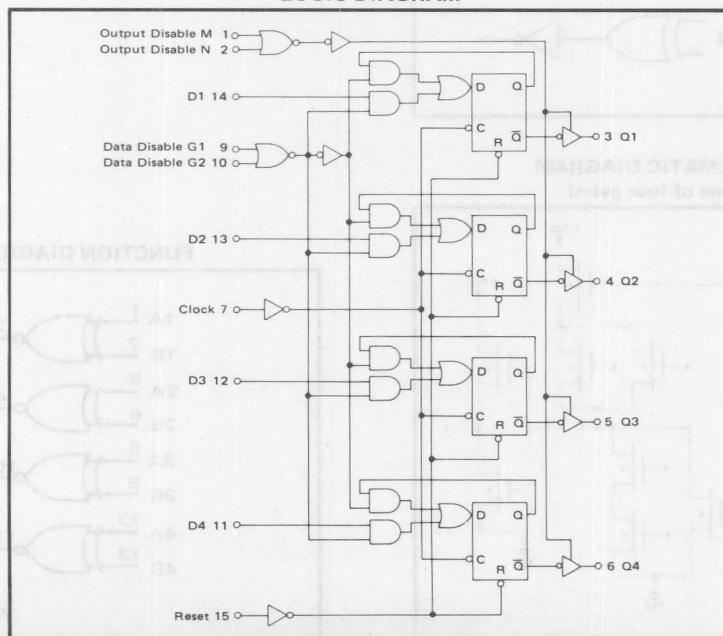
TIMING DIAGRAM



THREE-STATE PROPAGATION DELAY WAVESHAPE AND CIRCUIT



LOGIC DIAGRAM



SCL4077B



CMOS QUAD EXCLUSIVE-NOR GATE

FEATURES

- ◆ Buffered Outputs
- ◆ Diode Protection on all Inputs
- ◆ Fully "B"-Series Compatible
- ◆ Balanced Output Drive Current Specification

DESCRIPTION

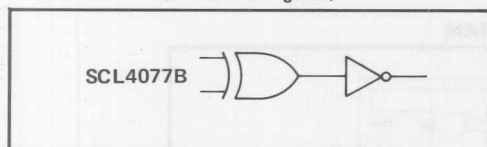
The SCL4077B contains four independent exclusive-NOR gates integrated on a single monolithic silicon chip. Each exclusive-NOR gate consists of five N-channel and five P-channel enhancement-mode transistors, plus output buffering devices.

TRUTH TABLE
(one of four gates)

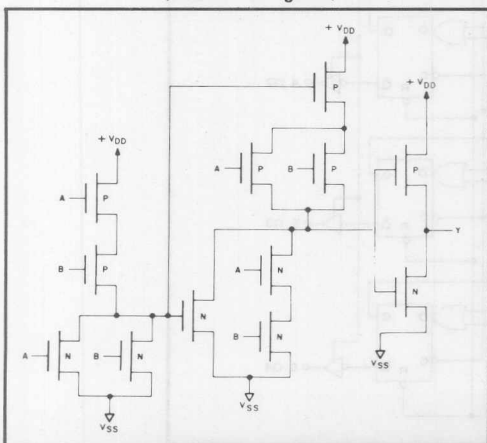
A	B	Y
0	0	1
1	0	0
0	1	0
1	1	1

Where 1 = High Level
0 = Low Level

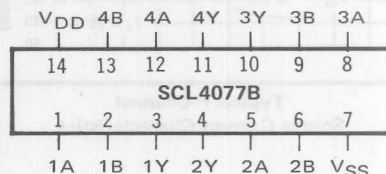
LOGIC DIAGRAM
(one of four gates)



SCHEMATIC DIAGRAM
(one of four gates)



CONNECTION DIAGRAM
(all packages)



Add suffix for package:

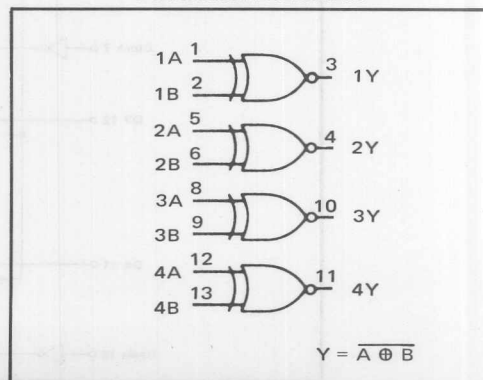
- C 14-pin Cerdip
- D 14-pin Ceramic
- E 14-pin Epoxy
- F 14-pin Flat
- H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A	-55 to +125	°C
C, D, F, H Device		-40 to +85	°C

FUNCTION DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS^{1, 3}

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	V _{IN} = V _{SS} or V _{DD} All valid input combinations	—	0.05	—	0.0005	0.05	—	1.5	μAdc
			—	0.10	—	0.001	0.10	—	3.0	
			—	0.20	—	0.002	0.20	—	6.0	
			—	—	—	—	—	—	—	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

² T_{LOW} = -55°C for C, D, F, H device.

= -40°C for E device.

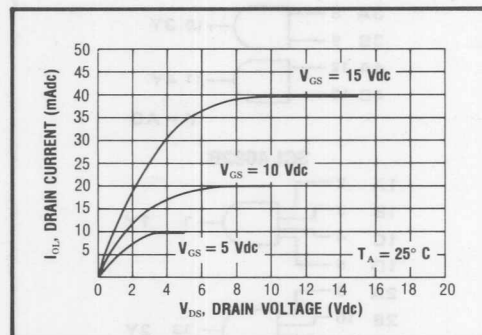
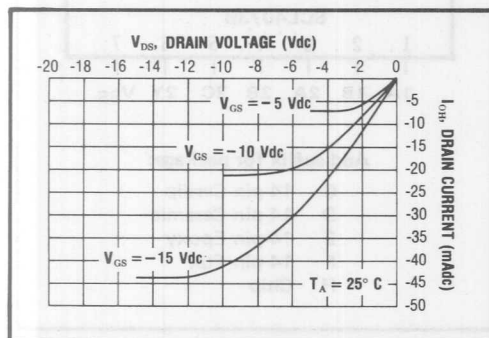
T_{HIGH} = +125°C for C, D, F, H device.

= + 85°C for E device.

³ This device has been designed for balanced output drive current specifications. Consult Family Specifications.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V _{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME	t _{PLH} , t _{PHL}	5	—	150	300	ns
		10	—	65	130	
		15	—	50	100	
		—	—	—	—	
OUTPUT TRANSITION TIME	t _{TLH} , t _{THL}	5	—	100	200	ns
		10	—	50	100	
		15	—	40	80	
		—	—	—	—	



SCL4081B, SCL4082B SCL4073B



CMOS AND GATES

SCL4081B - Quad 2-Input AND
SCL4082B - Dual 4-Input AND
SCL4073B - Triple 3-Input AND

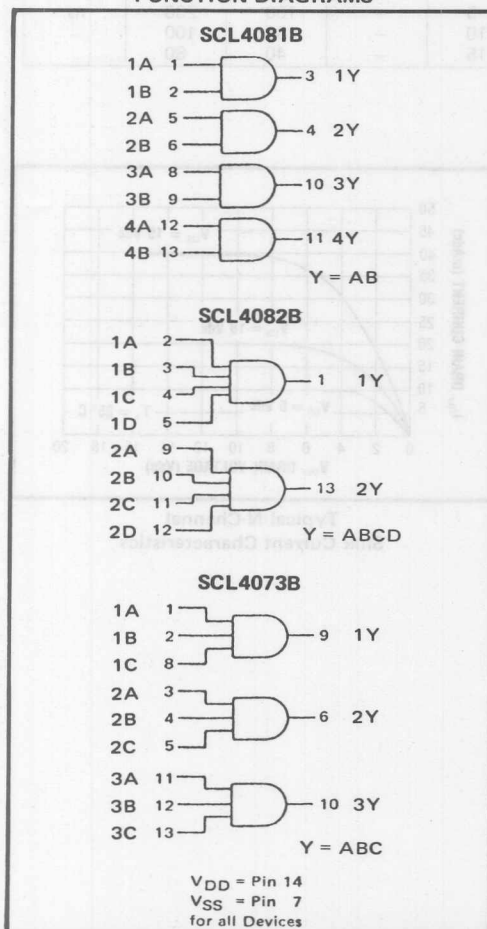
FEATURES

- ◆ Buffered Outputs
- ◆ Diode Protection on all Inputs
- ◆ Fully "B"-Series Compatible
- ◆ Balanced Output Drive Current Specifications

TRUTH TABLE

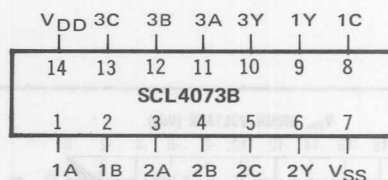
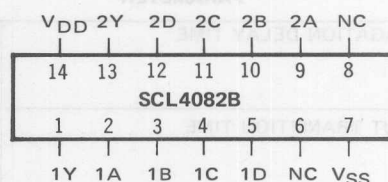
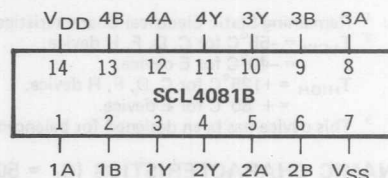
Inputs	Output
1 1 ... 1	1
All other combinations	0

FUNCTION DIAGRAMS



CONNECTION DIAGRAMS

(all packages)



Add suffix for package:

- C 14-pin Cerdip
- D 14-pin Ceramic
- E 14-pin Epoxy
- F 14-pin Flat
- H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	V_{dc}
Operating Temperature	T_A	-55 to +125	$^{\circ}C$
C, D, F, H Device		-40 to +85	$^{\circ}C$
E Device			

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS^{1, 3}

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	V _{IN} = V _{SS} or V _{DD} All valid input combinations	—	0.05	—	0.0005	0.05	—	1.5	μAdc
	5		—	0.10	—	0.001	0.10	—	3.0	
	10		—	0.20	—	0.002	0.20	—	6.0	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

² T_{LOW} = -55°C for C, D, F, H device.

= -40°C for E device.

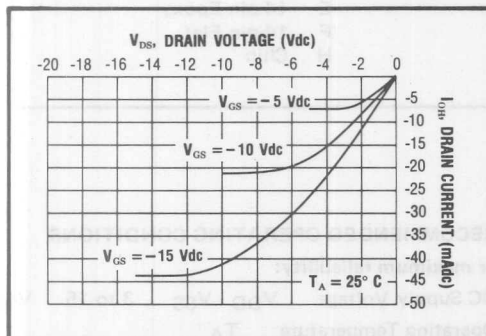
T_{HIGH} = +125°C for C, D, F, H device.

= + 85°C for E device.

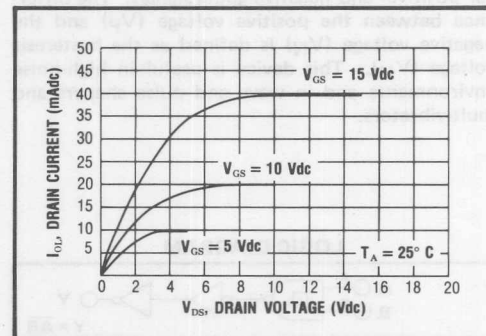
³ These devices have been designed for balanced output drive current specifications. Consult Family Specifications.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V _{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME	t _{PLH} , t _{PHL}	5	—	150	300	ns
		10	—	65	130	
		15	—	50	100	
OUTPUT TRANSITION TIME	t _{TLH} , t _{THL}	5	—	100	200	ns
		10	—	50	100	
		15	—	40	80	

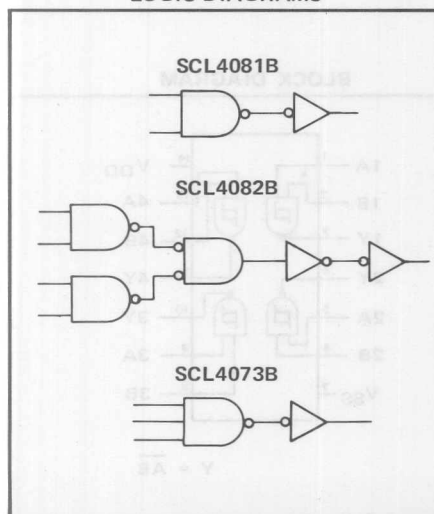


Typical P-Channel
Source Current Characteristics

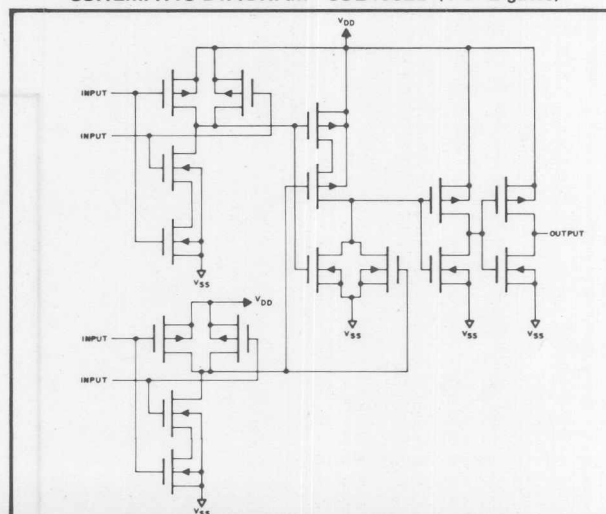


Typical N-Channel
Sink Current Characteristics

LOGIC DIAGRAMS



SCHEMATIC DIAGRAM - SCL4082B (1 of 2 gates)





FEATURES

- ◆ Schmitt Trigger Action on each Input with no External Components
- ◆ Quad 2-Input NAND Configuration
- ◆ Noise Immunity Greater than 50%
- ◆ No Limit on Input Rise and Fall Times
- ◆ Balanced Output Drive Current Specifications

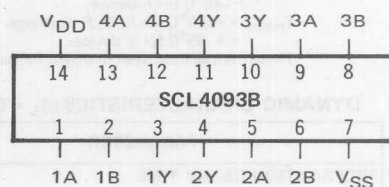
DESCRIPTION

The SCL4093B consists of four Schmitt trigger circuits. Each circuit functions as a 2-input NAND gate with Schmitt trigger action on both inputs. The gate switches at different points for positive- and negative-going signals. The difference between the positive voltage (V_P) and the negative voltage (V_N) is defined as the hysteresis voltage (V_H). This device is useful in high-noise environments and in wave and pulse shapers and multivibrators.

LOGIC DIAGRAM



* All inputs protected by Standard Protection Network

CONNECTION DIAGRAM
(all packages)

Add suffix for package:

- C 14-pin Cerdip
- D 14-pin Ceramic
- E 14-pin Epoxy
- F 14-pin Flat
- H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

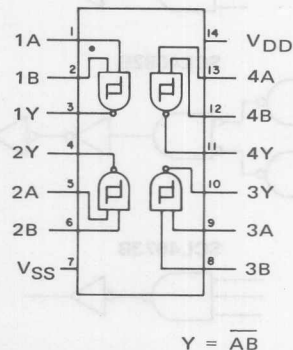
DC Supply Voltage $V_{DD} - V_{SS}$ 3 to 15 Vdc

Operating Temperature T_A

C, D, F, H Device -55 to +125 °C

E Device -40 to +85 °C

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS^{1,3}

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	5	—	0.05	—	0.0005	0.05	—	1.5	μA _{dc}
		10	—	0.10	—	0.001	0.10	—	3.0	
		15	—	0.20	—	0.002	0.20	—	6.0	
POSITIVE TRIGGER THRESHOLD VOLTAGE	V _P (V _{IL})	5	3 typ			2.9 typ		2.9 typ		Vdc
		10	5.9 typ			5.9 typ		5.9 typ		
		15	8.9 typ			8.9 typ		8.9 typ		
NEGATIVE TRIGGER THRESHOLD VOLTAGE	V _N (V _{IH})	5	2.6 typ			2.3 typ		2.1 typ		Vdc
		10	4 typ			3.9 typ		3.8 typ		
		15	5.5 typ			5.4 typ		5.3 typ		

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

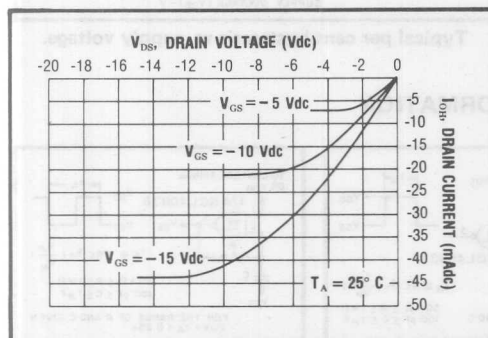
² T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.

T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

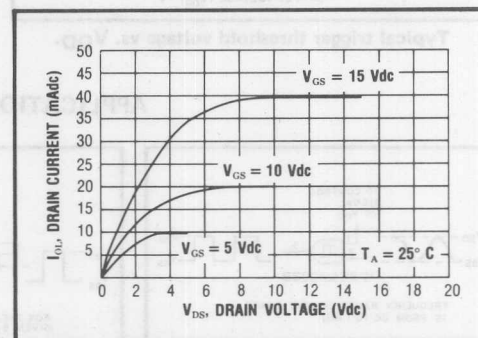
³ This device has been designed for balanced output drive current specifications. Consult Family Specifications.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

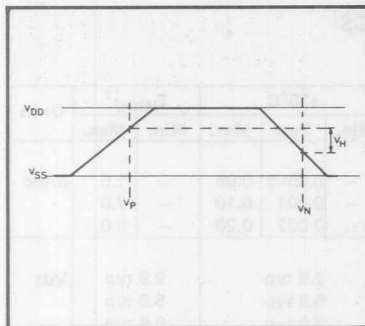
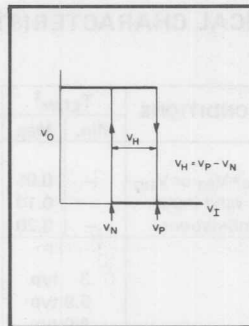
PARAMETER		V _{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME	t _{PLH} , t _{PHL}	5	—	300	600	ns
		10	—	150	300	
		15	—	120	240	
OUTPUT TRANSITION TIME	t _{TLH} , t _{THL}	5	—	100	200	ns
		10	—	50	100	
		15	—	40	80	



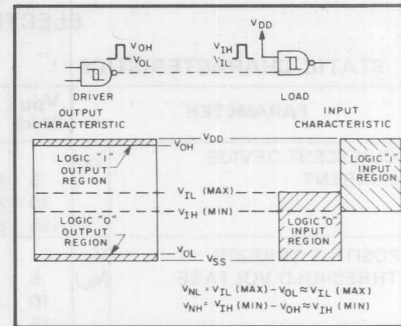
Typical P-Channel
Source Current Characteristics



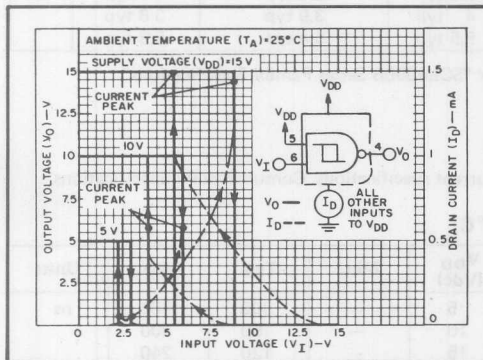
Typical N-Channel
Sink Current Characteristics


Definition of V_P , V_N and V_H .


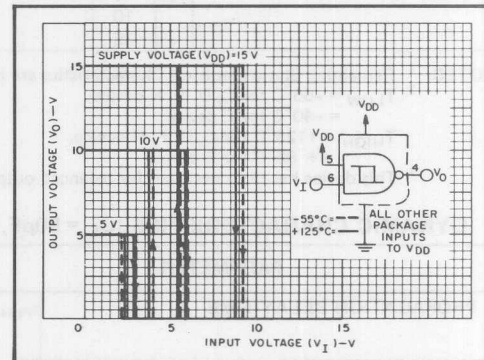
Transfer characteristic of 1 of 4 gates.



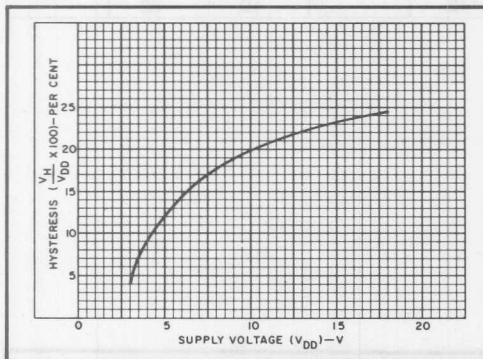
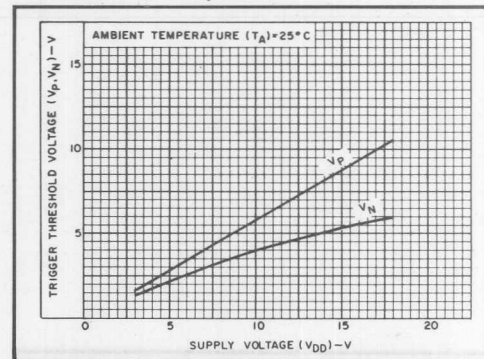
Input and output characteristics.



Typical current and voltage transfer characteristics.

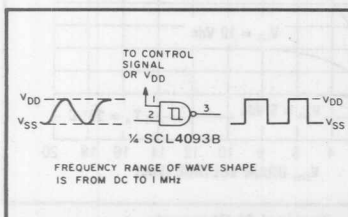


Typical voltage transfer characteristics as a function of temperature.

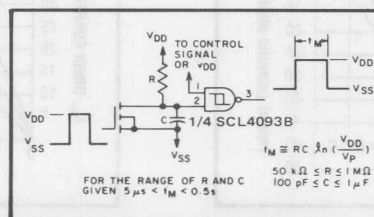

Typical trigger threshold voltage vs. V_{DD} .


Typical per cent hysteresis vs. supply voltage.

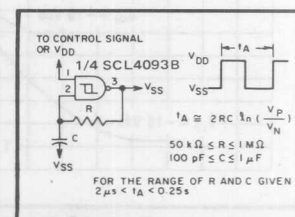
APPLICATIONS INFORMATION



Wave shaper.



Monostable multivibrator.



Astable multivibrator.

**SCL4160B, SCL4161B
SCL4162B, SCL4163B
Preliminary**



CMOS SYNCHRONOUS 4-BIT COUNTERS

FEATURES

- ◆ BCD Decade (SCL4160B, SCL4162B) or 4-Bit Binary (SCL4161B, SCL4163B) Counting
- ◆ Internal Look-Ahead for Fast Counting
- ◆ Carry Output for Cascading
- ◆ Synchronously Programmable
- ◆ Synchronous Counting
- ◆ Load Control Input
- ◆ Clear Input - Asynchronous (SCL4160B, SCL4161B) or Synchronous (SCL4162B, SCL4163B)
- ◆ Static Operation - DC to 5MHz @ 10Vdc
- ◆ Balanced Output Drive Current Specifications

DESCRIPTION

The SCL4160B - SCL4163B are Synchronous Programmable Counters constructed with complementary MOS P-Channel and N-Channel enhancement-mode devices in a single monolithic structure. These counters are functionally equivalent to the 74160 - 74163 TTL counters.

Two are synchronous programmable decade counters with asynchronous and synchronous Clear inputs respectively (SCL4160, SCL4162). The other two are 4-bit binary counters with asynchronous and synchronous Clear respectively (SCL4161, SCL4163).

SYNCHRONOUS MODE SELECTION SCL4160B/SCL4161B

L	PE	TE	Mode
L	X	X	Preset
H	L	X	No Change
H	X	L	No Change
H	H	H	Count

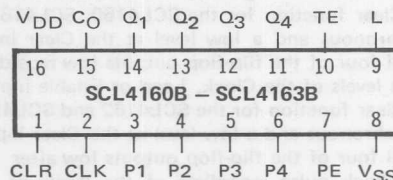
H = High level L = Low level X = Don't care

SYNCHRONOUS MODE SELECTION SCL4162B/SCL4163B

CLR	L	PE	TE	Mode
H	L	X	X	Preset
H	H	L	X	No Change
H	H	X	L	No Change
H	H	H	H	Count
L	X	X	X	Reset

H = High level L = Low level X = Don't care

CONNECTION DIAGRAM (all packages)



Add suffix for package:

- C 16-pin Cerdip
- D 16-pin Ceramic
- E 16-pin Epoxy
- F 16-pin Flat
- H Chip

RECOMMENDED OPERATING CONDITIONS

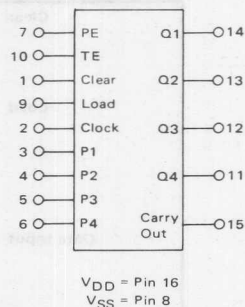
For maximum reliability:

DC Supply Voltage $V_{DD} - V_{SS}$ 3 to 15 Vdc

Operating Temperature T_A

C, D, F, H Device -55 to +125 °C
E Device -40 to +85 °C

BLOCK DIAGRAM



SELECTOR GUIDE

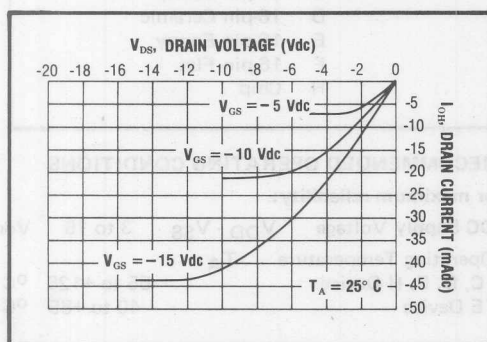
CLEAR	MODULUS	
	DECADE	BINARY
Asynchronous	SCL4160B	SCL4161B
Synchronous	SCL4162B	SCL4163B

FUNCTIONAL DESCRIPTION

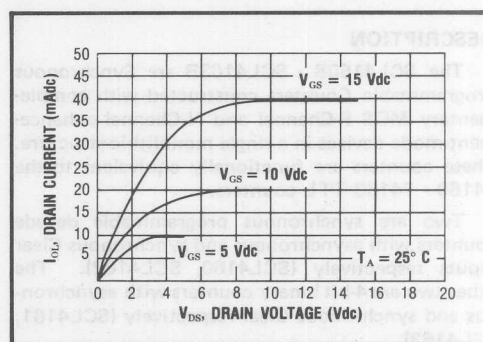
These counters are fully programmable; that is, the outputs may be preset to either level. As pre-setting is synchronous, setting up a low level at the Load input disables the counter and causes the outputs to agree with the setup data after the next Clock pulse regardless of the levels of the Enable inputs. Low-to-high transitions at the Load input should be avoided when the Clock is low if the Enable inputs are high at or before the transition. The Clear function for the SCL4160, SCL4161 is asynchronous and a low level at the Clear input sets all four of the flip-flop outputs low regardless of the levels of the Clock, Load or Enable inputs. The Clear function for the SCL4162 and SCL4163 is synchronous and a low level at the Clear inputs sets all four of the flip-flop outputs low after the next Clock pulse regardless of the levels of the Enable inputs. This synchronous Clear allows the count length to be modified easily; decoding the

maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the Clear input to synchronously clear the counter to 0000 (LLLL).

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two Count Enable inputs and a Carry output. Both Count Enable inputs (PE, TE) must be high to count, and Enable input TE is fed forward to enable the carry output. The Carry output thus enabled will produce a positive output pulse with a duration approximately equal to the positive portion of the Q1 output. This positive overflow Carry pulse can be used to enable successive cascaded stages. High-to-low-level transitions at the Enable PE or TE inputs should occur only when the Clock input is high.

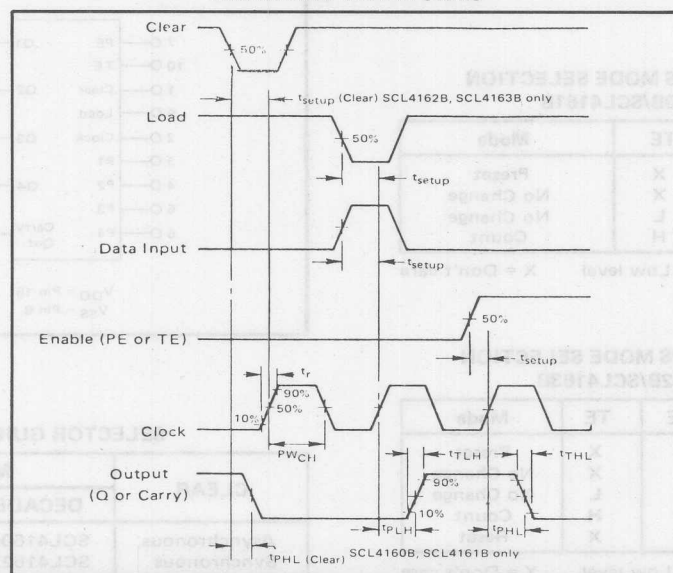


Typical P-Channel
Source Current Characteristics



Typical N-Channel
Sink Current Characteristics

SWITCHING WAVEFORMS



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS^{1, 3}

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	V _{IN} = V _{SS} or V _{DD} All valid input combinations	—	5	—	0.05	5	—	150	μAdc
			—	10	—	0.1	10	—	300	
			—	20	—	0.2	20	—	600	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

² T_{LOW} = -55°C for C, D, F, H device.

= -40°C for E device.

T_{HIGH} = +125°C for C, D, F, H device.

= + 85°C for E device.

³ These devices have been designed for balanced output drive current specifications. Consult Family Specifications.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V _{DD} (Vdc)	Min.	Typ.	Max.	Units	
CLOCKED OPERATION							
PROPAGATION DELAY TIME Clock to Q	t _{PLH} , t _{PHL}	5	—	200	400	ns	
		10	—	80	160		
		15	—	60	120		
		Clock to Carry Out	5	—	240	480	ns
			10	—	95	190	
			15	—	75	150	
		TE to Carry Out	5	—	180	360	ns
			10	—	70	140	
			15	—	50	100	
OUTPUT TRANSITION TIME	t _{TLH} , t _{THL}	5	—	100	200	ns	
10	—	50	100				
15	—	40	80				
MINIMUM CLOCK PULSE WIDTH	PW _{CL}	5	—	85	170	ns	
10	—	35	70				
15	—	25	50				
MAXIMUM CLOCK FREQUENCY	f _{CL}	5	2.0	3.0	—	MHz	
		10	5.5	8.5	—		
		15	8.0	12.0	—		
MAXIMUM CLOCK RISE AND FALL TIME ¹	t _{rCL} , t _{fCL}	5	50	∞	—	ms	
10	50	∞	—				
15	50	∞	—				
MINIMUM SETUP TIME Data to Clock	t _{setup}	5	—	120	240	ns	
		10	—	45	90		
		15	—	30	65		
		Load to Clock	5	—	120	240	ns
			10	—	45	90	
			15	—	30	65	
		PE or TE to Clock	5	—	170	340	ns
			10	—	70	140	
			15	—	50	100	
CLEAR OPERATION							
PROPAGATION DELAY TIME Clear to Q (SCL 4160, SCL 4161 only)	t _{PLH} , t _{PHL}	5	—	150	300	ns	
		10	—	50	100		
		15	—	30	60		
MINIMUM SETUP TIME Clear to Clock (SCL 4162, SCL 4163 only)	t _{setup}	5	—	120	240	ns	
		10	—	50	100		
		15	—	30	60		

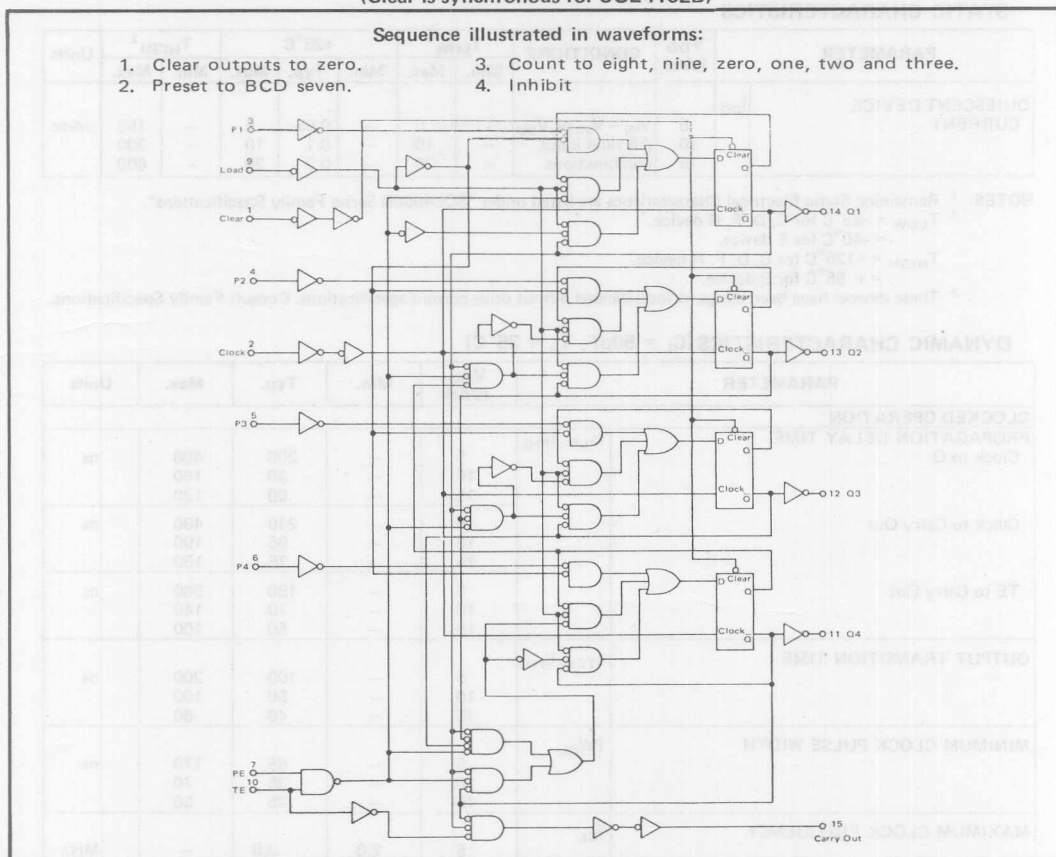
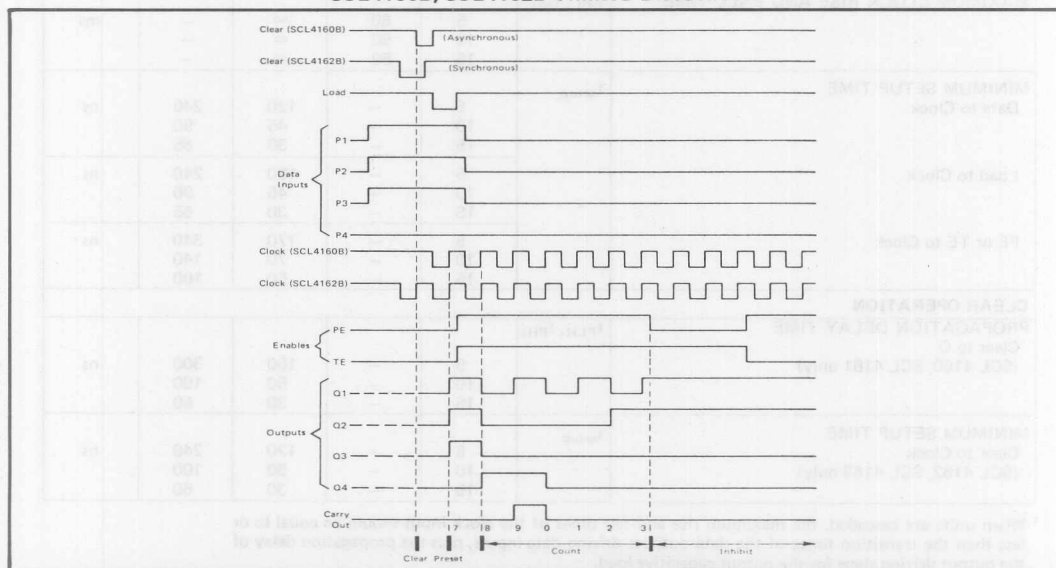
¹ When units are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the transition times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitive load.

SCL4160B, SCL4162B LOGIC DIAGRAM

(Clear is synchronous for SCL4162B)

Sequence illustrated in waveforms:

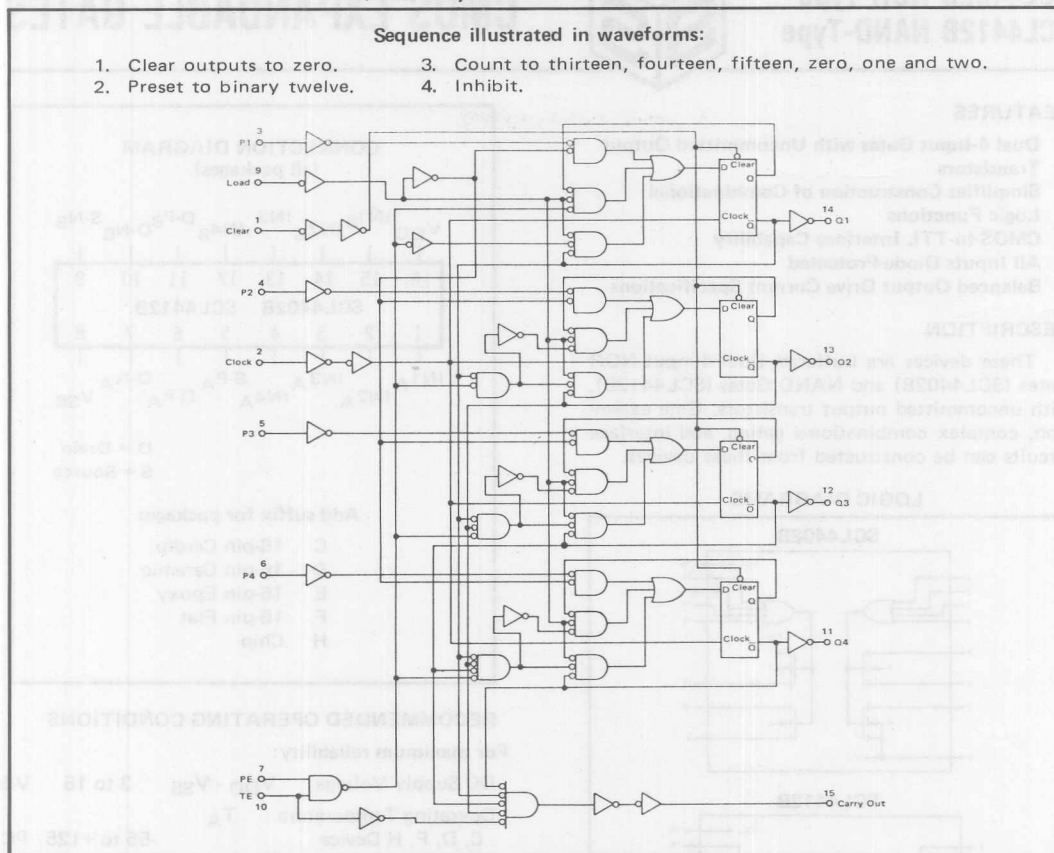
1. Clear outputs to zero.
2. Preset to BCD seven.
3. Count to eight, nine, zero, one, two and three.
4. Inhibit

**SCL4160B, SCL4162B TIMING DIAGRAM**

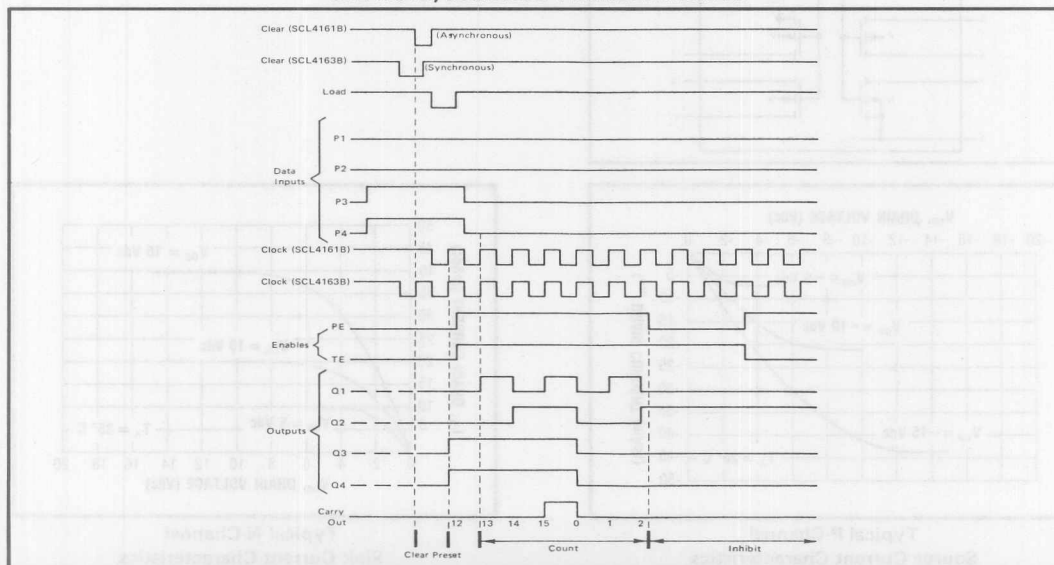
SCL4161B, SCL4163B LOGIC DIAGRAM (Clear is Synchronous for SCL4163B)

Sequence illustrated in waveforms:

1. Clear outputs to zero.
2. Preset to binary twelve.
3. Count to thirteen, fourteen, fifteen, zero, one and two.
4. Inhibit.



SCL4161B, SCL4163B TIMING DIAGRAM



SCL4402B NOR-Type SCL4412B NAND-Type



CMOS EXPANDABLE GATES

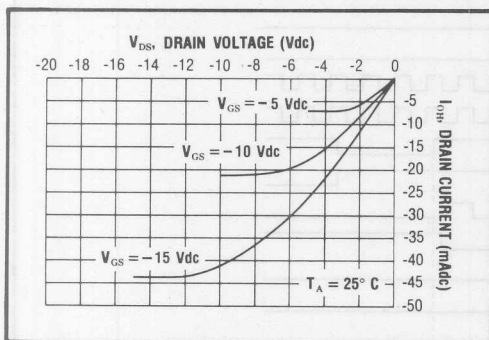
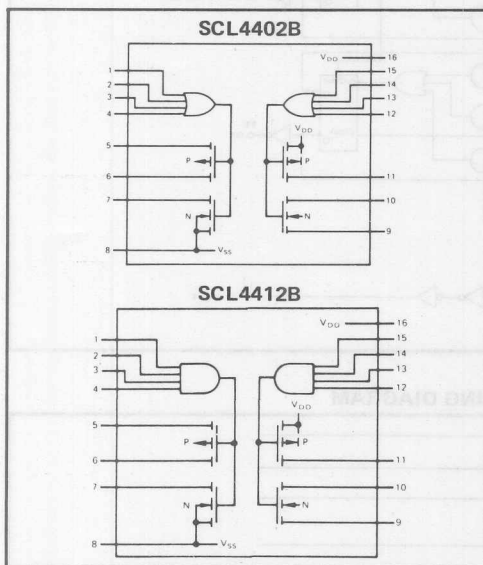
FEATURES

- ◆ Dual 4-Input Gates with Uncommitted Output Transistors
- ◆ Simplifies Construction of Combinational Logic Functions
- ◆ CMOS-to-TTL Interface Capability
- ◆ All Inputs Diode-Protected
- ◆ Balanced Output Drive Current Specifications

DESCRIPTION

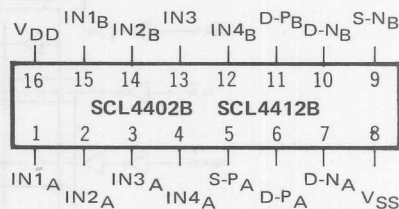
These devices are buffered Dual 4-input NOR Gates (SCL4402B) and NAND Gates (SCL4412B), with uncommitted output transistors. Gate expansion, complex combinational gating, and interface circuits can be constructed from these devices.

LOGIC DIAGRAMS



Typical P-Channel
Source Current Characteristics

CONNECTION DIAGRAM (all packages)



D = Drain
S = Source

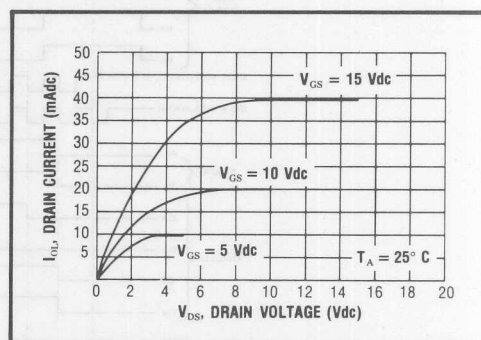
Add suffix for package:

- C 16-pin Cerdip
- D 16-pin Ceramic
- E 16-pin Epoxy
- F 16-pin Flat
- H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A	-55 to +125	°C
C, D, F, H Device		-40 to +85	°C
E Device			



Typical N-Channel
Sink Current Characteristics

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS^{1,3}

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	V _{IN} = V _{SS} or V _{DD} All valid input combinations	—	0.05	—	0.0005	0.05	—	1.5	μA _{dc}
			—	0.10	—	0.001	0.10	—	3.0	
			—	0.20	—	0.002	0.20	—	6.0	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

² T_{LOW} = -55°C for C, D, F, H device.

= -40°C for E device.

T_{HIGH} = +125°C for C, D, F, H device.

= + 85°C for E device.

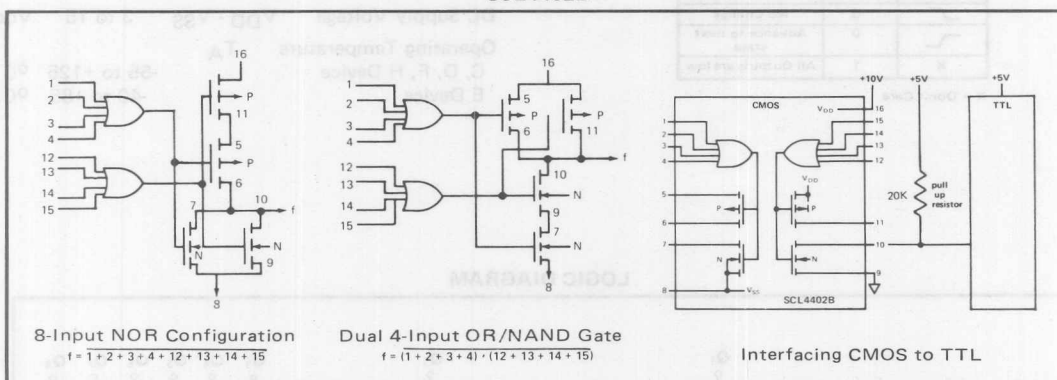
³ These devices have been designed for balanced output drive current specifications. Consult Family Specifications.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

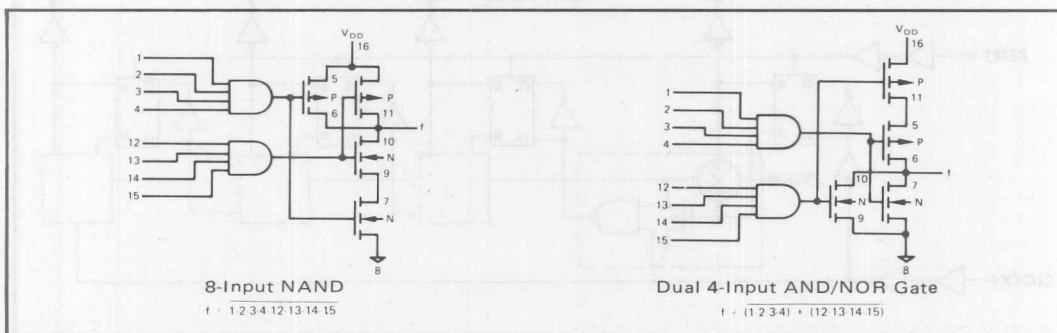
PARAMETER		V _{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME Connected as Dual 4-Input Gates	t _{PLH} , t _{PHL}	5	—	125	250	ns
		10	—	60	120	
		15	—	45	90	
OUTPUT TRANSITION TIME	t _{TLH} , t _{THL}	5	—	100	200	ns
		10	—	50	100	
		15	—	40	80	

APPLICATIONS INFORMATION

SCL4402B



SCL4412B



For additional information, see Application Note AN-102.

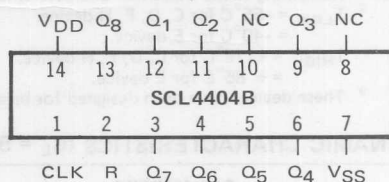


FEATURES

- ◆ 8-Stage Synchronous Counter
- ◆ Buffered Outputs from all 8 Stages
- ◆ Direct Reset
- ◆ Fully Static Operation — DC to 8MHz @ 10Vdc
- ◆ Balanced Output Drive Current Specifications

DESCRIPTION

The SCL4404B consists of eight synchronous, single-phase clocked counting stages, with the Q output of each stage accessible. The counter is reset to all "zeroes" by a high level on the Reset line. Each stage of the counter utilizes a master-slave flip-flop configuration. The state of the counter is advanced one step in binary order on the negative-going transition of the input clock pulse.

CONNECTION DIAGRAM
(all packages)

Add suffix for package:

- C 14-pin Cerdip
- D 14-pin Ceramic
- E 14-pin Epoxy
- F 14-pin Flat
- H Chip

TRUTH TABLE

CLOCK	RESET	OUTPUT STATE
	0	No Change
	0	Advance to next state
X	1	All Outputs are low

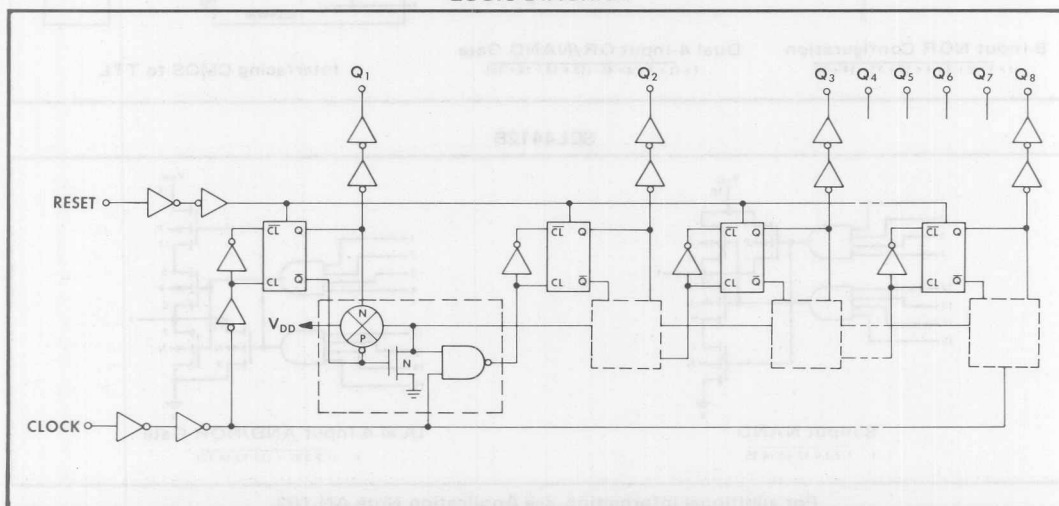
X = Don't Care

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS^{1,3}

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	V _{IN} = V _{SS} or V _{DD} All valid input combinations	—	5	—	0.05	5	—	150	μAdc
			—	10	—	0.1	10	—	300	
			—	20	—	0.2	20	—	600	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

² T_{LOW} = -55°C for C, D, F, H device.

= -40°C for E device.

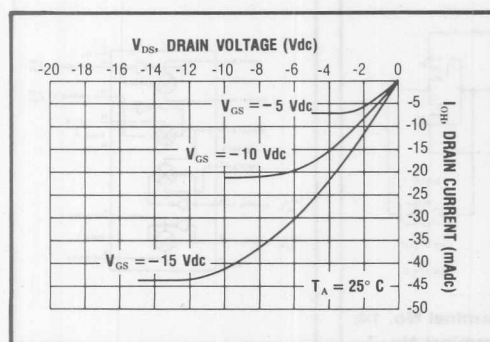
T_{HIGH} = +125°C for C, D, F, H device.

= + 85°C for E device.

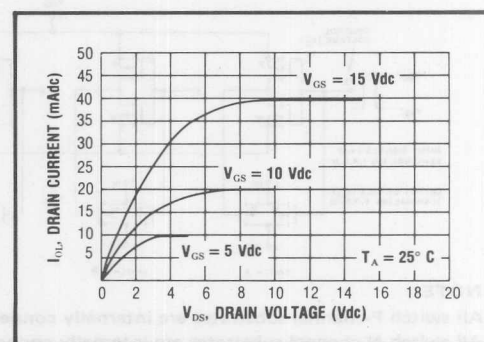
³ This device has been designed for balanced output drive current specifications. Consult Family Specifications.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V _{DD} (Vdc)	Min.	Typ.	Max.	Units
CLOCKED OPERATION						
PROPAGATION DELAY TIME	t _{PLH} , t _{PHL}	5 10 15	— — —	250 125 100	500 250 200	ns
OUTPUT TRANSITION TIME	t _{TLH} , t _{THL}	5 10 15	— — —	100 50 40	200 100 80	ns
MINIMUM CLOCK PULSE WIDTH	PW _{CL}	5 10 15	— — —	125 65 50	250 130 100	ns
MAXIMUM CLOCK FREQUENCY	f _{CL}	5 10 15	2.0 4.0 5	4.0 8.0 10	— — —	MHz
MAXIMUM CLOCK RISE AND FALL TIME	t _{rCL} , t _{fCL}	5 10 15	15 5 3	— — —	— — —	μs
RESET OPERATION						
PROPAGATION DELAY TIME	t _{PHL}	5 10 15	— — —	175 75 60	350 150 120	ns
MINIMUM RESET PULSE WIDTH	PW _R	5 10 15	— — —	100 50 40	200 100 80	ns
RESET REMOVAL TIME	t _{rem}	5 10 15	— — —	200 90 65	400 180 130	ns



Typical P-Channel
Source Current Characteristics



Typical N-Channel
Sink Current Characteristics

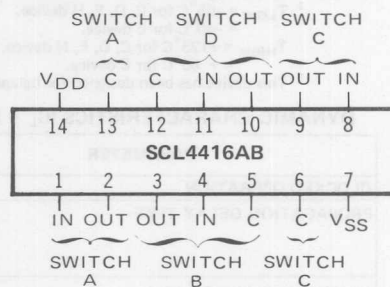


FEATURES

- ◆ DPDT Switch Operation Without External Logic
- ◆ Wide Range of Digital and Analog Signal Levels — Digital or Analog Signal to 18 Volts peak
- ◆ Low ON Resistance — $200\ \Omega$ typ. over $15V_{p-p}$ Signal Input Range, $V_{DD} - V_{SS} = 15V$
- ◆ Matched Switch Characteristics - $10\ \Omega$ typ. Difference Between R_{ON} Values at a Fixed Bias Point over $15V_{p-p}$ Signal Input Range, $V_{DD} - V_{SS} = 15V$
- ◆ High "ON/OFF" Output Voltage Ratio — $65\ dB$ typ. @ $f_{is} = 10\ kHz$, $R_L = 10\ k\Omega$
- ◆ High Degree of Linearity — 0.4% Distortion typ. @ $f_{is} = 1\ kHz$, $V_{is} = 5\ V_{p-p}$, $V_{DD} - V_{SS} = 10V$, $R_L = 10\ k\Omega$
- ◆ Extremely low OFF Switch Leakage Resulting in Very Low Offset Current and High Effective OFF Switch Resistance — $10\ pA$ typ. @ $V_{DD} - V_{SS} = 10V$, $T_A = 25^\circ C$
- ◆ Extremely High Control Input Impedance (Control Circuit Isolated from Signal Circuit) — $10^{12}\ \Omega$ typ.
- ◆ Low Crosstalk Between Switches — $-50\ dB$ typ. @ $f_{is} = 0.9\ MHz$, $R_L = 1\ k\Omega$
- ◆ Matched Control-Input to Signal-Output Capacitances - Reduces Output Signal Transients
- ◆ Transmits Frequencies up to $40\ MHz$

DESCRIPTION

The SCL4416AB is a single-chip monolithic silicon integrated circuit containing eight N-channel and eight P-channel enhancement-mode MOS transistors connected to form four independent bilateral signal switches. Each switch consists of both P- and N-channel devices with common source and drain connections. A single control signal is required per switch. Both P and N devices in a

CONNECTION DIAGRAM
(all packages)

Add suffix for package:

C	14-pin Cerdip	F	14-pin Flat
D	14-pin Ceramic	H	Chip
E	14-pin Epoxy		

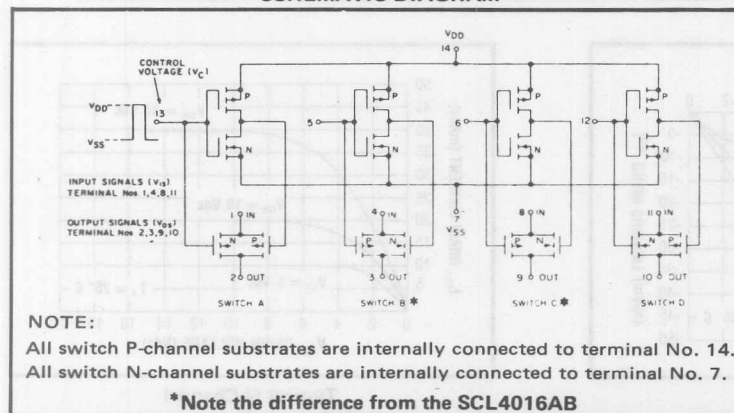
RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

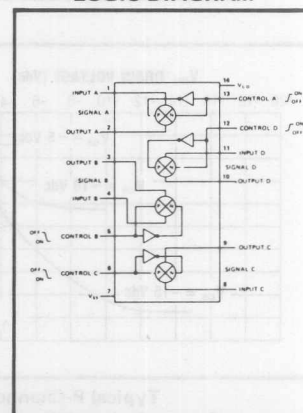
DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	$^\circ C$
E Device		-40 to +85	$^\circ C$

given switch are biased ON or OFF by the control signal. The CMOS switch permits peak input-signal voltage swings equal to the full supply voltage, a considerable advantage over single-channel types.

SCHEMATIC DIAGRAM



LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS^{1,3}

PARAMETER	CONDITIONS	V _{SS} (Vdc)	V _{DD} (Vdc)	T _{LOW} ²		25°C			T _{HIGH} ²		Units
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD} V _{IN} = V _{SS} or V _{DD} All valid input combinations	0	5	—	0.05	—	0.0005	0.05	—	1.5	μAdc
		0	10	—	0.1	—	0.001	0.1	—	3.0	
		0	15	—	0.2	—	0.002	0.2	—	6.0	
MINIMUM INPUT HIGH VOLTAGE (Control Input)	V _{IH} V _{IS} = V _{SS} V _{OS} = V _{DD} I _{OS} = 10μA	0	5	—	2.9	—	1.5	2.9	—	2.4	Vdc
		0	10	—	2.9	—	1.5	2.7	—	2.4	
		0	15	—	2.9	—	1.5	2.7	—	2.4	
MAXIMUM INPUT LOW VOLTAGE (Control Input)	V _{IL} V _{IS} = V _{SS} V _{OS} = V _{DD} I _{OS} = 10μA	0	5	0.9	—	0.7	1.5	—	0.4	—	Vdc
		0	10	0.9	—	0.7	1.5	—	0.4	—	
		0	15	0.9	—	0.7	1.5	—	0.4	—	
SWITCH INPUT/OUTPUT LEAKAGE (Switch off)	I _{OFF} V _C = V _{SS} ⁴ V _{IS}	±7.5	—	—	—	—	—	—	—	—	nAdc
		±5	—	—	—	—	—	—	—	—	
ON-RESISTANCE C, D, F, H device	R _{ON} V _C = V _{DD} ⁴ R _L = 10kΩ	V _{IS} (Vdc)		—	—	—	—	—	—	—	Ω
		+7.5		—	360	—	200	400	—	600	
		-7.5		—	360	—	200	400	—	600	
		±0.25		—	775	—	280	850	—	1230	
		+5		—	600	—	250	660	—	960	
		-5		—	600	—	250	660	—	960	
		±0.25		—	1870	—	580	2000	—	2600	
		+15		—	360	—	200	400	—	600	
		+0.25		—	360	—	200	400	—	600	
		+9.3		—	775	—	300	850	—	1230	
		+10		—	600	—	250	660	—	960	
		+0.25		—	600	—	250	660	—	960	
		+5.6		—	1870	—	560	2000	—	2600	
E device	R _{ON} V _C = V _{DD} ⁴ R _L = 10kΩ	V _{IS} (Vdc)		—	—	—	—	—	—	—	Ω
		+7.5		—	370	—	200	400	—	520	
		-7.5		—	370	—	200	400	—	520	
		±0.25		—	790	—	280	850	—	1080	
		+5		—	610	—	250	660	—	840	
		-5		—	610	—	250	660	—	840	
		±0.25		—	1900	—	580	2000	—	2380	
		+15		—	370	—	200	400	—	520	
		+0.25		—	370	—	200	400	—	520	
		+9.3		—	790	—	300	850	—	1080	
		+10		—	610	—	250	660	—	840	
		+0.25		—	610	—	250	660	—	840	
		+5.6		—	1900	—	560	2000	—	2380	
ON-RESISTANCE MATCH (Same package)	ΔR _{ON} V _C = V _{DD} ⁴ R _L = 10kΩ	V _{IS} (Vdc)		—	—	—	—	—	—	—	Ω
		±7.5		—	—	—	10	—	—	—	
		±5		—	—	—	15	—	—	—	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".² T_{LOW} = -55°C for C, D, F, H device.

= -40°C for E device.

T_{HIGH} = +125°C for C, D, F, H device.

= + 85°C for E device.

³ This device has been designed for balanced output drive current specifications. Consult Family Specifications.⁴ Reverse polarity of V_C (control input) for switches B and C.DYNAMIC CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

PARAMETER	CONDITIONS	V _{SS} (Vdc)	V _{DD} (Vdc)	Min.	Typ.	Max.	Units
SIGNAL INPUTS (V _{IS}) AND OUTPUTS (V _{OS})							
PROPAGATION DELAY TIME Signal input to signal output	t _{PLH} , t _{PHL} V _C = V _{DD} ¹ V _{IS} = square wave R _L = 10kΩ	0	5	—	20	40	ns
		0	10	—	10	20	
		0	15	—	7.5	15	
BANDWIDTH (-3dB) (Sine Wave)	BW V _C = V _{DD} ¹ V _{IS} = 5V _{p-p} centered @0.0Vdc	R _L		—	—	—	MHz
		1kΩ		-5	+5	54	
		10kΩ		—	—	40	
		100kΩ		—	—	38	
		1MΩ		—	—	37	

ELECTRICAL CHARACTERISTICS (Continued)

DYNAMIC CHARACTERISTICS ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$) (Continued)

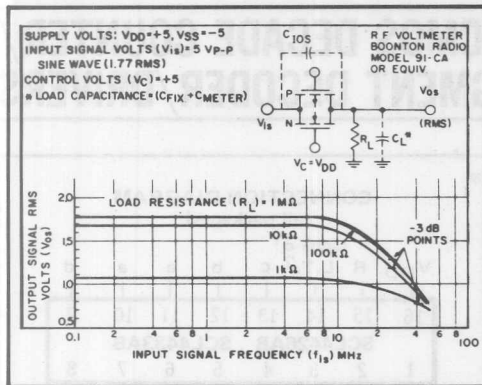
PARAMETER	CONDITIONS	V_{SS} (Vdc)	V_{DD} (Vdc)	Min.	Typ.	Max.	Units
SIGNAL INPUTS (V_{IS}) AND OUTPUTS (V_{OS}) (Continued)							
INSERTION LOSS ($= 20 \log_{10} \frac{V_{OS}}{V_{IS}}$)	$V_C = V_{DD}^1$ $V_{IS} = 5V_{pp}$ centered @0.0Vdc	R_L 1k Ω 10k Ω 100k Ω 1M Ω	-5 +5	- -	2.3 0.2 0.1 0.05	- -	dB
SIGNAL DISTORTION (Sine Wave)	$V_C = V_{DD}^1$ $V_{IS} = 5V_{pp}$ centered @0.0Vdc $f_{IS} = 1.0\text{kHz}$ $R_L = 10k\Omega$	-5	+5	-	0.4	-	%
FEEDTHROUGH (-50dB)	$V_C = V_{SS}^1$ $V_{IS} = 5V_{pp}$ centered @0.0Vdc	R_L 1k Ω 10k Ω 100k Ω 1M Ω	-5 +5	- -	1250 140 18 2	- -	kHz
CROSSTALK (-50dB) (Between two switches)	$V_C(A) = V_{DD}^1$ $V_C(B) = V_{SS}^1$ $V_{IS}(A) = 5V_{pp}$ centered @0.0Vdc $R_L = 1.0k$	-5	+5	-	0.9	-	MHz
CAPACITANCE Input Output Feedthrough	C_{IS} C_{OS} C_{IOS} $V_C = V_{SS}^1$	-5	+5	- - -	4 4 0.2	- - -	pF pF pF
CONTROL INPUT (V_C)							
PROPAGATION DELAY TIME Turn on	t_{PLH} , t_{PHL} $V_{SS} \leq V_{IS} \leq V_{DD}$ $R_L = 10k\Omega$	0 0 0	5 10 15	- - -	40 20 15	80 40 30	ns
MAXIMUM INPUT FREQUENCY	f_C $V_{SS} \leq V_{IS} \leq V_{DD}$ $R_L = 1.0k\Omega$	0 0 0	5 10 15	- - -	5 10 12	- -	MHz
CROSSTALK (To signal port)	$V_C = \text{Square wave}$ $R_L = 10k\Omega$ $R_{IN} = 1.0k\Omega$	0 0 0	5 10 15	- - -	30 50 100	- -	mV

NOTE: ¹ Reverse polarity of V_C (control input) for switches B and C.

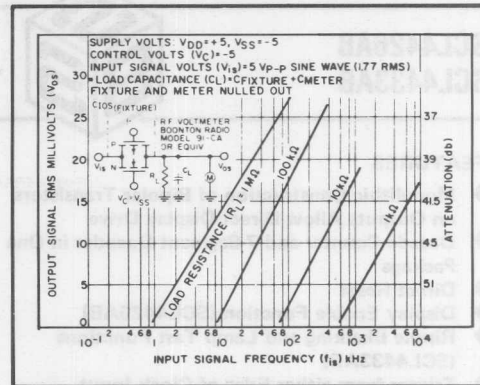
TYPICAL ON-RESISTANCE CHARACTERISTICS

CHARACTERISTIC*	SUPPLY CONDITIONS		LOAD CONDITIONS					
	V_{DD} (V)	V_{SS} (V)	$R_L = 1k\Omega$		$R_L = 10k\Omega$		$R_L = 100k\Omega$	
			VALUE (Ω)	V_{IS} (V)	VALUE (Ω)	V_{IS} (V)	VALUE (Ω)	V_{IS} (V)
R_{ON}	+15	0	200	+15	200	+15	180	+15
$R_{ON(max.)}$	+15	0	300	+11	300	+9.3	320	+9.2
R_{ON}	+10	0	290	+10	250	+10	240	+10
$R_{ON(max.)}$	+10	0	500	+7.4	560	+5.6	610	+5.5
R_{ON}	+5	0	880	+5	470	+5	450	+5
$R_{ON(max.)}$	+5	0	600	0	580	0	800	0
R_{ON}	+7.5	-7.5	200	+7.5	200	+7.5	180	+7.5
$R_{ON(max.)}$	+7.5	-7.5	290	± 0.25	280	± 0.25	400	± 0.25
R_{ON}	+5	-5	260	+5	250	+5	240	+5
$R_{ON(max.)}$	+5	-5	310	-5	250	-5	240	-5
R_{ON}	+2.5	-2.5	590	+2.5	450	+2.5	490	+2.5
$R_{ON(max.)}$	+2.5	-2.5	720	-2.5	520	-2.5	520	-2.5
R_{ON}	+2.5	-2.5	232k	± 0.25	300k	± 0.25	870k	± 0.25

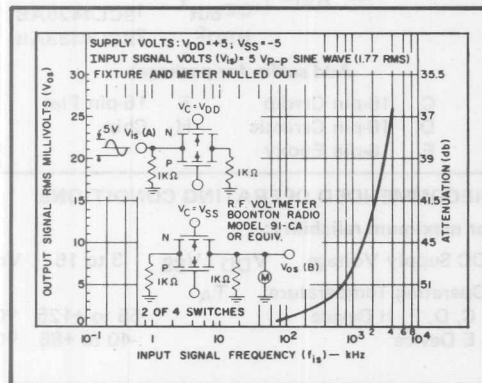
* Variation from a perfect switch; $R_{ON} = 0\Omega$.



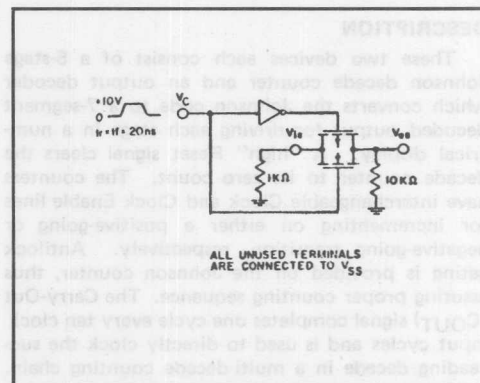
Typ. switch frequency response - switch "ON"



Typ. feedthru vs. freq. — switch "OFF"



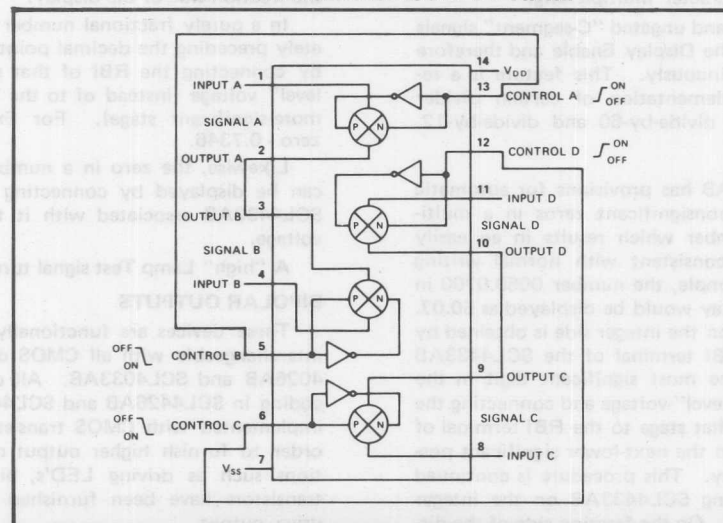
Typ. crosstalk between switch circuits in the same package



Test circuit, Crosstalk-control input to signal output.

APPLICATIONS INFORMATION

SCL4416AB connected as a DPDT Switch



SCL4426AB SCL4433AB



CMOS DECADE COUNTER/ 7-SEGMENT DECODER/DRIVERS

FEATURES

- ◆ Monolithic Construction of Bipolar Transistors on Outputs Allow Direct Display Drive
- ◆ Decade Counter and 7-Segment Decoder in One Package
- ◆ Direct Reset
- ◆ Display Enable Function (SCL4426AB)
- ◆ Ripple Blanking and Lamp Test Functions (SCL4433AB)
- ◆ Trigger from either Edge of Clock Input
- ◆ Carry Output for Cascading Stages
- ◆ Fully Static Operation - DC to 5MHz @ 10Vdc

DESCRIPTION

These two devices each consist of a 5-stage Johnson decade counter and an output decoder which converts the Johnson code to a 7-segment decoded output for driving each stage in a numerical display. A "high" Reset signal clears the decade counter to its zero count. The counters have interchangeable Clock and Clock Enable lines for incrementing on either a positive-going or negative-going transition, respectively. Antilock gating is provided on the Johnson counter, thus assuring proper counting sequence. The Carry-Out (C_{OUT}) signal completes one cycle every ten clock input cycles and is used to directly clock the succeeding decade in a multi-decade counting chain.

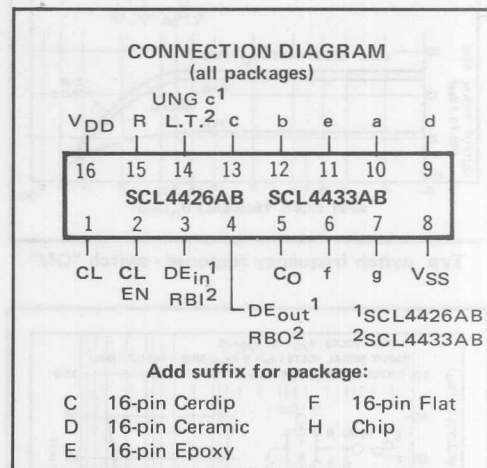
SCL4426AB

When the Display Enable is "low" the seven decoded outputs are forced off regardless of the state of the counter. Activation of the display only when required results in significant power savings. This system also facilitates implementation of display-character multiplexing.

The Carry Out and ungated "C-segment" signals are not gated by the Display Enable and therefore are available continuously. This feature is a requirement in implementation of certain divider functions such as divide-by-60 and divide-by-12.

SCL4433AB

The SCL4433AB has provisions for automatic blanking of the nonsignificant zeros in a multi-digit decimal number which results in an easily readable display consistent with normal writing practice. For example, the number 0050.0700 in an eight-digit display would be displayed as 50.07. Zero suppression on the integer side is obtained by connecting the RBI terminal of the SCL4433AB associated with the most significant digit in the display to a "low-level" voltage and connecting the RBO terminal of that stage to the RBI terminal of the SCL4433AB in the next-lower significant position in the display. This procedure is continued for each succeeding SCL4433AB on the integer side of the display. On the fraction side of the display



RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

play the RBI of the SCL4433AB associated with the least significant digit is connected to a "low level" voltage and the RBO of the SCL4433AB is connected to the RBI terminal of the SCL4433AB in the next more-significant-digit position. Again, this procedure is continued for all SCL4433AB on the fraction side of the display.

In a purely fractional number the zero immediately preceding the decimal point can be displayed by connecting the RBI of that stage to a "high-level" voltage (instead of to the RBO of the next more-significant stage). For Example: optional zero - 0.7346.

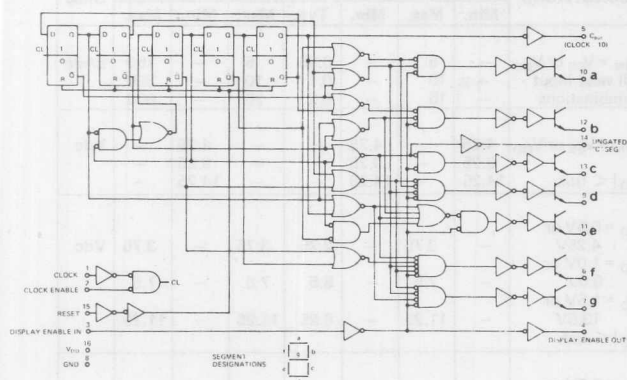
Likewise, the zero in a number such as 736.0 can be displayed by connecting the RBI of the SCL4433AB associated with it to a "high-level" voltage.

A "high" Lamp Test signal turns on all outputs.

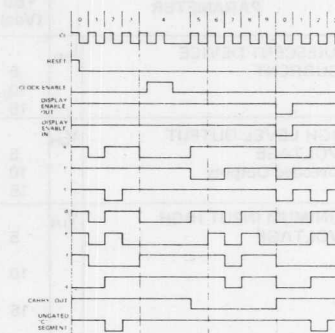
BIPOLAR OUTPUTS

These devices are functionally and pin-for-pin interchangeable with all CMOS device types SCL 4026AB and SCL4033AB. All counting and decoding in SCL4426AB and SCL4433AB devices is implemented with CMOS transistor circuitry. In order to furnish higher output drive for applications such as driving LED's, bipolar Darlington transistors have been furnished at each display drive output.

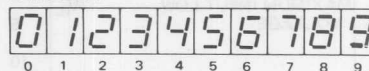
LOGIC DIAGRAM



TIMING DIAGRAM



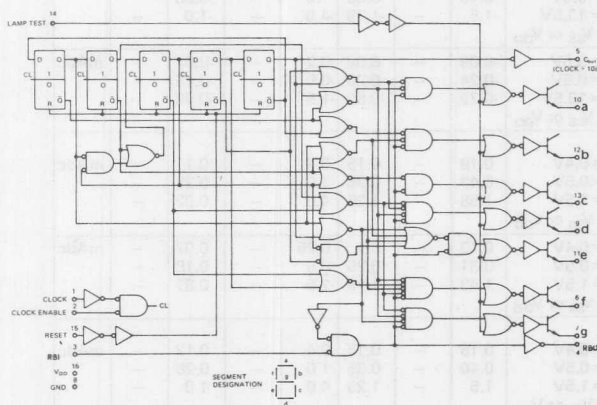
DISPLAY



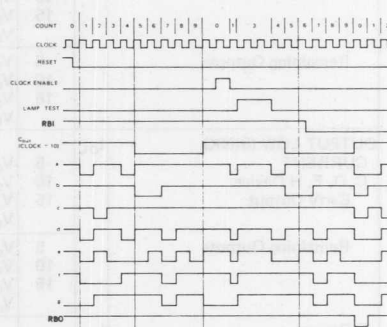
Collector of each output transistor
internally tied to V_{DD} .

SCL4426AB Decade Counter/7-Segment Decoder/Driver with Display Enable.

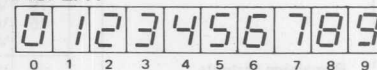
LOGIC DIAGRAM



TIMING DIAGRAM



DISPLAY



Collector of each output transistor
internally tied to V_{DD} .

SCL4433AB Decade Counter/7-Segment Decoder/Driver with Ripple Blanking.

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS^{1, 3}

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	5 V _{IN} = V _{SS} or V _{DD}	—	5	—	0.05	5	—	150	μAdc
		10 All valid input combinations	—	10	—	0.1	10	—	300	
		15	—	15	—	0.2	20	—	600	
HIGH LEVEL OUTPUT VOLTAGE Decoded Outputs	V _{OH}	5 V _{IN} = V _{SS} or V _{DD}	4.25	—	4.25	—	—	4.25	—	Vdc
		10	9.25	—	9.25	—	—	9.25	—	
		15 I _O < 1μA	14.25	—	14.25	—	—	14.25	—	
MINIMUM INPUT HIGH VOLTAGE	V _{IH}	5 V _O = 0.5V or 4.25V	—	3.75	—	2.75	3.75	—	3.75	Vdc
		10 V _O = 1.0V or 9.0V	—	7.5	—	5.5	7.5	—	7.5	
		15 V _O = 1.5V or 13.5V	—	11.25	—	8.25	11.25	—	11.25	
		I _O < 1μA	—	—	—	—	—	—	—	
MAXIMUM INPUT LOW VOLTAGE	V _{IL}	5 V _O = 0.5V or 4.25V	1.25	—	1.25	2.25	—	1.25	—	Vdc
		10 V _O = 1.0V or 9.0V	2.5	—	2.5	4.5	—	7.5	—	
		15 V _O = 1.5V or 13.5V	3.75	—	3.75	6.75	—	3.75	—	
		I _O < 1μA	—	—	—	—	—	—	—	
OUTPUT HIGH (SOURCE) CURRENT Decoded Outputs ³	I _E	5 V _{OH} = 3.5V	—	—	-15	-25	—	—	—	mAdc
		10 V _{OH} = 8.5V	—	—	—	-60	—	—	—	
		15 V _{OH} = 13.5V	—	—	—	-100	—	—	—	
C, D, F, H Device: Carry Output	I _{OH}	5 V _{OH} = 4.6V	-0.19	—	-0.15	-0.4	—	-0.11	—	mAdc
		10 V _{OH} = 9.5V	-0.43	—	-0.35	-1.0	—	-0.25	—	
		15 V _{OH} = 13.5V V _{IN} = V _{SS} or V _{DD}	-1.58	—	-1.25	-4.0	—	-0.92	—	
	Remaining Outputs	5 V _{OH} = 4.6V	-0.10	—	-0.08	-0.2	—	-0.06	—	mAdc
		10 V _{OH} = 9.5V	-0.25	—	-0.20	-0.5	—	-0.14	—	
		15 V _{OH} = 13.5V V _{IN} = V _{SS} or V _{DD}	-0.75	—	-0.60	-1.5	—	-0.42	—	
E Device: Carry Output	I _{OH}	5 V _{OH} = 4.6V	-0.18	—	-0.15	-0.4	—	-0.12	—	mAdc
		10 V _{OH} = 9.5V	-0.40	—	-0.35	-1.0	—	-0.28	—	
		15 V _{OH} = 13.5V V _{IN} = V _{SS} or V _{DD}	-1.5	—	-1.25	-4.0	—	-1.0	—	
	Remaining Outputs	5 V _{OH} = 3.5V	-0.09	—	-0.08	-0.2	—	-0.07	—	mAdc
		10 V _{OH} = 9.5V	-0.24	—	-0.20	-0.5	—	-0.16	—	
		15 V _{OH} = 13.5V V _{IN} = V _{SS} or V _{DD}	-0.72	—	-0.60	-1.5	—	-0.48	—	
OUTPUT LOW (SINK) CURRENT C, D, F, H Device: Carry Output	I _{OL}	5 V _{OL} = 0.4V	0.19	—	0.15	0.4	—	0.11	—	mAdc
		10 V _{OL} = 0.5V	0.43	—	0.35	1.0	—	0.25	—	
		15 V _{OL} = 1.5V V _{IN} = V _{SS} or V _{DD}	1.58	—	1.25	4.0	—	0.92	—	
	Remaining Outputs	5 V _{OL} = 0.4V	0.13	—	0.1	0.25	—	0.07	—	mAdc
		10 V _{OL} = 0.5V	0.31	—	0.25	0.6	—	0.18	—	
		15 V _{OL} = 1.5V V _{IN} = V _{SS} or V _{DD}	1.43	—	1.15	2.5	—	0.81	—	
E Device: Carry Output	I _{OL}	5 V _{OL} = 0.4V	0.18	—	0.15	0.4	—	0.12	—	mAdc
		10 V _{OL} = 0.5V	0.40	—	0.35	1.0	—	0.28	—	
		15 V _{OL} = 1.5V V _{IN} = V _{SS} or V _{DD}	1.5	—	1.25	4.0	—	1.0	—	
	Remaining Outputs	5 V _{OL} = 0.4V	0.12	—	0.1	0.25	—	0.08	—	mAdc
		10 V _{OL} = 0.5V	0.30	—	0.25	0.6	—	0.20	—	
		15 V _{OL} = 1.5V	1.36	—	1.15	2.5	—	0.94	—	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

² T_{LOW} = -55°C for C, D, F, H device.

= -40°C for E device.

T_{HIGH} = +125°C for C, D, F, H device.

= + 85°C for E device.

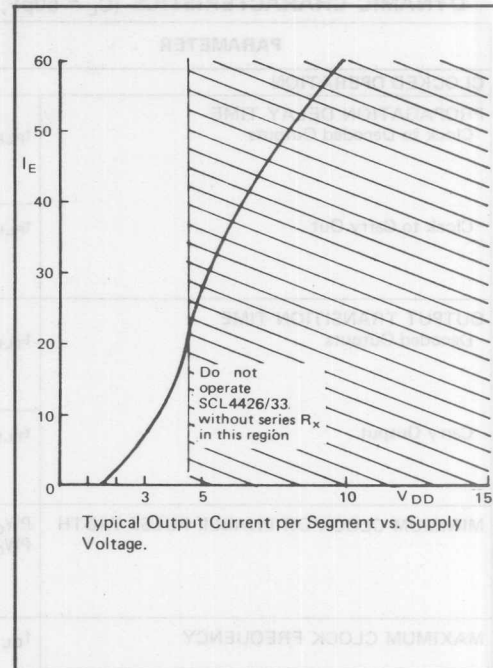
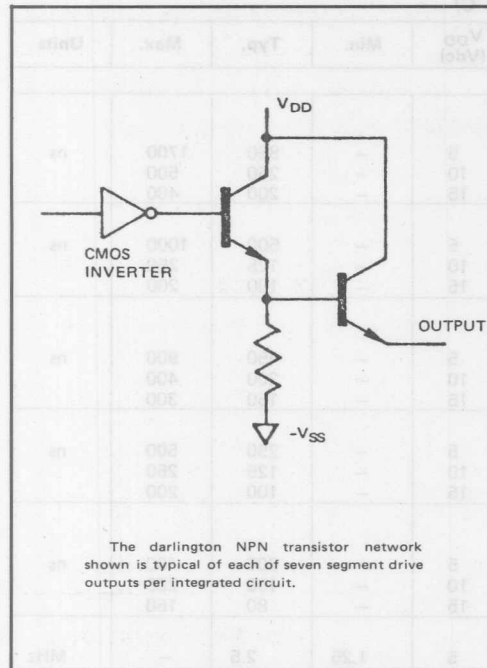
³ Observe Package Power Dissipation rating.

ELECTRICAL CHARACTERISTICS (Continued)

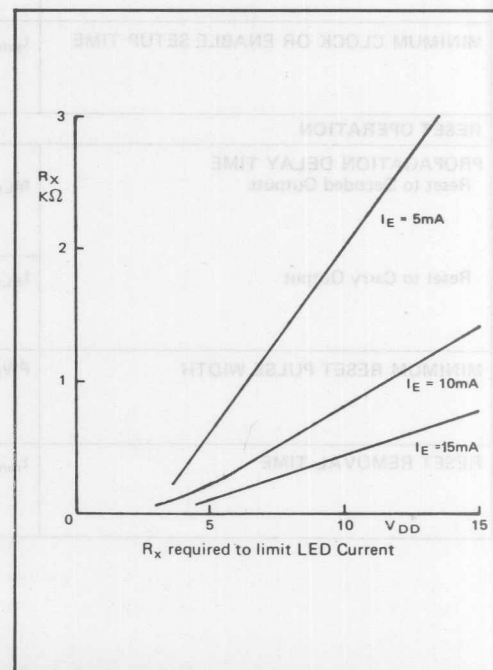
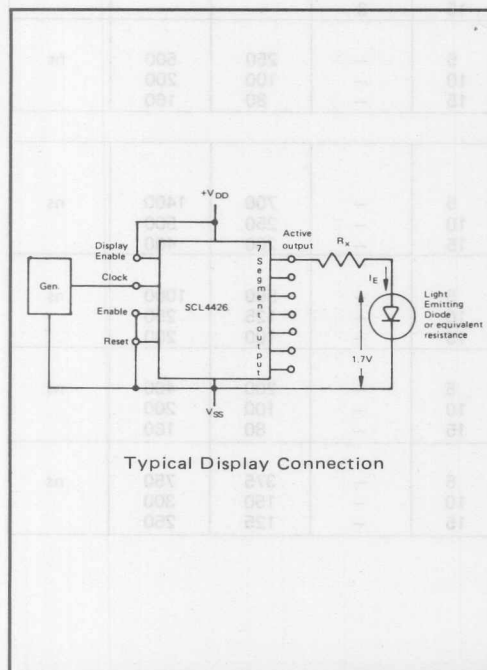
DYNAMIC CHARACTERISTICS ($C_L = 50\text{pF}$, $T_A = 25^\circ\text{C}$)

PARAMETER		V _{DD} (V _{dc})	Min.	Typ.	Max.	Units	
CLOCKED OPERATION							
PROPAGATION DELAY TIME Clock to Decoded Outputs	t _{PLH} , t _{PHL}	5	—	850	1700	ns	
		10	—	250	500		
		15	—	200	400		
	Clock to Carry Out	t _{PLH} , t _{PHL}	5	—	500	1000	ns
			10	—	125	250	
			15	—	100	200	
OUTPUT TRANSITION TIME Decoded Outputs	t _{TLH} , t _{THL}	5	—	450	900	ns	
		10	—	200	400		
		15	—	150	300		
	Carry Output	t _{TLH} , t _{THL}	5	—	250	500	ns
			10	—	125	250	
			15	—	100	200	
MINIMUM CLOCK OR ENABLE PULSE WIDTH	PW _{CL} , PW _{CE}	5	—	200	400	ns	
		10	—	100	200		
		15	—	80	160		
MAXIMUM CLOCK FREQUENCY	f _{CL}	5	1.25	2.5	—	MHz	
		10	2.5	5.0	—		
		15	3.0	6.0	—		
MAXIMUM CLOCK OR ENABLE RISE AND FALL TIME	t _{rCL} , t _{fCL}	5	15	—	—	μs	
		10	15	—	—		
		15	3	—	—		
MINIMUM CLOCK OR ENABLE SETUP TIME	t _{setup}	5	—	250	500	ns	
		10	—	100	200		
		15	—	80	160		
RESET OPERATION							
PROPAGATION DELAY TIME Reset to Decoded Outputs	t _{PLH} , t _{PHL}	5	—	700	1400	ns	
		10	—	250	500		
		15	—	200	400		
	Reset to Carry Output	t _{PLH} , t _{PHL}	5	—	500	1000	ns
			10	—	125	250	
			15	—	100	200	
MINIMUM RESET PULSE WIDTH	PW _R	5	—	200	400	ns	
		10	—	100	200		
		15	—	80	160		
RESET REMOVAL TIME	t _{rem}	5	—	375	750	ns	
		10	—	150	300		
		15	—	125	250		

OUTPUT NETWORK



DISPLAY INTERFACE





FEATURES

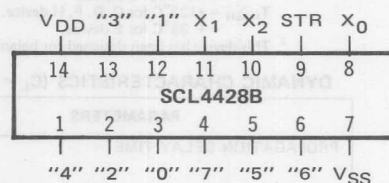
- ◆ Binary-to-Octal Decoding
- ◆ Buffered Outputs Go High on Selection
- ◆ Strobe Input for Simple Expansion
- ◆ Balanced Output Drive Current Specification

DESCRIPTION

The SCL4428B is a one-of-eight CMOS Strobed Decoder. The three inputs labeled X_0 , X_1 , and X_2 , constitute a three-bit word which defines a number from 0 to 7, and activates one of eight outputs of the decoder. The Strobe line inhibits the outputs from responding to the inputs. If the Strobe line is a logic "1", one of eight outputs is a logic "1". This is an important feature of the Strobe since many SCL4428B's may be cascading to produce a 1 or N X 8 strobed decoder. This array is particularly useful in expanding memory systems.

TRUTH TABLE — Strobe at Logical 1

Address Input				Output							
	X_2	X_1	X_0	"0"	"1"	"2"	"3"	"4"	"5"	"6"	"7"
PIN	10	11	8	3	12	2	13	1	5	6	4
	0	0	0	1	0	0	0	0	0	0	0
	0	0	1	0	1	0	0	0	0	0	0
	0	1	0	0	0	0	1	0	0	0	0
	0	1	1	0	0	0	1	0	0	0	0
	1	0	0	0	0	0	0	1	0	0	0
	1	0	1	0	0	0	0	0	1	0	0
	1	1	0	0	0	0	0	0	0	1	0
	1	1	1	0	0	0	0	0	0	0	1

CONNECTION DIAGRAM
(all packages)

Add suffix for package:

- C 14-pin Cerdip
- D 14-pin Ceramic
- E 14-pin Epoxy
- F 14-pin Flat
- H Chip

RECOMMENDED OPERATING CONDITIONS

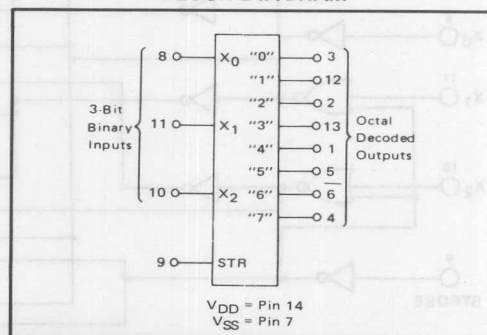
For maximum reliability:

DC Supply Voltage $V_{DD} - V_{SS}$ 3 to 15 VdcOperating Temperature T_A

C, D, F, H Device -55 to +125 °C

E Device -40 to +85 °C

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS^{1,3}

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	V _{IN} = V _{SS} or V _{DD} All valid input combinations	—	5	—	0.05	5	—	150	μAdc
	10		—	10	—	0.1	10	—	300	
	15		—	20	—	0.2	20	—	600	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

² T_{LOW} = -55°C for C, D, F, H device.

= -40°C for E device.

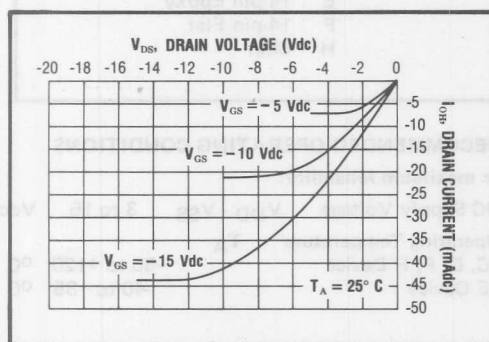
T_{HIGH} = +125°C for C, D, F, H device.

= + 85°C for E device.

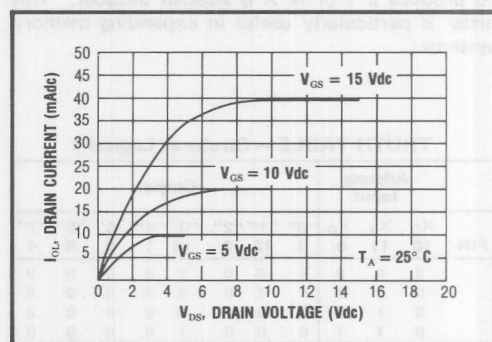
³ This device has been designed for balanced output drive current specifications. Consult Family Specifications.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETERS		V _{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME	t _{PLH} , t _{PHL}	5	—	225	450	ns
		10	—	100	200	
		15	—	70	140	
OUTPUT TRANSITION TIME	t _{TLH} , t _{THL}	5	—	100	200	ns
		10	—	50	100	
		15	—	40	80	

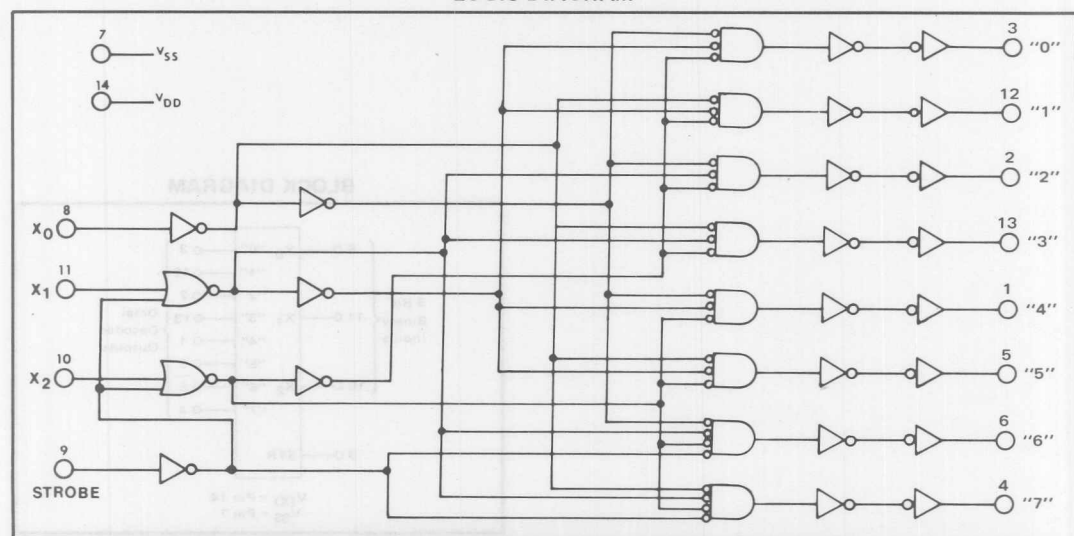


Typical P-Channel
Source Current Characteristics

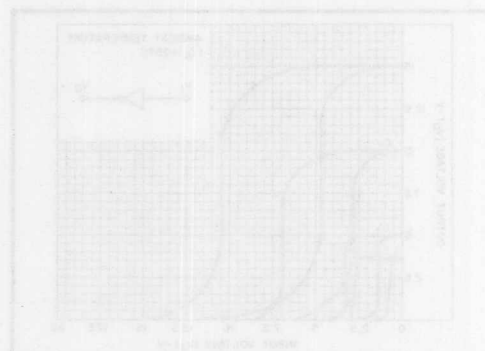
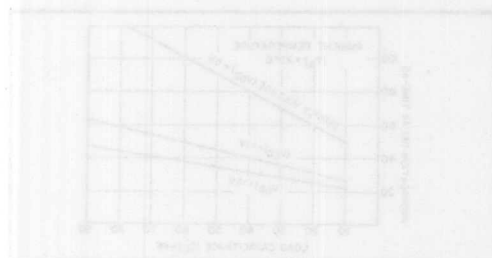
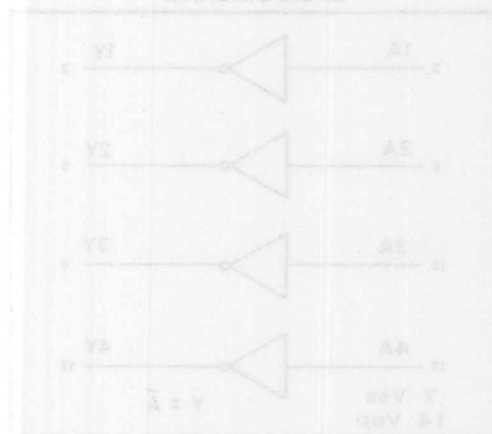
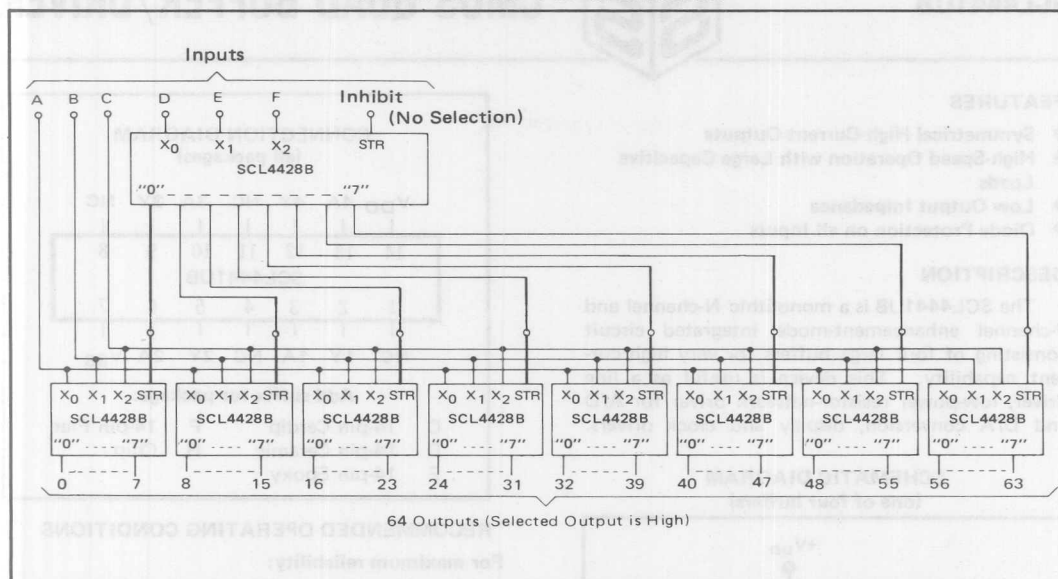


Typical N-Channel
Sink Current Characteristics

LOGIC DIAGRAM



APPLICATIONS INFORMATIONSIX-BIT BINARY 1-OF-64 DECODER





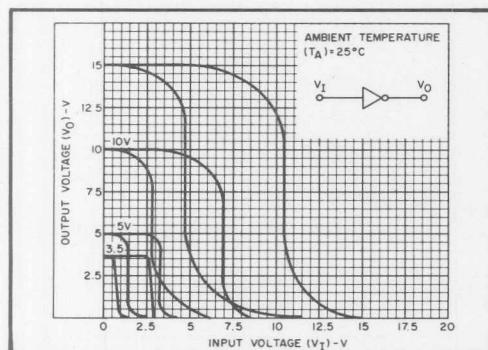
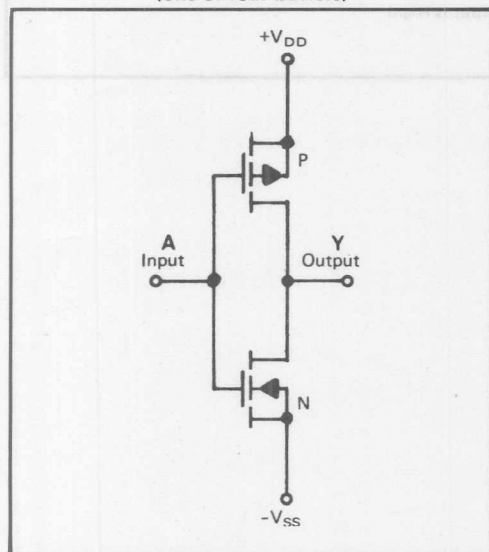
FEATURES

- ◆ Symmetrical High-Current Outputs
- ◆ High-Speed Operation with Large Capacitive Loads
- ◆ Low Output Impedance
- ◆ Diode Protection on all Inputs

DESCRIPTION

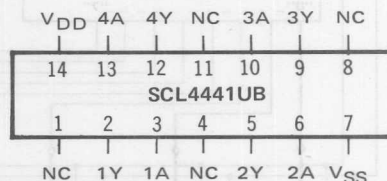
The SCL4441UB is a monolithic N-channel and P-channel enhancement-mode integrated circuit consisting of four large buffers for very high current capability. This device is useful as a line driver, low-power resistor-network driver for A/D and D/A conversion, display and clock drivers.

SCHEMATIC DIAGRAM
(one of four buffers)



Minimum and maximum transfer characteristics.

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

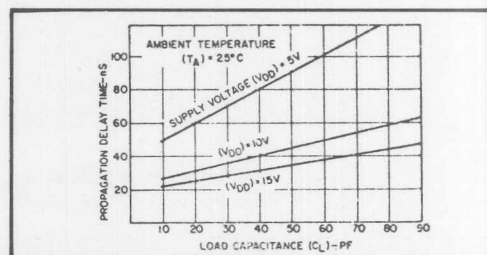
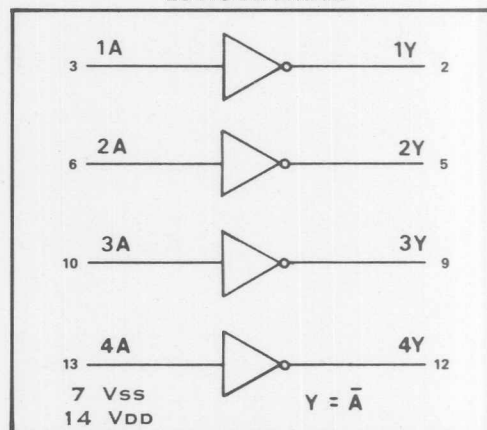
C	14-pin Cerdip	F	14-pin Flat
D	14-pin Ceramic	H	Chip
E	14-pin Epoxy		

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A	-55 to +125	°C
C, D, F, H Device		-40 to +85	°C
E Device			

LOGIC DIAGRAM



Typical propagation delay time vs. C_L

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS¹

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	V _{IN} = V _{SS} or V _{DD} All valid input combinations	—	1.0	—	0.005	1.0	—	30	μAdc
			—	2.0	—	0.01	2.0	—	60	
			—	4.0	—	0.02	4.0	—	120	
OUTPUT HIGH (SOURCE) CURRENT C, D, F, H device	I _{OH}	V _{OH} = 4.6V V _{OH} = 9.5V V _{OH} = 13.5V V _{IN} = V _{SS}	-2.5	—	-2.0	-4.5	—	-1.4	—	mAdc
			-7.3	—	-5.8	-14.0	—	-4.0	—	
			-23.1	—	-18.5	-45	—	-13.0	—	
E device	I _{OH}	V _{OH} = 4.6V V _{OH} = 9.5V V _{OH} = 13.5V V _{IN} = V _{SS}	-2.4	—	-2.0	-4.5	—	-1.6	—	mAdc
			-7.0	—	-5.8	-14.0	—	-4.6	—	
			-22.2	—	-18.5	-45	—	-14.8	—	
OUTPUT LOW (SINK) CURRENT C, D, F, H device	I _{OL}	V _{OL} = 0.4V V _{OL} = 0.5V V _{OL} = 1.5V V _{IN} = V _{DD}	3.0	—	2.4	4.5	—	1.7	—	mAdc
			8.7	—	7.0	14.0	—	4.9	—	
			33	—	27	45	—	19	—	
E device	I _{OL}	V _{OL} = 0.4V V _{OL} = 0.5V V _{OL} = 1.5V V _{IN} = V _{DD}	2.8	—	2.4	4.5	—	2.0	—	mAdc
			8.4	—	7.0	14.0	—	5.6	—	
			32	—	27	45	—	22	—	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

² T_{LOW} = -55°C for C, D, F, H device.

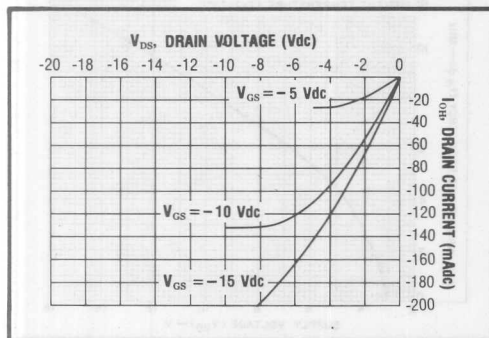
= -40°C for E device.

T_{HIGH} = +125°C for C, D, F, H device.

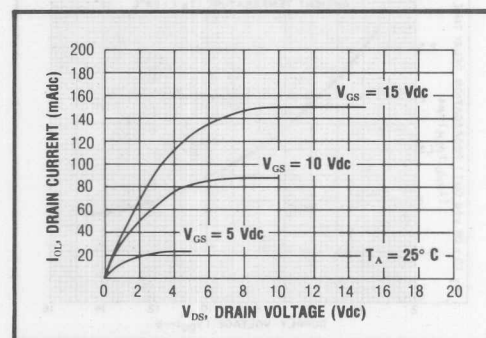
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V _{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME	t _{PLH} , t _{PHL}	5	—	90	180	ns
		10	—	45	90	
		15	—	35	70	
OUTPUT TRANSITION TIME	t _{TLH} , t _{THL}	5	—	90	180	ns
		10	—	45	90	
		15	—	35	70	



Typical P-Channel
Source Current Characteristics



Typical N-Channel
Sink Current Characteristics



FEATURES

- ◆ Low Duty Cycle Push-Pull Outputs
- ◆ Balanced Output Drive Current Specifications
- ◆ Inverter on Chip for Crystal Oscillator Circuit
- ◆ Buffered Output Available for Trimming Oscillator
- ◆ 21 Fully Static Stages
- ◆ 10MHz Counting Rate @ 10Vdc

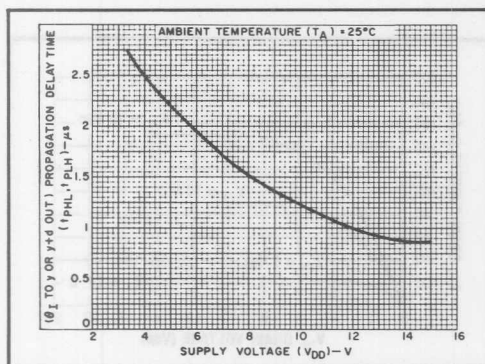
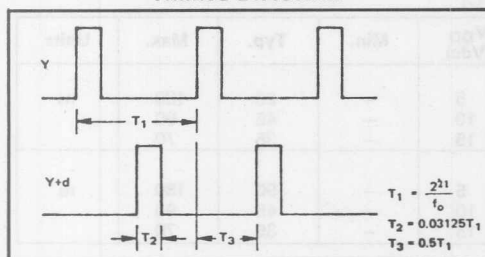
DESCRIPTION

The SCL4445B monolithic aluminum gate CMOS integrated circuit consists of an oscillator inverter, 21 toggle flip-flops, and two flip-flops used to produce a 3.125% duty cycle output wave-form. Push-pull operation is provided by the inverter output buffers. A divide-by-4 frequency output is provided as an oscillator monitor or subsidiary high frequency output.

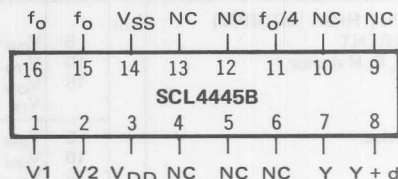
The SCL4445B is especially suited for low-power timekeeping applications such as desk or wall clocks, automobile clocks, and digital timing references. Its output is suitable for driving miniature synchronous motors, stepping motors, or external bipolar transistors in push-push fashion.

The SCL4445B is pin compatible with device type CD4045A. The extra function $f_o/4$ is provided on pin 11.

TIMING DIAGRAM



Typical propagation delay (f_o to y or y + d out) vs. V_{DD} . ($C_L = 50pF$).

CONNECTION DIAGRAM
(all packages)

Add suffix for package:

C	16-pin Cerdip
D	16-pin Ceramic
E	16-pin Epoxy
F	16-pin Flat
H	Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

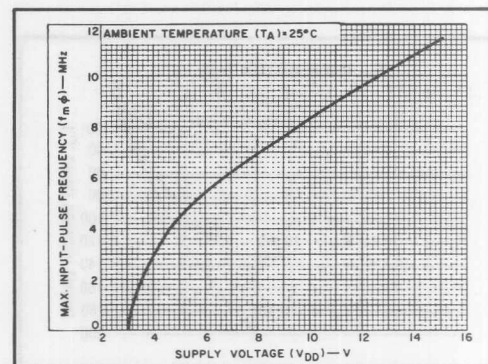
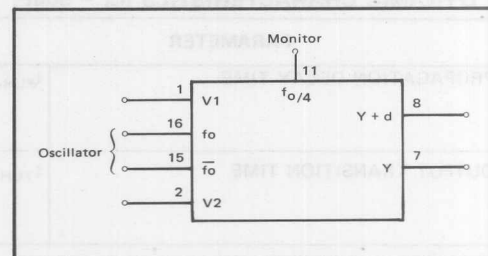
DC Supply Voltage $V_{DD} - V_{SS}$ 3 to 15 Vdc

Operating Temperature T_A

C, D, F, H Device -55 to +125 °C

E Device -40 to +85 °C

LOGIC DIAGRAM



Typical f_o vs. V_{DD} ($C_L = 50pF$).

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS^{1, 3}

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	V _{IN} = V _{SS} or V _{DD} All valid input combinations	—	5	—	0.05	5	—	150	μA _{dc}
			—	10	—	0.1	10	—	300	
			—	20	—	0.2	20	—	600	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

² T_{LOW} = -55°C for C, D, F, H device.

= -40°C for E device.

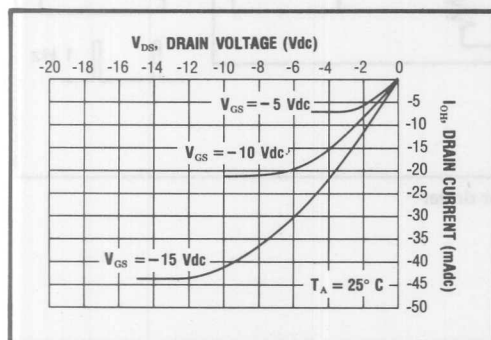
T_{HIGH} = +125°C for C, D, F, H device.

= + 85°C for E device.

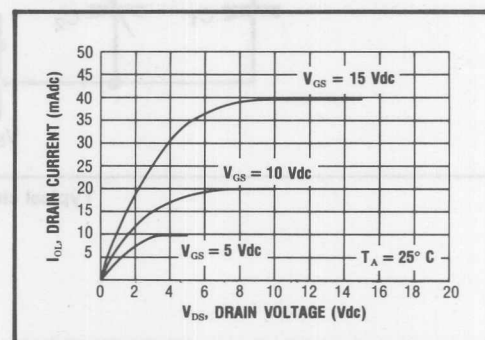
³ This device has been designed for balanced output drive current specifications. Consult Family Specifications.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V _{DD} (Vdc)	Min.	Typ.	Max.	Units
OUTPUT TRANSITION TIME	t _{TLH} , t _{THL}	5	—	100	200	ns
		10	—	50	100	
		15	—	40	80	
MAXIMUM CLOCK FREQUENCY	f _{CL}	5	2.5	5	—	MHz
		10	4.5	9	—	
		15	5.5	11	—	
MAXIMUM CLOCK RISE AND FALL TIME	t _{rCL} , t _{fCL}	5	15	—	—	μs
		10	15	—	—	
		15	5	—	—	

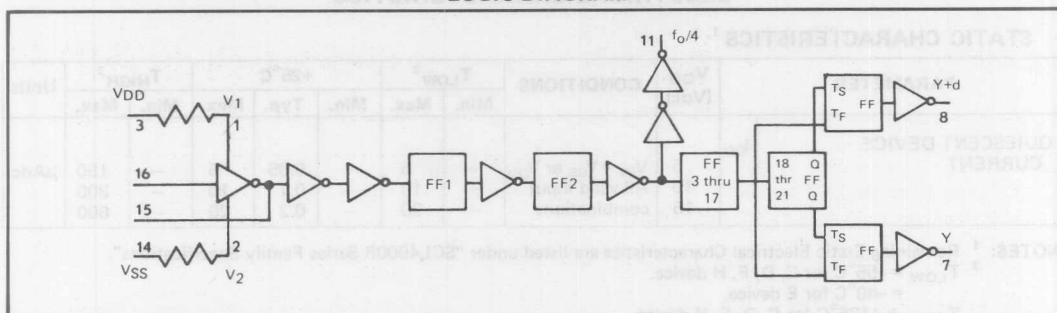


Typical P-Channel
Source Current Characteristics



Typical N-Channel
Sink Current Characteristics

LOGIC DIAGRAM



APPLICATIONS INFORMATION

RECOMMENDED CIRCUIT
FOR 2.097152 MHz OSCILLATOR

$$R_1 = 10 \text{ M}\Omega$$

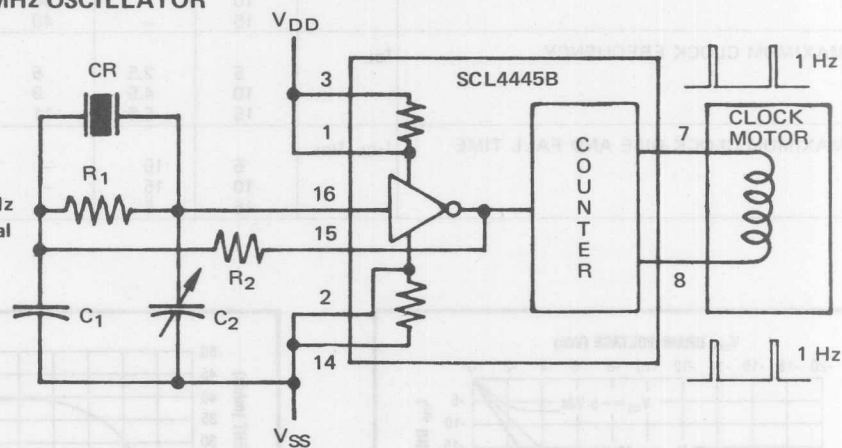
$$R_2 = 2 \text{ K}\Omega$$

$$C_1 = 120 \text{ pF}$$

$$C_2 = 5\text{-}30 \text{ pF}$$

$$CR = 2.097152 \text{ MHz}$$

Quartz Crystal



Typical clock motor driver

SCL4449UB



CMOS HEX INVERTER

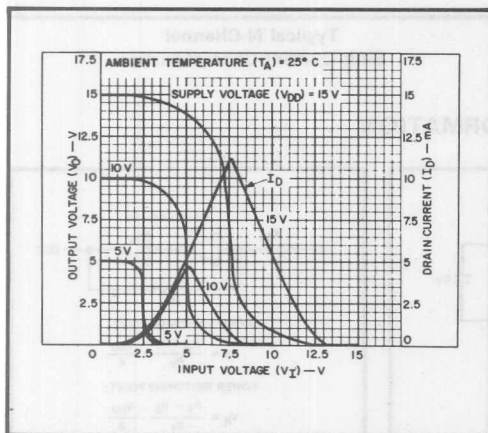
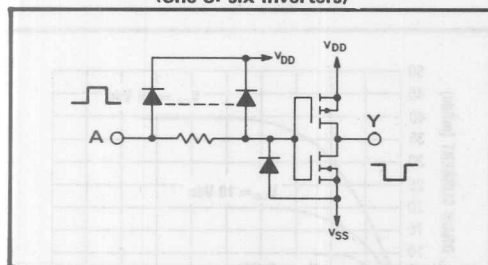
FEATURES

- ◆ All Inputs Fully Diode-Protected
- ◆ Pin Compatible with SCL4009B, SCL4049B
- ◆ Fully "B"-Series Compatible
- ◆ Balanced Output Drive Current Specifications

DESCRIPTION

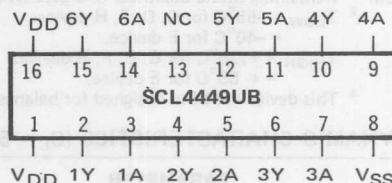
The SCL4449UB consists of six CMOS inverter circuits. It is pin-compatible with the SCL4009UB, SCL4049UB, and equivalent device types. In systems which do not require the high output current and level-shifting capabilities of the buffers, the less expensive SCL4449 can be substituted directly with no change in board layout. The device is particularly useful for quasi-linear circuits, such as oscillators and multivibrators.

SCHEMATIC DIAGRAM (one of six inverters)



Typical current and voltage transfer characteristics.

CONNECTION DIAGRAM (all packages)



Add suffix for package:

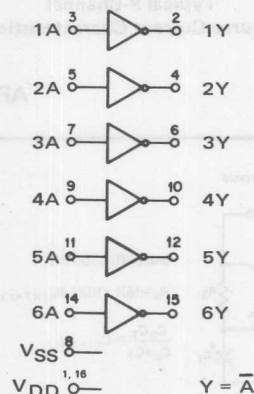
- C 16-pin Cerdip
- D 16-pin Ceramic
- E 16-pin Epoxy
- F 16-pin Flat
- H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

LOGIC DIAGRAM



		(Vdc)									Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.		
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN} = V_{SS}$ or V_{DD}	—	0.05	—	0.0005	0.05	—	1.5	μA_{dc}
		10	All valid input combinations	—	0.10	—	0.001	0.10	—	3.0	
		15		—	0.20	—	0.002	0.20	—	6.0	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

² $T_{LOW} = -55^{\circ}C$ for C, D, F, H device.

$= -40^{\circ}C$ for E device.

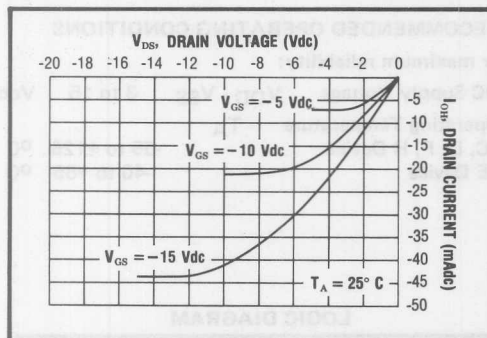
$T_{HIGH} = +125^{\circ}C$ for C, D, F, H device.

$= +85^{\circ}C$ for E device.

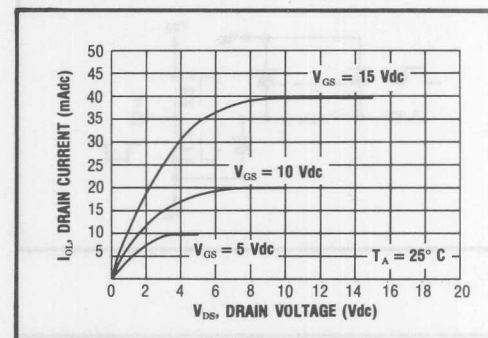
³ This device has been designed for balanced output drive current specifications. Consult Family Specifications.

DYNAMIC CHARACTERISTICS ($C_L = 50pF$, $T_A = 25^{\circ}C$)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME	t_{PLH}, t_{PHL}	5	—	60	120	ns
		10	—	30	60	
		15	—	25	50	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	—	100	200	ns
		10	—	50	100	
		15	—	40	80	

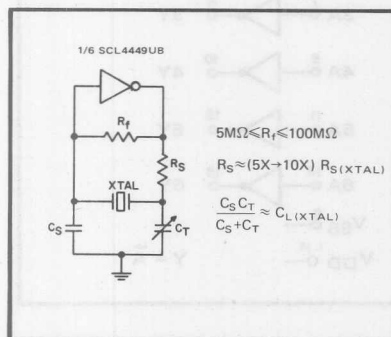


Typical P-Channel
Source Current Characteristics

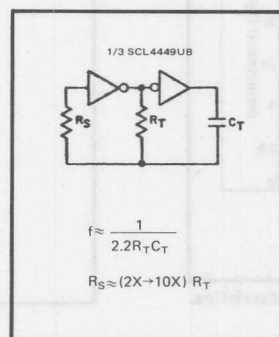


Typical N-Channel
Sink Current Characteristics

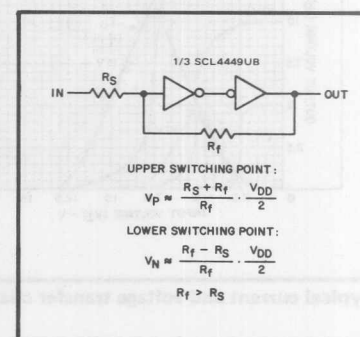
APPLICATIONS INFORMATION



Typical crystal oscillator circuit



Typical RC oscillator circuit



Input pulse shaping circuit (Schmitt trigger)

SCL4502B



CMOS STROBED HEX INVERTER/BUFFER

FEATURES

- ◆ 3-State Outputs with Separate Disable Control
- ◆ Common Input Inhibit Line
- ◆ TTL Output Drive Guaranteed Over Temperature Range
- ◆ Output Impedance $< 200 \Omega$ @ 5Vdc Guaranteed Over Temperature Range

DESCRIPTION

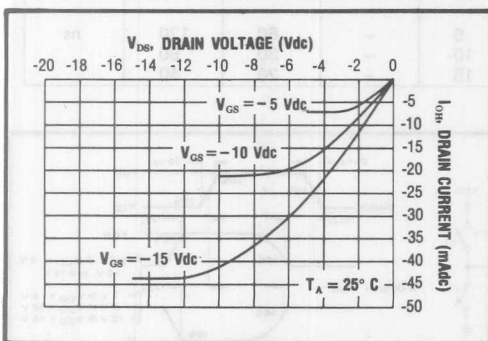
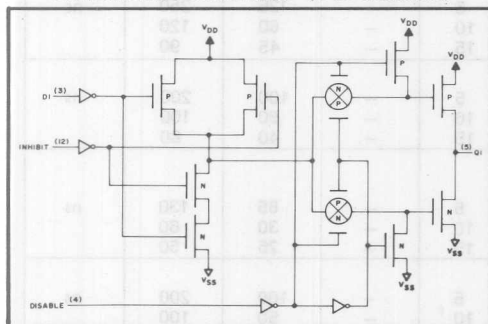
The SCL4502B is a Strobed Hex Inverter/Buffer with a common Data Input Inhibit Control and a common Output Disable Control. The 3-state output allows common bus configurations.

TRUTH TABLE

D_n	Inhibit	Disable	Q_n
0	0	0	1
1	0	0	0
X	1	0	0
X	X	1	High Impedance

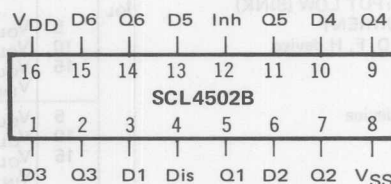
X = Don't Care

SCHEMATIC DIAGRAM (1 of 6 buffers)



Typical P-Channel
Source Current Characteristics

CONNECTION DIAGRAM (all packages)



Add suffix for package:

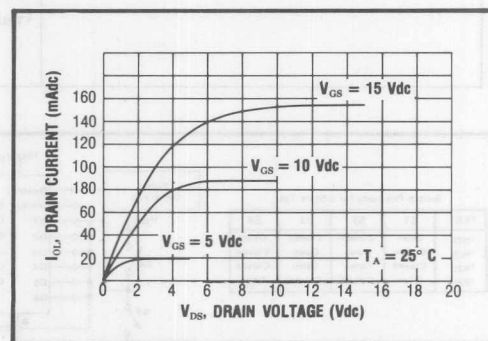
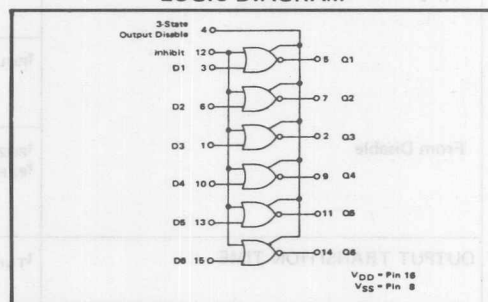
C	16-pin Cerdip	F	16-pin Flat
D	16-pin Ceramic	H	Chip
E	16-pin Epoxy		

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

LOGIC DIAGRAM



Typical N-Channel
Sink Current Characteristics

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS^{1,3}

PARAMETER		V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	5	V _{IN} = V _{SS} or V _{DD}	—	1.0	—	0.005	1.0	—	30	μAdc
		10	All valid input combinations	—	2.0	—	0.01	2.0	—	60	
		15		—	4.0	—	0.02	4.0	—	120	
OUTPUT LOW (SINK) CURRENT C, D, F, H device	I _{OL}	5	V _{OL} = 0.4V	3.5	—	2.8	5.7	—	2.0	—	mAdc
		10	V _{OL} = 0.5V	7.8	—	6.3	12.5	—	4.4	—	
		15	V _{OL} = 1.5V	29	—	24.0	49	—	16	—	
			V _{IN} = V _{SS} or V _{DD}								mAdc
		5	V _{OL} = 0.4V	3.3	—	2.8	5.7	—	2.3	—	
		10	V _{OL} = 0.5V	7.4	—	6.3	12.5	—	5.2	—	
E device		15	V _{OL} = 1.5V	28	—	24.0	49	—	19	—	mAdc
			V _{IN} = V _{SS} or V _{DD}								
3-STATE OUTPUT LEAKAGE CURRENT	I _{ZL}	15		—	±0.1	—	±10 ⁻⁴	±0.1	—	±1.0	μAdc

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

² T_{LOW} = -55°C for C, D, F, H device.

= -40°C for E device.

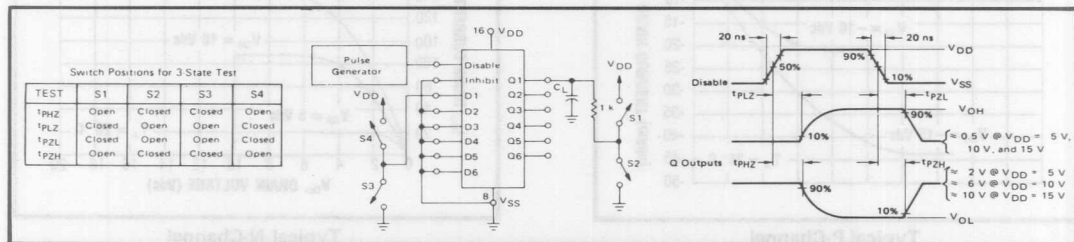
T_{HIGH} = +125°C for C, D, F, H device.

= + 85°C for E device.

³ This device has been designed to meet the balanced output drive current specification for Output High (Source) Current. Consult Family Specifications.

DYNAMIC CHARACTERISTICS ($C_L = 50\text{pF}$, $T_A = 25^\circ\text{C}$)

PARAMETER		V _{DD} (V _{DC})	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME From Data Inputs 	t _{PLH}	5 10 15	— — —	125 60 45	250 120 90	ns
	t _{PHL}	5 10 15	— — —	100 50 40	200 100 80	ns
	t _{PHZ} , t _{PLZ} t _{PZH} , t _{PZL}	5 10 15	— — —	65 30 25	130 60 50	ns
	From Disable					
OUTPUT TRANSITION TIME	t _{TLH}	5 10 15	— — —	100 50 40	200 100 80	ns
	t _{THL}	5 10 15	— — —	60 30 20	120 60 40	ns



3-State AC Test Circuit and Waveforms (tpHZ, tpZH, tpLZ, tpZL)

SCL4508B Preliminary



CMOS DUAL 4-BIT LATCH

FEATURES

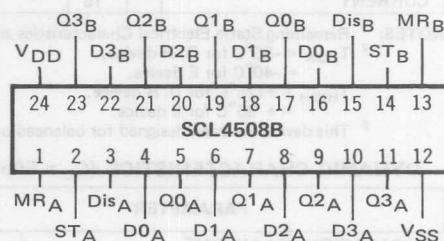
- ◆ Two Independent Four-Bit Latches
- ◆ 3-State Outputs
- ◆ Direct Reset
- ◆ All Inputs Buffered
- ◆ Balanced Output Drive Current Specifications

DESCRIPTION

The SCL4508B consists of two identical independent 4-Bit Latches with separate Strobe (ST) and Master Reset (MR) controls. Separate Disable inputs force the outputs to a high-impedance state for bus line applications.

These devices find primary use in buffer storage, holding register, and display circuits, and other general digital logic applications.

CONNECTION DIAGRAM (all packages)



Add suffix for package:

- D 24-pin Ceramic
- E 24-pin Plastic
- H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

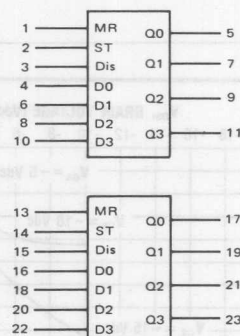
DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
D, H Device		-55 to +125	°C
E Device		-40 to +85	°C

TRUTH TABLE

MR	ST	Disable	D3	D2	D1	D0	Q3	Q2	Q1	Q0
0	1	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	1	0	0	0	1
0	1	0	0	0	1	0	0	0	1	0
0	1	0	0	1	0	0	0	1	0	0
0	1	0	1	0	0	0	1	0	0	0
0	0	0	X	X	X	X	Latched			
1	X	0	X	X	X	X	0	0	0	0
X	X	1	X	X	X	X	High Impedance			

X = Don't Care

BLOCK DIAGRAM



V_{DD} = Pin 24
 V_{SS} = Pin 12

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS^{1, 3}

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	V _{IN} = V _{SS} or V _{DD} All valid input combinations	—	5	—	0.05	5	—	150	μAdc
			—	10	—	0.1	10	—	300	
			—	20	—	0.2	20	—	600	
3-STATE OUTPUT LEAKAGE CURRENT	I _{ZL}		—	±0.1	—	±10 ⁻⁴	±0.1	—	±1.0	μAdc

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

² T_{LOW} = -55°C for D, H device.

= -40°C for E device.

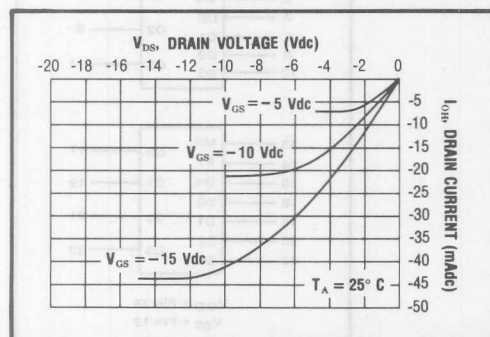
T_{HIGH} = +125°C for D, H device.

= + 85°C for E device.

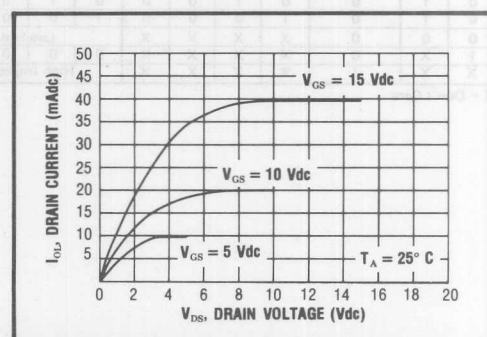
³ This device has been designed for balanced output drive current specifications. Consult Family Specifications.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V _{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME From Data Inputs	t _{PLH} , t _{PHL}	5	—	220	440	ns
		10	—	90	180	
		15	—	60	120	
From Disable Input	t _{PHZ} , t _{PLZ} t _{PZH} , t _{PZL}	5	—	85	170	ns
		10	—	45	90	
		15	—	30	60	
OUTPUT TRANSITION TIME	t _{TLH} , t _{THL}	5	—	100	200	ns
		10	—	50	100	
		15	—	40	80	
MINIMUM MASTER RESET PULSE WIDTH	PW _{MR}	5	—	100	200	ns
		10	—	50	100	
		15	—	35	70	
MINIMUM STROBE PULSE WIDTH	PW _{ST}	5	—	70	140	ns
		10	—	35	70	
		15	—	20	40	
MINIMUM SETUP TIME Data Inputs	t _{setup}	5	—	25	50	ns
		10	—	10	20	
		15	—	5	10	
MINIMUM HOLD TIME Data Inputs	t _{hold}	5	—	0	0	ns
		10	—	0	0	
		15	—	0	0	

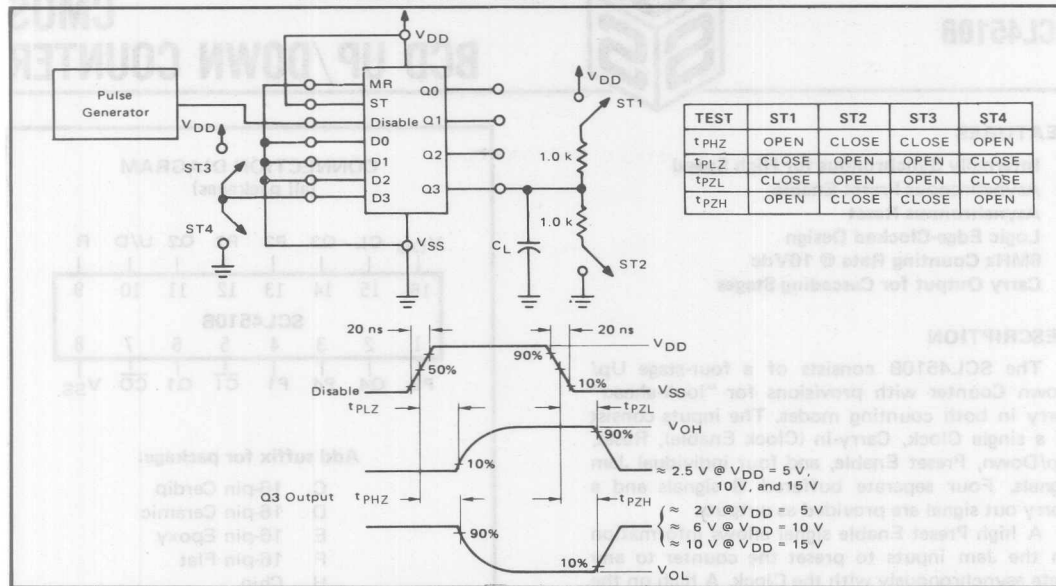


Typical P-Channel
Source Current Characteristics



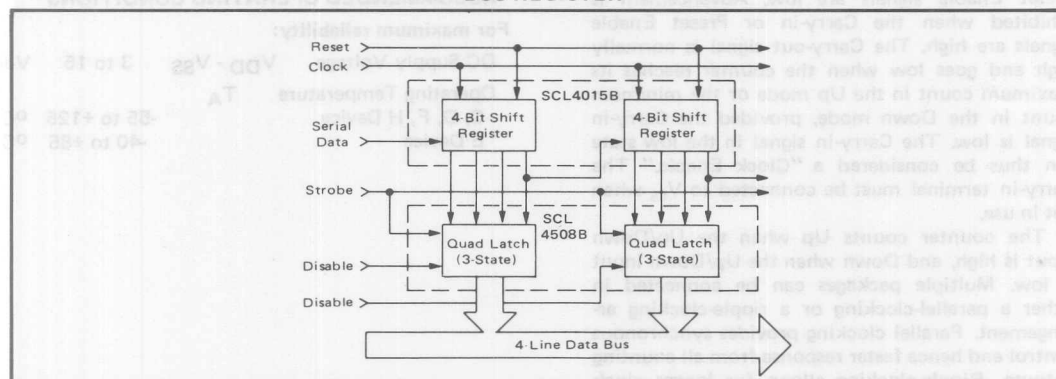
Typical N-Channel
Sink Current Characteristics

3-STATE AC TEST CIRCUIT AND WAVEFORMS

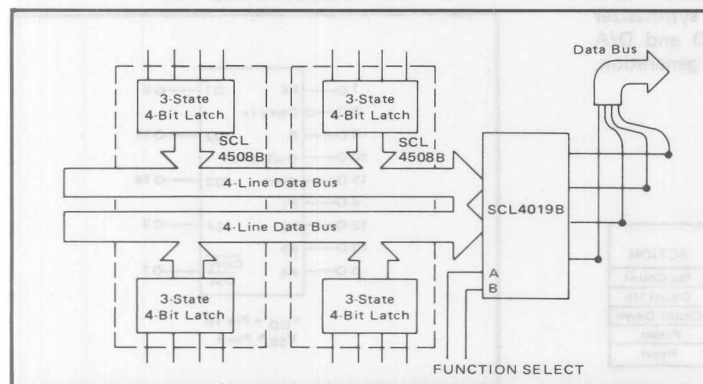


APPLICATIONS INFORMATION

BUS REGISTER



DUAL MULTIPLEXED BUS REGISTER WITH FUNCTION SELECT



FUNCTION SELECT

A	B	Function
0	0	Inhibit (all 0)
1	0	Select A Bus
0	1	Select B Bus
1	1	$A_i + B_i$



FEATURES

- ◆ Internally Synchronous for High Speed
- ◆ Asynchronous Preset Enable
- ◆ Asynchronous Reset
- ◆ Logic Edge-Clocked Design
- ◆ 6MHz Counting Rate @ 10Vdc
- ◆ Carry Output for Cascading Stages

DESCRIPTION

The SCL4510B consists of a four-stage Up/Down Counter with provisions for "look-ahead" carry in both counting modes. The inputs consist of a single Clock, Carry-in (Clock Enable), Reset, Up/Down, Preset Enable, and four individual Jam signals. Four separate buffered Q signals and a Carry out signal are provided as outputs.

A high Preset Enable signal allows information on the Jam inputs to preset the counter to any state asynchronously with the Clock. A high on the Reset line resets all stages to the "zero" state. The counter is advanced one count at the positive transition of the Clock when the Carry-in and Preset Enable signals are low. Advancement is inhibited when the Carry-in or Preset Enable signals are high. The Carry-out signal is normally high and goes low when the counter reaches its maximum count in the Up mode or the minimum count in the Down mode, provided the Carry-in signal is low. The Carry-in signal in the low state can thus be considered a "Clock Enable." The Carry-in terminal must be connected to V_{SS} when not in use.

The counter counts Up when the Up/Down input is high, and Down when the Up/Down input is low. Multiple packages can be connected in either a parallel-clocking or a ripple-clocking arrangement. Parallel clocking provides synchronous control and hence faster response from all counting outputs. Ripple-clocking allows for longer clock input rise and fall times.

This counter finds primary use in up/down and differential counting and frequency synthesizer applications. It is also useful in A/D and D/A conversion and for magnitude and sign generation.

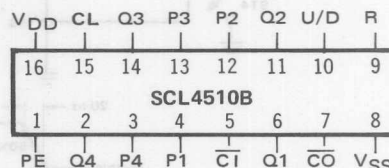
TRUTH TABLE

CARRY IN	UP/DOWN	PRESET ENABLE	RESET	ACTION
1	X	0	0	No Count
0	1	0	0	Count Up
0	0	0	0	Count Down
X	X	1	0	Preset
X	X	X	1	Reset

X = Don't Care

CONNECTION DIAGRAM

(all packages)



Add suffix for package:

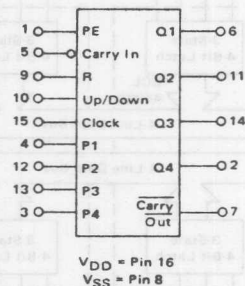
- C 16-pin Cerdip
- D 16-pin Ceramic
- E 16-pin Epoxy
- F 16-pin Flat
- H Chip

RECOMMENDED OPERATING CONDITIONS

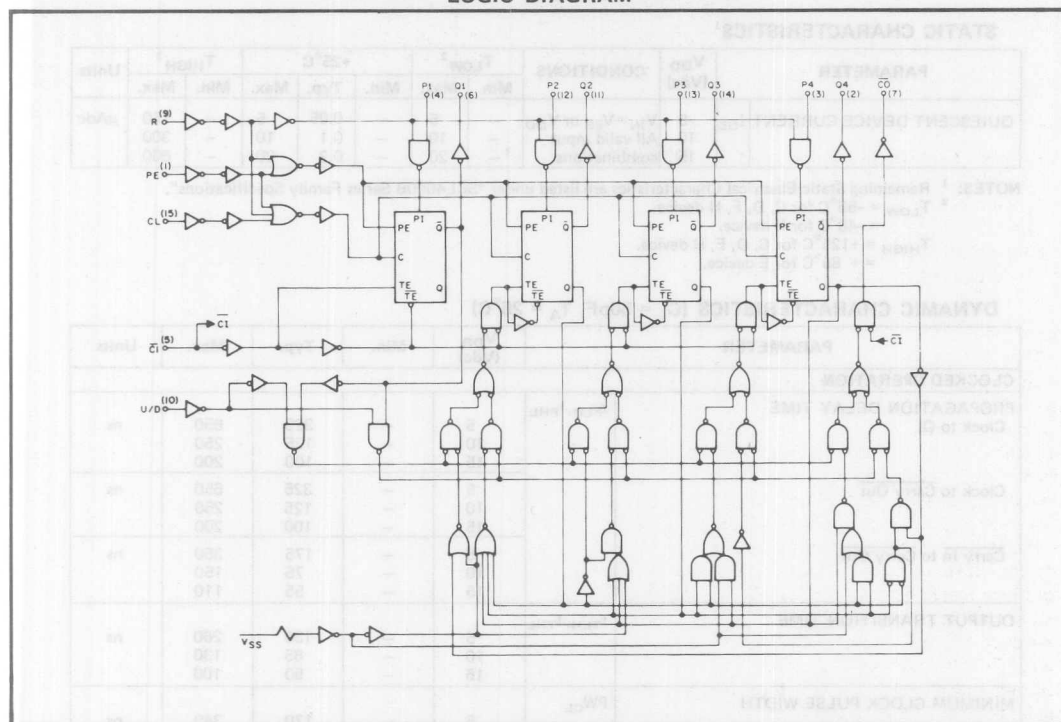
For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A	-55 to +125	°C
C, D, F, H Device		-40 to +85	°C
E Device			

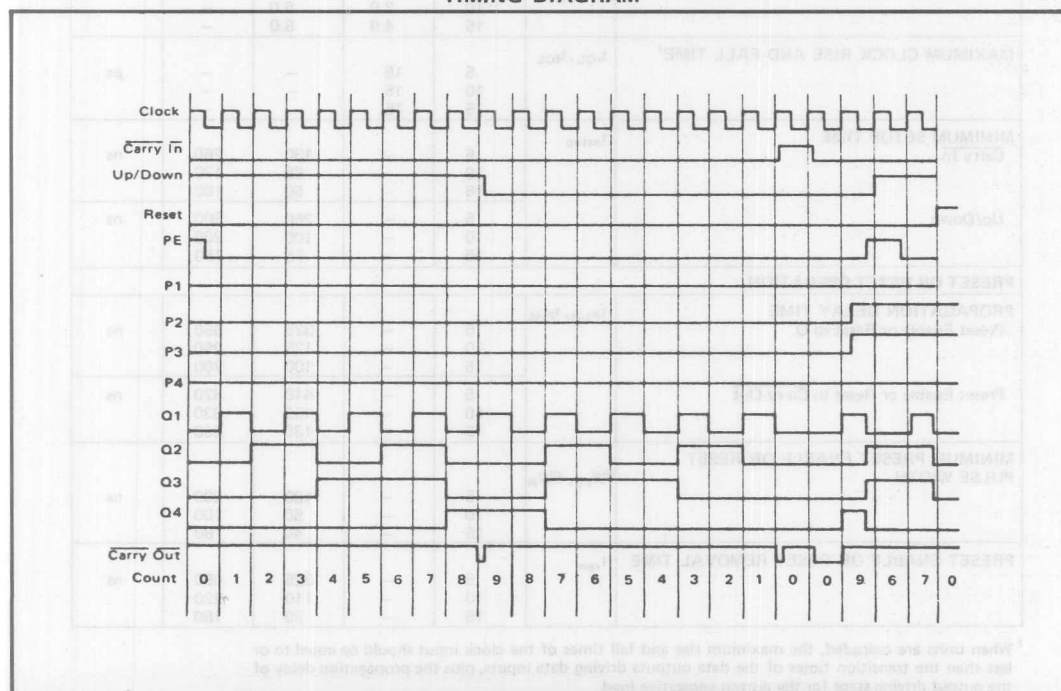
BLOCK DIAGRAM



LOGIC DIAGRAM



TIMING DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS¹

PARAMETER	V _{DD} (V _{dc})	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT I _{DD}	5	V _{IN} = V _{SS} or V _{DD}	—	5	—	0.05	5	—	150	μA _{dc}
	10	All valid input combinations	—	10	—	0.1	10	—	300	
	15		—	20	—	0.2	20	—	600	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

² T_{LOW} = -55°C for C, D, F, H device.

= -40°C for E device.

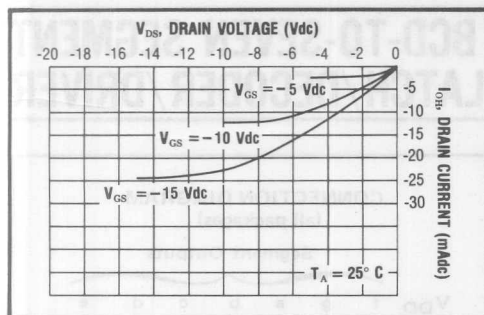
T_{HIGH} = +125°C for C, D, F, H device.

= + 85°C for E device.

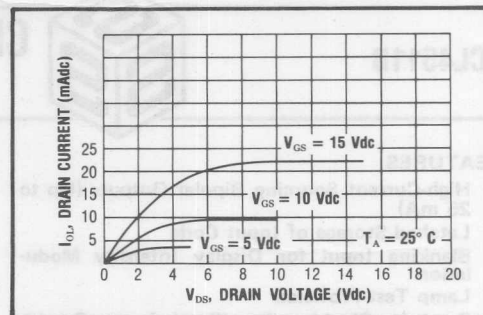
DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V _{DD} (V _{dc})	Min.	Typ.	Max.	Units	
CLOCKED OPERATION							
PROPAGATION DELAY TIME Clock to Q	t _{PLH} , t _{PHL}	5	—	325	650	ns	
		10	—	125	250		
		15	—	100	200		
	Clock to <u>Carry Out</u>		5	—	325	650	ns
			10	—	125	250	
			15	—	100	200	
	<u>Carry In</u> to <u>Carry Out</u>		5	—	175	350	ns
			10	—	75	150	
			15	—	55	110	
OUTPUT TRANSITION TIME	t _{TLH} , t _{THL}	5	—	130	260	ns	
		10	—	65	130		
		15	—	50	100		
MINIMUM CLOCK PULSE WIDTH	PW _{CL}	5	—	170	340	ns	
		10	—	85	170		
		15	—	70	140		
MAXIMUM CLOCK FREQUENCY	f _{CL}	5	1.5	3.0	—	MHz	
		10	3.0	6.0	—		
		15	4.0	8.0	—		
MAXIMUM CLOCK RISE AND FALL TIME ¹	t _{rCL} , t _{fCL}	5	15	—	—	μs	
		10	15	—	—		
		15	15	—	—		
MINIMUM SETUP TIME <u>Carry In</u>	t _{setup}	5	—	130	260	ns	
		10	—	65	130		
		15	—	50	100		
	Up/Down		5	—	250	500	ns
			10	—	100	200	
			15	—	75	150	
PRESET OR RESET OPERATION							
PROPAGATION DELAY TIME Preset Enable or Reset to Q	t _{PLH} , t _{PHL}	5	—	325	650	ns	
		10	—	125	250		
		15	—	100	200		
	Preset Enable or Reset to <u>Carry Out</u>		5	—	410	820	ns
			10	—	165	330	
			15	—	130	260	
MINIMUM PRESET ENABLE OR RESET PULSE WIDTH	PW _{PE} , PW _R	5	—	100	200	ns	
		10	—	50	100		
		15	—	40	80		
PRESET ENABLE OR RESET REMOVAL TIME	t _{rem}	5	—	325	650	ns	
		10	—	110	220		
		15	—	90	180		

¹ When units are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the transition times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitive load.



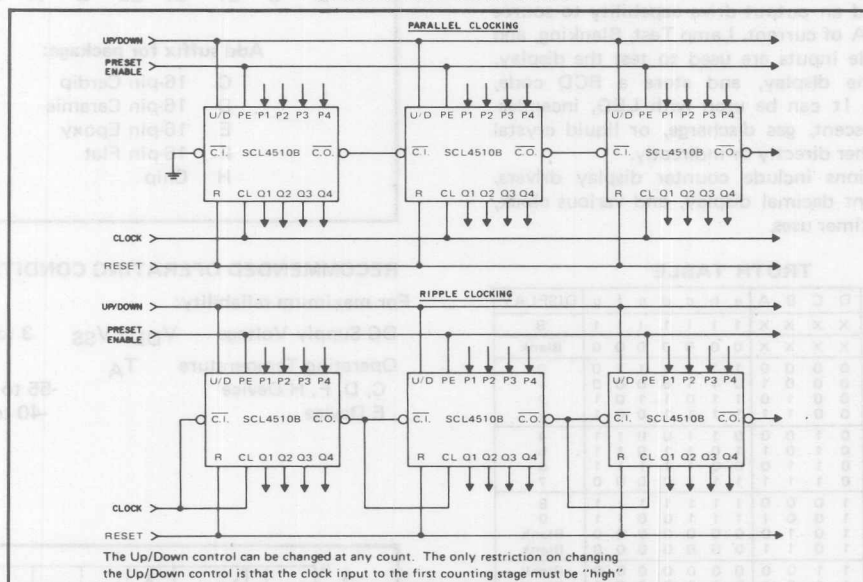
Typical P-Channel
Source Current Characteristics



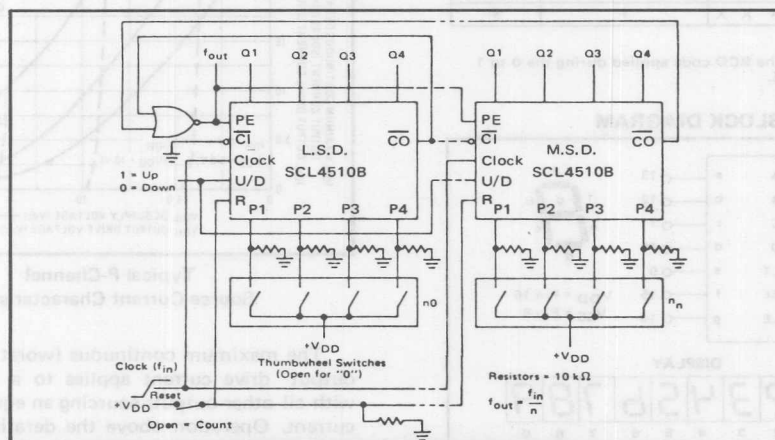
Typical N-Channel
Sink Current Characteristics

APPLICATIONS INFORMATION

CASCADING COUNTERS



Cascading Counter Packages.



Programmable Cascaded Frequency Divider

SCL4511B



CMOS BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER

FEATURES

- ◆ High-Current Sourcing Bipolar Outputs (Up to 25 mA)
- ◆ Latched Storage of Input Code
- ◆ Blanking Input for Display Intensity Modulation
- ◆ Lamp Test Provision
- ◆ Readout Blanking for Illegal Input Combinations

DESCRIPTION

The SCL4511B provides the functions of a 4-bit storage latch, an 8421 BCD-to-seven segment decoder, and an output drive capability to source up to 25 mA of current. Lamp Test, Blanking, and Latch Enable inputs are used to test the display, turn off the display, and store a BCD code, respectively. It can be used with LED, incandescent, fluorescent, gas discharge, or liquid crystal readouts either directly or indirectly.

Applications include counter display drivers, seven-segment decimal display, and various clock, watch, and timer uses.

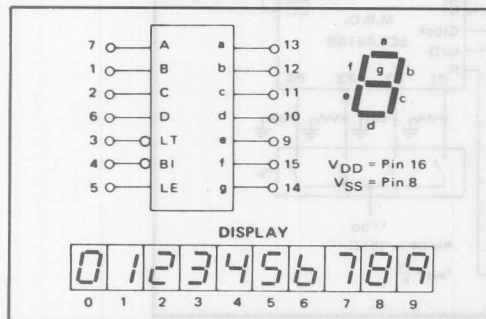
TRUTH TABLE

LE	BI	LT	D	C	B	A	a	b	c	d	e	f	g	DISPLAY
X	X	0	X	X	X	X	1	1	1	1	1	1	1	8
X	0	1	X	X	X	X	0	0	0	0	0	0	0	Blank
0	1	1	0	0	0	0	1	1	1	1	1	1	0	0
0	1	1	0	0	0	1	0	1	1	0	0	0	0	1
0	1	1	0	0	1	0	1	1	0	1	1	0	1	2
0	1	1	0	0	1	1	1	1	1	0	0	1	1	3
0	1	1	0	1	0	0	0	1	1	0	0	1	1	4
0	1	1	0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	1	0	0	0	1	1	1	1	1	6
0	1	1	0	1	1	1	1	1	0	0	0	0	0	7
0	1	1	1	0	0	0	0	1	1	1	1	1	1	8
0	1	1	1	0	0	1	1	1	1	0	0	1	1	9
0	1	1	1	0	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	0	1	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	0	0	0	0	0	0	0	0	Blank
1	1	1	X	X	X	X	*	*	*	*	*	*	*	*

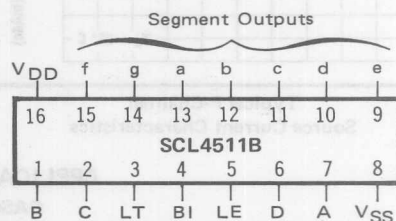
X = Don't care

* Depends upon the BCD code applied during the 0 to 1 transition of LE.

BLOCK DIAGRAM



CONNECTION DIAGRAM (all packages)



Add suffix for package:

- C 16-pin Cerdip
- D 16-pin Ceramic
- E 16-pin Epoxy
- F 16-pin Flat
- H Chip

RECOMMENDED OPERATING CONDITIONS

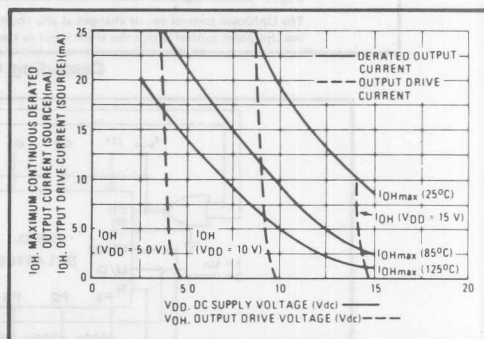
For maximum reliability:

DC Supply Voltage $V_{DD} - V_{SS}$ 3 to 15 Vdc

Operating Temperature T_A

C, D, F, H Device -55 to +125 °C

E Device -40 to +85 °C



Typical P-Channel
Source Current Characteristics

The maximum continuous (worst case) derated output drive current applies to a single output with all other outputs sourcing an equal amount of current. Operation above the derating curve at a given temperature is not recommended.

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS¹

PARAMETER	V _{DD} (V _{dc})	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ³		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT I _{DD}	5	V _{IN} = V _{SS} or V _{DD}	—	5	—	0.05	5	—	150	μAdc
	10	All valid input combinations	—	10	—	0.1	10	—	300	
	15		—	20	—	0.2	20	—	600	
OUTPUT DRIVE VOLTAGE V _{OUT}	5	I _{OH} = 0 mAdc	4.99	—	4.99	5.0	—	4.95	—	Vdc
		- 5	—	—	—	4.25	—	—	—	
		- 10	—	—	3.9	4.13	—	—	—	
		- 15	—	—	—	3.95	—	—	—	
		- 20	—	—	3.4	3.75	—	—	—	
		- 25	—	—	—	3.5	—	—	—	
	10	I _{OH} = 0 mAdc	9.99	—	9.99	10	—	9.95	—	Vdc
		- 5	—	—	—	9.25	—	—	—	
		- 10	—	—	9.0	9.15	—	—	—	
		- 15	—	—	—	9.03	—	—	—	
		- 20	—	—	8.6	8.90	—	—	—	
		- 25	—	—	—	8.75	—	—	—	
	15	I _{OH} = 0 mAdc	14.99	—	14.99	15	—	14.95	—	Vdc
		- 5	—	—	—	14.25	—	—	—	
		- 10	—	—	14.0	14.18	—	—	—	
		- 15	—	—	—	14.08	—	—	—	
		- 20	—	—	13.6	13.95	—	—	—	
		- 25	—	—	—	13.80	—	—	—	
OUTPUT LOW (SINK) CURRENT C, D, F, H device	5	V _{OL} = 0.4V	1.9	—	1.5	3.4	—	1.1	—	mAdc
		V _{OL} = 0.5V	5.0	—	4.0	6.5	—	2.8	—	
		V _{OL} = 1.5V V _{IN} = V _{SS} or V _{DD}	13.8	—	11.0	24	—	7.7	—	
	10	V _{OL} = 0.4V	1.8	—	1.5	3.4	—	1.2	—	mAdc
		V _{OL} = 0.5V	4.8	—	4.0	6.5	—	3.2	—	
		V _{OL} = 1.5V V _{IN} = V _{SS} or V _{DD}	13.2	—	11.0	24	—	8.8	—	
E device	5	V _{OL} = 0.4V	1.8	—	1.5	3.4	—	1.2	—	mAdc
	10	V _{OL} = 0.5V	4.8	—	4.0	6.5	—	3.2	—	
	15	V _{OL} = 1.5V V _{IN} = V _{SS} or V _{DD}	13.2	—	11.0	24	—	8.8	—	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".² T_{LOW} = -55°C for C, D, F, H device.

= -40°C for E device.

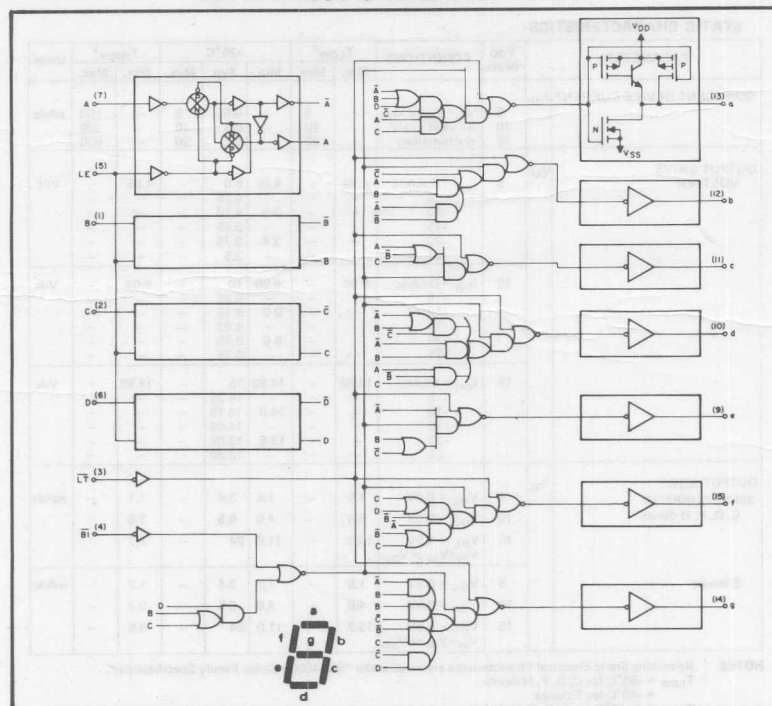
T_{HIGH} = +125°C for C, D, F, H device.

= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

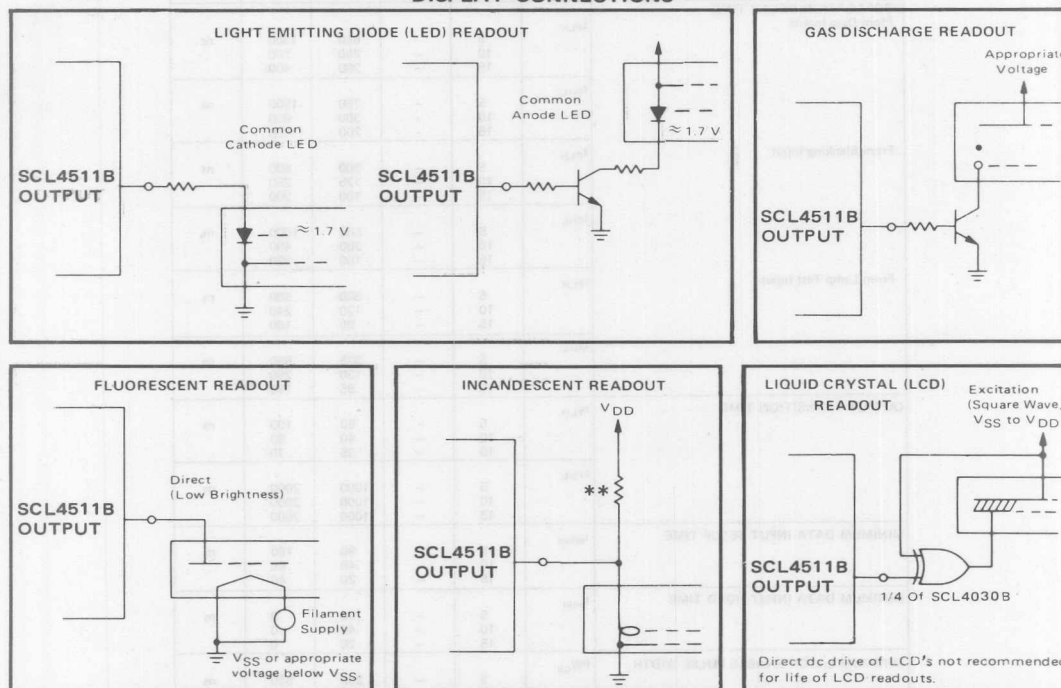
PARAMETER		V _{DD} (V _{dc})	Min.	Typ.	Max.	Units	
PROPAGATION DELAY TIME From Data Inputs	t _{PLH}	5	—	650	1300	ns	
		10	—	250	500		
		15	—	200	400		
	t _{PHL}	5	—	750	1500	ns	
		10	—	300	600		
		15	—	200	400		
	From Blanking Input	t _{PLH}	5	—	300	600	ns
			10	—	125	250	
			15	—	100	200	
	From Lamp Test Input	t _{PHL}	5	—	500	1000	ns
			10	—	200	400	
			15	—	160	320	
t _{PLH}		5	—	300	600	ns	
		10	—	120	240		
		15	—	90	180		
	t _{PHL}	5	—	325	650	ns	
		10	—	130	260		
		15	—	95	190		
OUTPUT TRANSITION TIME	t _{TLH}	5	—	50	100	ns	
		10	—	40	80		
		15	—	35	70		
	t _{THL}	5	—	1000	2000	ns	
		10	—	1000	2000		
		15	—	1000	2000		
MINIMUM DATA INPUT SETUP TIME	t _{setup}	5	—	90	180	ns	
		10	—	40	80		
		15	—	20	40		
MINIMUM DATA INPUT HOLD TIME	t _{hold}	5	—	-90	0	ns	
		10	—	-40	0		
		15	—	-20	0		
MINIMUM LATCH ENABLE PULSE WIDTH	PW _{LE}	5	—	260	520	ns	
		10	—	110	220		
		15	—	65	130		

LOGIC DIAGRAM



APPLICATIONS INFORMATION

DISPLAY CONNECTIONS



**A filament pre-warm resistor is recommended to reduce filament thermal shock and increase the effective cold resistance of the filament.



FEATURES

- ◆ 3-State Output with Disable Control
- ◆ Separate Inhibit Input
- ◆ Selects One of Eight Data Sources
- ◆ Performs Parallel-To-Serial Conversion

DESCRIPTION

The SCL4512B is an 8-Channel Data Selector with Function Inhibit and Output Disable controls. One of eight binary inputs is selected by Select inputs A, B, and C, and is routed to the output Z. A high on the Disable input causes the Z output to assume a high-impedance state, regardless of other input conditions. This allows the output to interface directly with bus-oriented systems. When the Inhibit input is high, it forces the output low, providing the Disable input is low. By manipulation of the inputs, the SCL4512B can provide any logic functions of four variables (see Applications Information).

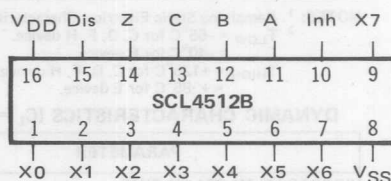
TRUTH TABLE

C	B	A	INHIBIT	DISABLE	Z
0	0	0	0	0	X0
0	0	1	0	0	X1
0	1	0	0	0	X2
0	1	1	0	0	X3
1	0	0	0	0	X4
1	0	1	0	0	X5
1	1	0	0	0	X6
1	1	1	0	0	X7
φ	φ	φ	1	0	0
φ	φ	φ	φ	1	High Impedance

φ = Don't Care

CONNECTION DIAGRAM

(all packages)



Add suffix for package:

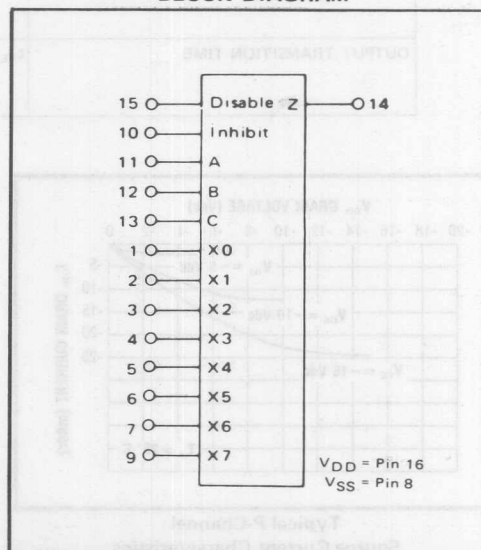
- C 16-pin Cerdip
- D 16-pin Ceramic
- E 16-pin Epoxy
- F 16-pin Flat
- H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A	-55 to +125	°C
C, D, F, H Device		-40 to +85	°C
E Device			

BLOCK DIAGRAM



		10 15	All valid input combinations	— —	10 20	— —	0.1 0.2	10 20	— —	300 600	μAdc
3-STATE OUTPUT LEAKAGE CURRENT	I_{ZL}	15		— ± 0.1	— $\pm 10^{-4}$	— ± 0.1	— ± 1.0	— ± 1.0	— ± 1.0	μAdc	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

² $T_{\text{LOW}} = -55^{\circ}\text{C}$ for C, D, F, H device.

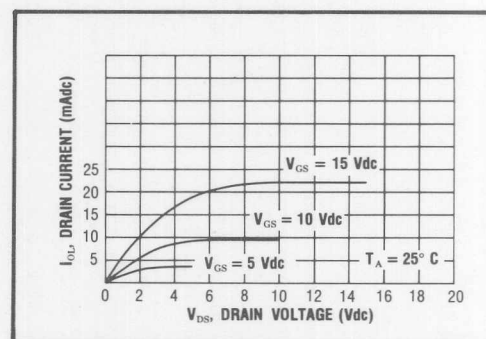
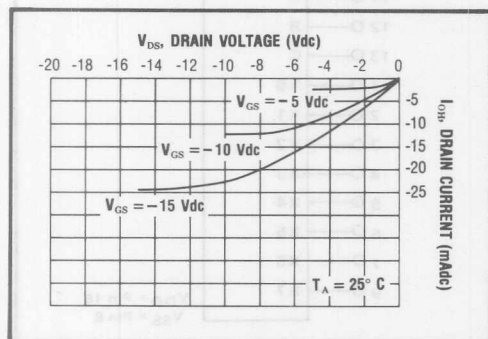
$= -40^{\circ}\text{C}$ for E device.

$T_{\text{HIGH}} = +125^{\circ}\text{C}$ for C, D, F, H device.

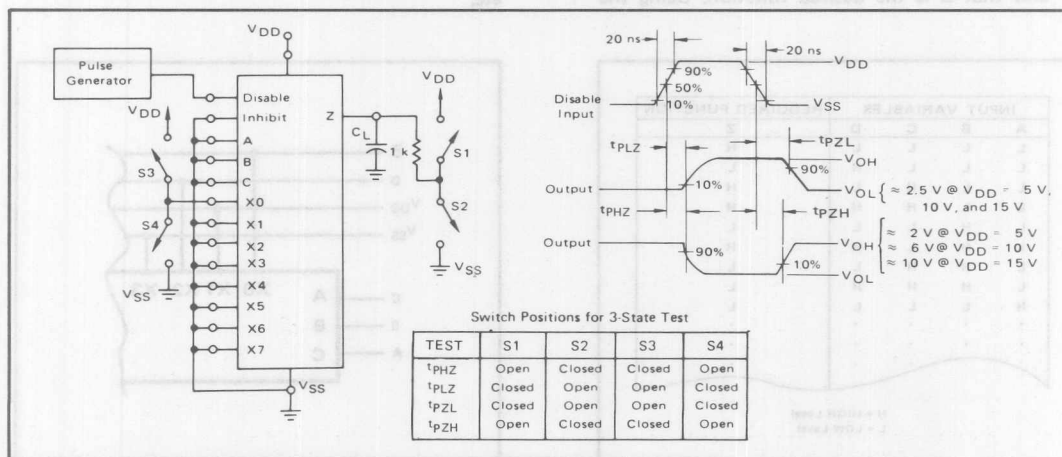
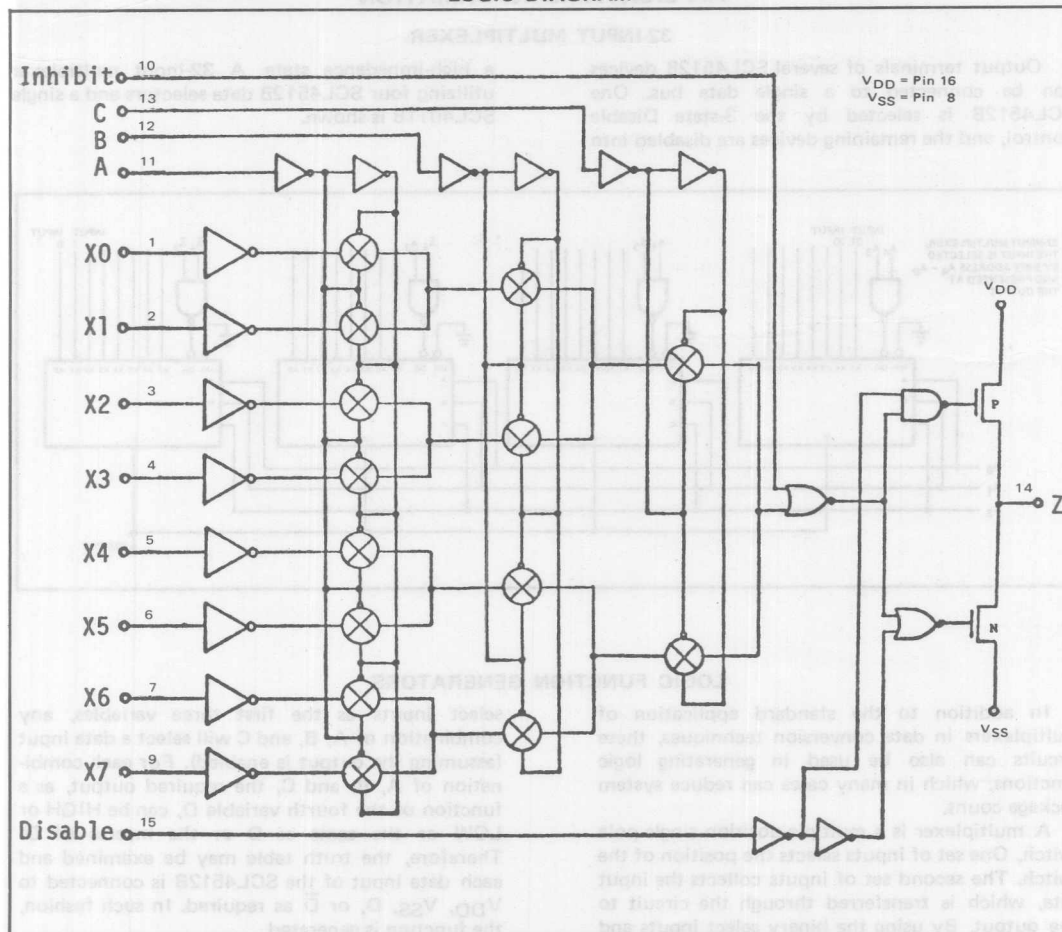
$= +85^{\circ}\text{C}$ for E device.

DYNAMIC CHARACTERISTICS ($C_L = 50\text{pF}$, $T_A = 25^{\circ}\text{C}$)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME From Inhibit	t_{PLH}	5	—	140	280	ns
		10	—	50	100	
		15	—	40	80	
	t_{PHL}	5	—	155	310	ns
		10	—	60	120	
		15	—	45	90	
From Select Input	t_{PLH}	5	—	225	450	ns
		10	—	85	170	
		15	—	65	130	
	t_{PHL}	5	—	300	600	ns
		10	—	105	210	
		15	—	80	160	
From Data Input	t_{PLH}	5	—	215	430	ns
		10	—	85	170	
		15	—	65	130	
	t_{PHL}	5	—	290	580	ns
		10	—	105	210	
		15	—	80	160	
From Disable	t_{PHZ}, t_{PZH} t_{PLZ}, t_{PLZ}	5	—	75	150	ns
		10	—	45	90	
		15	—	35	70	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	—	130	260	ns
		10	—	65	130	
		15	—	50	100	



LOGIC DIAGRAM



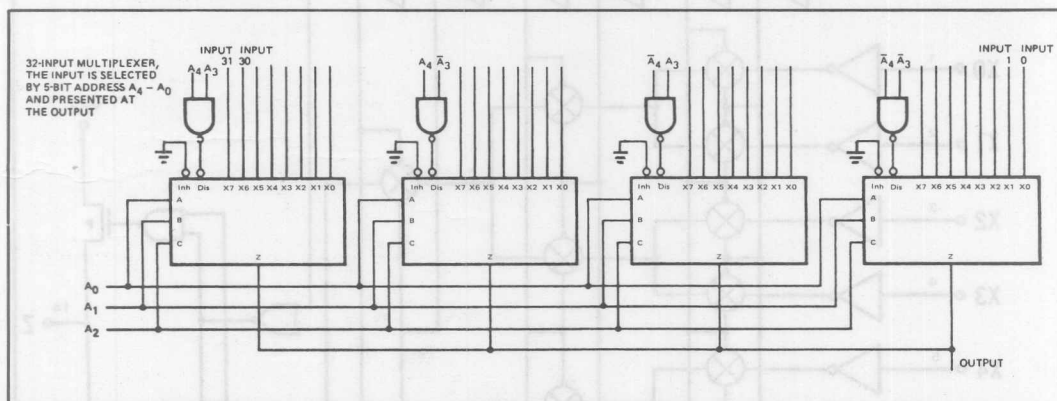
3-State AC Test Circuit and Waveform

APPLICATIONS INFORMATION

32-INPUT MULTIPLEXER

Output terminals of several SCL4512B devices can be connected to a single data bus. One SCL4512B is selected by the 3-state Disable control, and the remaining devices are disabled into

a high-impedance state. A 32-input multiplexer utilizing four SCL4512B data selectors and a single SCL4011B is shown.



LOGIC FUNCTION GENERATORS

In addition to the standard application of multiplexers in data conversion techniques, these circuits can also be used in generating logic functions, which in many cases can reduce system package count.

A multiplexer is a multiple-position single-pole switch. One set of inputs selects the position of the switch. The second set of inputs collects the input data, which is transferred through the circuit to one output. By using the binary select inputs and the data inputs, the SCL4512B can generate any of the 65,536 different functions of four variables.

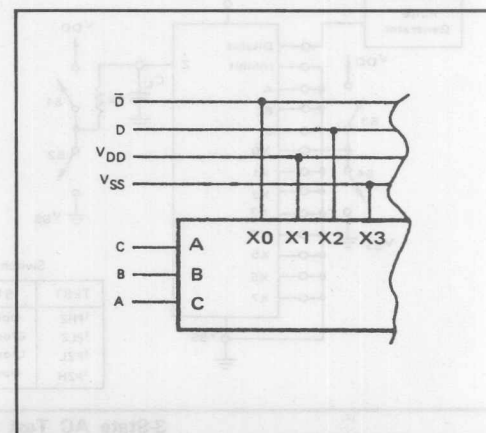
Assume the four binary inputs are A, B, C, and D, and that Z is the desired function. Using the

select inputs as the first three variables, any combination of A, B, and C will select a data input (assuming the output is enabled). For each combination of A, B, and C, the required output, as a function of the fourth variable D, can be HIGH or LOW or the same as D or the inverse of D. Therefore, the truth table may be examined and each data input of the SCL4512B is connected to V_{DD} , V_{SS} , D, or $\bar{D}$ as required. In such fashion, the function is generated.

In the example shown, the first two outputs are the inverse of D, so X0 is connected to $\bar{D}$. The next two are HIGH, so X1 is connected to V_{DD} , etc.

INPUT VARIABLES				REQUIRED FUNCTION
A	B	C	D	Z
L	L	L	L	H
L	L	L	H	L
L	L	H	L	H
L	L	H	H	H
L	H	L	L	L
L	H	L	H	H
L	H	H	L	L
L	H	H	H	L
H	L	L	L	L
.	.	.	.	.
.	.	.	.	.

H = HIGH Level
L = LOW Level



SCL4514B SCL4515B



CMOS 4-TO-16 LINE DECODERS WITH LATCH

FEATURES

- ◆ Strobed Input Latch
- ◆ Inhibit Control
- ◆ Selected Output Active High (SCL4514B) or Active Low (SCL4515B)

DESCRIPTION

The SCL4514B and SCL4515B are two output options of a 4-to-16 Line Decoder with Latched Inputs. The SCL4514B presents a logic "1" at the selected output, and the SCL4515B presents a logic "0" at the selected output. The latches hold the last input data presented prior to the Strobe transition from "1" to "0". Inhibit allows all outputs to be placed at "0" (SCL4514B), or "1" (SCL4515B), regardless of the state of the Data or Strobe inputs.

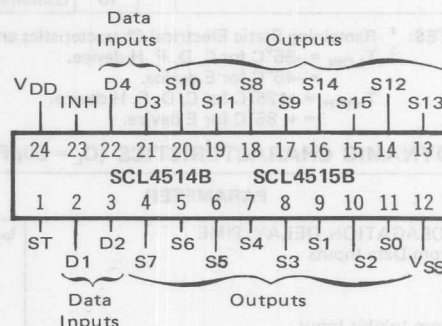
Applications include code conversion, address decoding, memory selection control, demultiplexing, and readout decoding.

TRUTH TABLE (Strobe = 1)

Inhibit	Data Inputs				Selected Output SCL4514B = Logic "1" SCL4515B = Logic "0"
	D	C	B	A	
0	0	0	0	0	S0
0	0	0	0	1	S1
0	0	0	1	0	S2
0	0	0	1	1	S3
0	0	1	0	0	S4
0	0	1	0	1	S5
0	0	1	1	0	S6
0	0	1	1	1	S7
0	1	0	0	0	S8
0	1	0	0	1	S9
0	1	0	1	0	S10
0	1	0	1	1	S11
0	1	1	0	0	S12
0	1	1	0	1	S13
0	1	1	1	0	S14
0	1	1	1	1	S15
1	X	X	X	X	All Outputs = "0", SCL4514B All Outputs = "1", SCL4515B

X = Don't Care

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

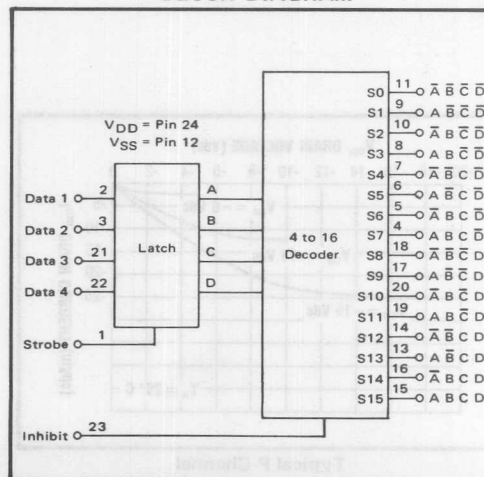
- D 24-pin Ceramic
- E 24-pin Epoxy
- H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	V_{dc}
Operating Temperature	T_A	-55 to +125	$^{\circ}C$
D, H Device		-40 to +85	$^{\circ}C$
E Device			

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS¹

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT <i>I</i> _{DD}	5	V _{IN} = V _{SS} or V _{DD}	—	5	—	0.05	5	—	150	μAdc
	10	All valid input combinations	—	10	—	0.1	10	—	300	
	15		—	20	—	0.2	20	—	600	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

² T_{LOW} = -55°C for C, D, F, H device.

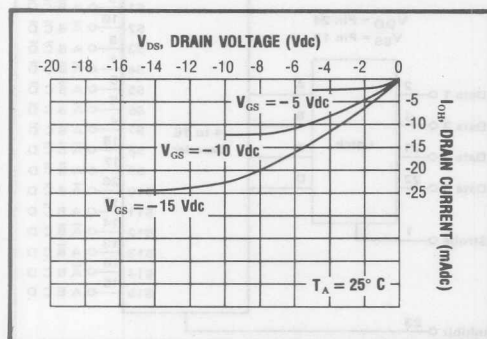
= -40°C for E device.

T_{HIGH} = +125°C for C, D, F, H device.

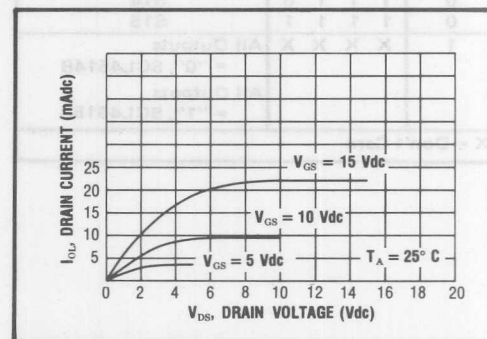
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V _{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME From Data Inputs	t _{PLH} , t _{PHL}	5	—	550	1100	ns
		10	—	225	450	
		15	—	150	300	
		5	—	400	800	ns
		10	—	150	300	
		15	—	100	200	
OUTPUT TRANSITION TIME	t _{TLH} , t _{THL}	5	—	130	260	ns
		10	—	65	130	
		15	—	50	100	
MINIMUM DATA INPUT SETUP TIME	t _{setup}	5	—	125	250	ns
		10	—	50	100	
		15	—	40	80	
MINIMUM STROBE PULSE WIDTH	PW _{ST}	5	—	175	350	ns
		10	—	50	100	
		15	—	40	80	



Typical P-Channel
Source Current Characteristics



Typical N-Channel
Sink Current Characteristics



FEATURES

- ◆ Internally Synchronous for High Speed
- ◆ Asynchronous Preset Enable
- ◆ Asynchronous Reset
- ◆ Logic Edge-Clocked Design
- ◆ 6MHz Counting Rate @ 10Vdc
- ◆ Carry Output for Cascading Stages

DESCRIPTION

The SCL4516B consists of a four-stage Up/Down Counter with provisions for "look-ahead" carry in both counting modes. The inputs consist of a single Clock, Carry-in (Clock Enable), Reset, Up/Down, Preset Enable, and four individual Jam signals. Four separate buffered Q signals and a Carry-out signal are provided as outputs.

A high Preset Enable signal allows information on the Jam inputs to preset the counter to any state asynchronously with the Clock. A high on the Reset line resets all stages to the "zero" state. The counter is advanced one count at the positive transition of the Clock when the Carry-in and Preset Enable signals are low. Advancement is inhibited when the Carry-in or Preset Enable signals are high. The Carry-out signal is normally high and goes low when the counter reaches its maximum count in the Up mode or the minimum count in the Down mode, provided the Carry-in signal is low. The Carry-in signal in the low state can thus be considered a "Clock Enable." The Carry-in terminal must be connected to V_{SS} when not in use.

The counter counts Up when the Up/Down input is high, and Down when the Up/Down input is low. Multiple packages can be connected in either a parallel-clocking or a ripple-clocking arrangement. Parallel clocking provides synchronous control and hence faster response from all counting outputs. Ripple-clocking allows for longer clock input rise and fall times.

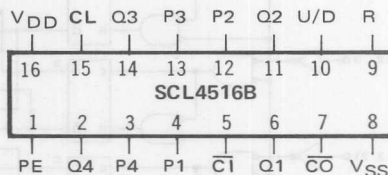
This counter finds primary use in up/down and differential counting and frequency synthesizer applications. It is also useful in A/D and D/A conversion and for magnitude and sign generation.

TRUTH TABLE

CARRY IN	UP/DOWN	PRESET ENABLE	RESET	ACTION
1	X	0	0	No Count
0	1	0	0	Count Up
0	0	0	0	Count Down
X	X	1	0	Preset
X	X	X	1	Reset

X = Don't Care

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

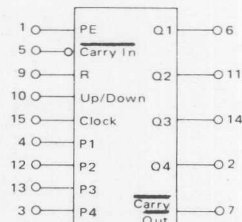
- C 16-pin Cerdip
- D 16-pin Ceramic
- E 16-pin Epoxy
- F 16-pin Flat
- H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

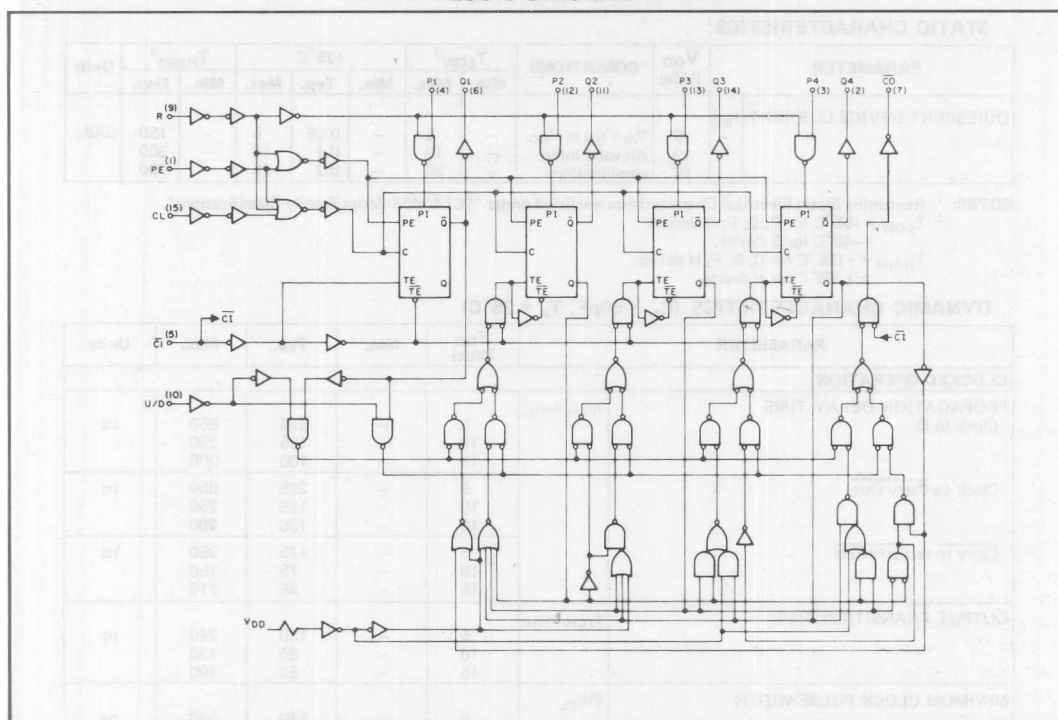
DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

BLOCK DIAGRAM

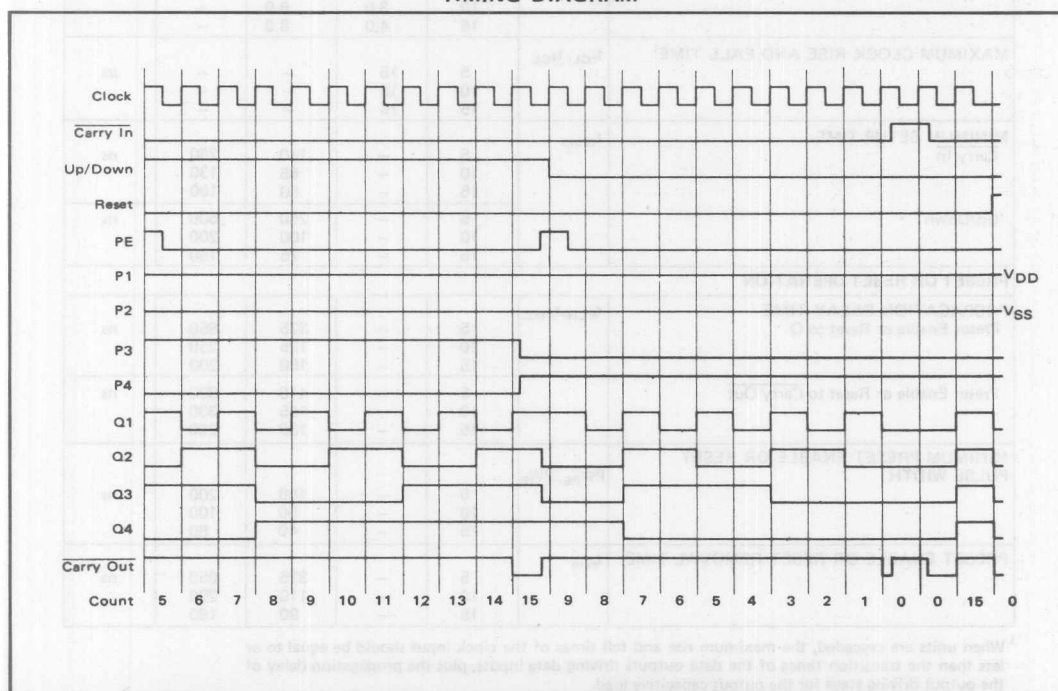


V_{DD} = Pin 16
 V_{SS} = Pin 8

LOGIC DIAGRAM



TIMING DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS¹

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT I _{DD}	5	V _{IN} = V _{SS} or V _{DD}	—	5	—	0.05	5	—	150	μA _{dc}
	10	All valid input	—	10	—	0.1	10	—	300	
	15	combinations	—	20	—	0.2	20	—	600	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

² T_{LOW} = -55°C for C, D, F, H device.

= -40°C for E device.

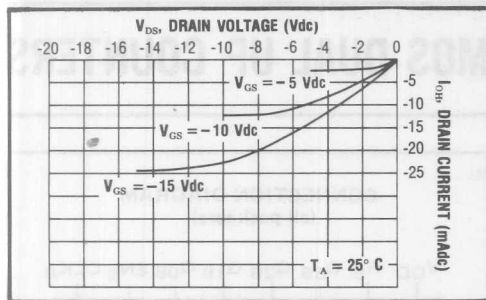
T_{HIGH} = +125°C for C, D, F, H device.

= + 85°C for E device.

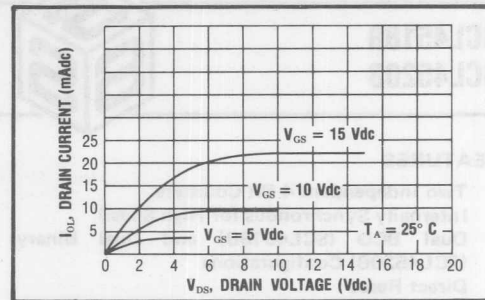
DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V _{DD} (Vdc)	Min.	Typ.	Max.	Units
CLOCKED OPERATION						
PROPAGATION DELAY TIME Clock to Q	t _{PLH} , t _{PHL}	5 10 15	— — —	325 125 100	650 250 200	ns
Clock to Carry Out		5 10 15	— — —	325 125 100	650 250 200	ns
Carry In to Carry Out		5 10 15	— — —	175 75 55	350 150 110	ns
OUTPUT TRANSITION TIME	t _{TLH} , t _{THL}	5 10 15	— — —	130 65 50	260 130 100	ns
MINIMUM CLOCK PULSE WIDTH	PW _{CL}	5 10 15	— — —	170 85 70	340 170 140	ns
MAXIMUM CLOCK FREQUENCY	f _{CL}	5 10 15	— 1.5 3.0 4.0	3.0 6.0 8.0	— — —	MHz
MAXIMUM CLOCK RISE AND FALL TIME ¹	t _{rCL} , t _{fCL}	5 10 15	15 15 15	— — —	— — —	μs
MINIMUM SETUP TIME Carry In	t _{setup}	5 10 15	— — —	130 65 50	260 130 100	ns
Up/Down		5 10 15	— — —	250 100 75	500 200 150	ns
PRESET OR RESET OPERATION						
PROPAGATION DELAY TIME Preset Enable or Reset to Q	t _{PLH} , t _{PHL}	5 10 15	— — —	325 125 100	650 250 200	ns
Preset Enable or Reset to Carry Out		5 10 15	— — —	410 165 130	820 330 260	ns
MINIMUM PRESET ENABLE OR RESET PULSE WIDTH	PW _{PE} , PW _R	5 10 15	— — —	100 50 40	200 100 80	ns
PRESET ENABLE OR RESET REMOVAL TIME	t _{rem}	5 10 15	— — —	325 110 90	650 220 180	ns

¹ When units are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the transition times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitive load.



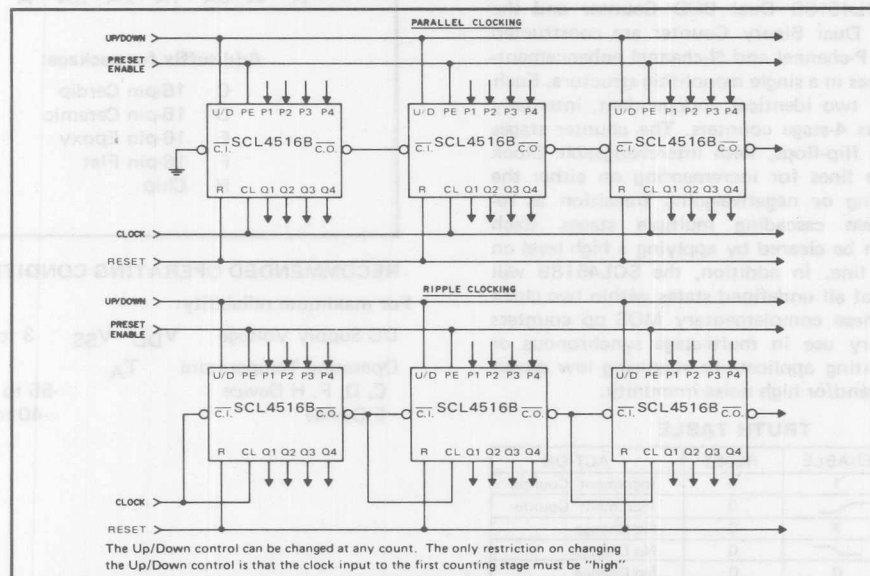
Typical P-Channel
Source Current Characteristics



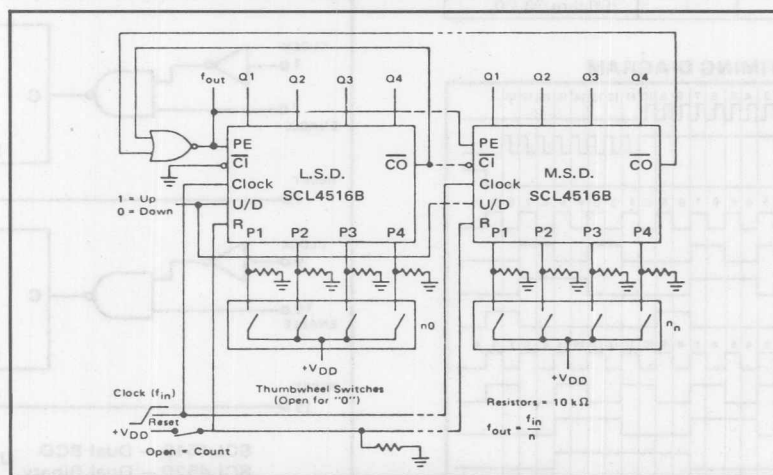
Typical N-Channel
Sink Current Characteristics

APPLICATIONS INFORMATION

CASCADING COUNTERS



Cascading counter packages.



Programmable Cascaded Frequency Divider

SCL4518B SCL4520B



CMOS DUAL UP COUNTERS

FEATURES

- ◆ Two Independent 4-Bit Counters
- ◆ Internally Synchronous for High Speed
- ◆ Dual BCD (SCL4518B) and Dual Binary (SCL4520B) Configurations
- ◆ Direct Reset
- ◆ Logic Edge-Clocked Design
- ◆ Trigger from either Edge of Clock Signal
- ◆ Static Operation— DC to 5MHz @ 10Vdc

DESCRIPTION

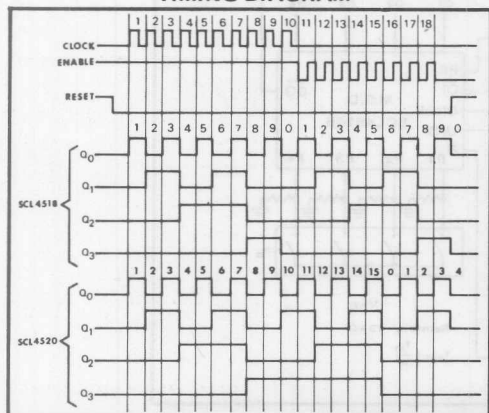
The SCL4518B Dual BCD Counter and the SCL4520B Dual Binary Counter are constructed with MOS P-channel and N-channel enhancement-mode devices in a single monolithic structure. Each consists of two identical, independent, internally synchronous 4-stage counters. The counter stages are type-D flip-flops, with interchangeable Clock and Enable lines for incrementing on either the positive-going or negative-going transition as required when cascading multiple stages. Each counter can be cleared by applying a high level on the Reset line. In addition, the SCL4518B will count out of all undefined states within two clock periods. These complementary MOS up counters find primary use in multi-stage synchronous or ripple counting applications requiring low power dissipation and/or high noise immunity.

TRUTH TABLE

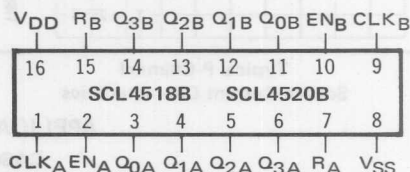
CLOCK	ENABLE	RESET	ACTION
	1	0	Increment Counter
0		0	Increment Counter
	X	0	No Change
X		0	No Change
	0	0	No Change
1		0	No Change
X	X	1	Q0 thru Q3 = 0

X = Don't Care

TIMING DIAGRAM



CONNECTION DIAGRAM (all packages)



Add suffix for package:

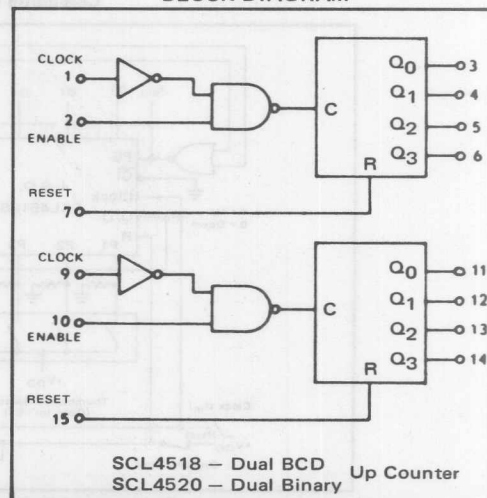
- C 16-pin Cerdip
- D 16-pin Ceramic
- E 16-pin Epoxy
- F 16-pin Flat
- H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A	-55 to +125	°C
C, D, F, H Device		-40 to +85	°C
E Device			

BLOCK DIAGRAM



SCL4518 — Dual BCD Up Counter
SCL4520 — Dual Binary Up Counter

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS¹

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	V _{IN} = V _{SS} or V _{DD} All valid input combinations	—	5	—	0.05	5	—	150	μAdc
			—	10	—	0.1	10	—	300	
			—	20	—	0.2	20	—	600	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

² T_{LOW} = -55°C for C, D, F, H device.

= -40°C for E device.

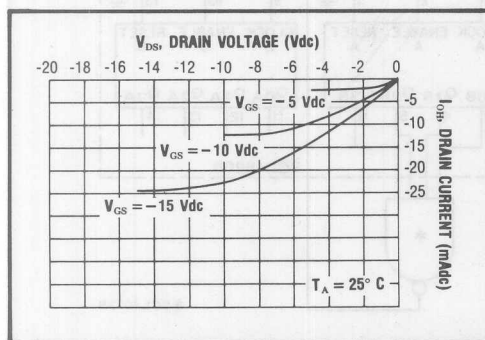
T_{HIGH} = +125°C for C, D, F, H device.

= + 85°C for E device.

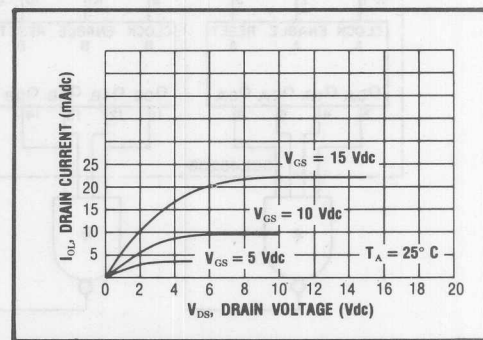
DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V _{DD} (V _{dc})	Min.	Typ.	Max.	Units
CLOCKED OPERATION						
PROPAGATION DELAY TIME From Clock or Clock Enable	t _{PLH} , t _{PHL}	5	—	225	450	ns
		10	—	100	200	
		15	—	80	160	
OUTPUT TRANSITION TIME	t _{TLH} , t _{THL}	5	—	130	260	ns
		10	—	65	130	
		15	—	50	100	
MINIMUM CLOCK PULSE WIDTH	PW _{CL}	5	—	120	240	ns
		10	—	50	100	
		15	—	40	80	
MINIMUM CLOCK ENABLE PULSE WIDTH	PW _{CE}	5	—	200	400	ns
		10	—	90	180	
		15	—	75	150	
MAXIMUM CLOCK FREQUENCY	f _{CL}	5	1.0	2.0	—	MHz
		10	2.5	5.0	—	
		15	3.0	6.0	—	
MAXIMUM CLOCK OR CLOCK ENABLE RISE & FALL TIME ¹	t _{rCL} , t _{fCL}	5	15	—	—	μs
		10	5	—	—	
		15	3	—	—	
RESET OPERATION						
PROPAGATION DELAY TIME	t _{PHL}	5	—	225	450	ns
		10	—	100	200	
		15	—	80	160	
MINIMUM RESET PULSE WIDTH	PW _R	5	—	120	240	ns
		10	—	50	100	
		15	—	40	80	
RESET REMOVAL TIME	t _{rem}	5	—	100	200	ns
		10	—	50	100	
		15	—	40	80	

¹ When units are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the transition times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitive load.

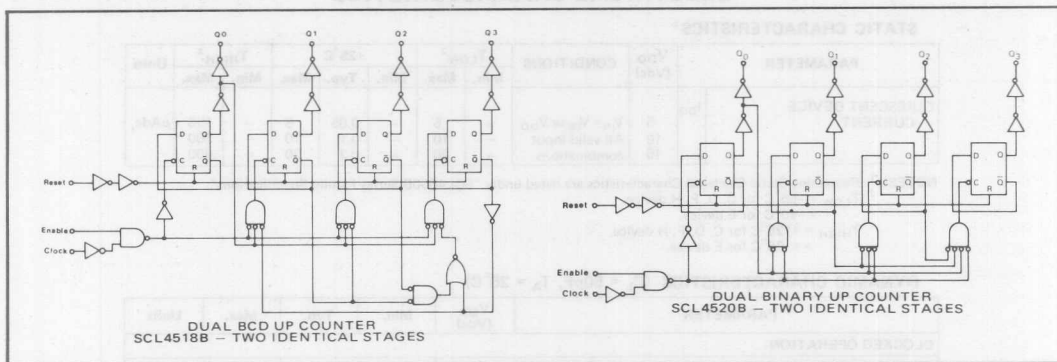


Typical P-Channel
Source Current Characteristics

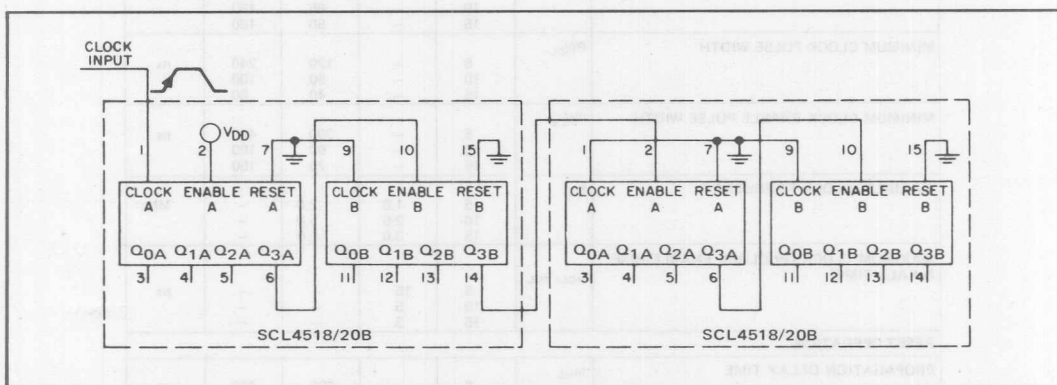


Typical N-Channel
Sink Current Characteristics

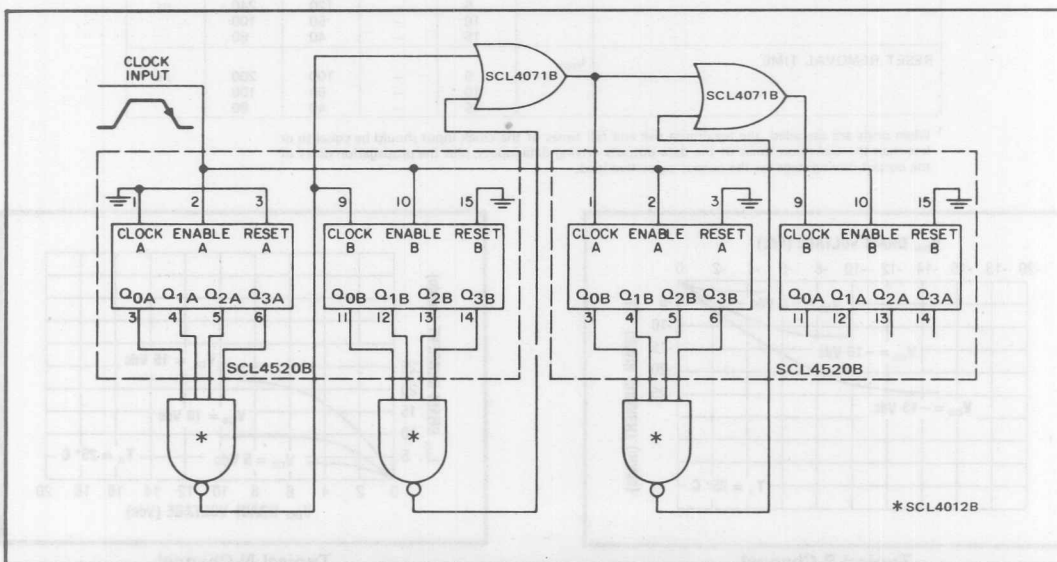
LOGIC DIAGRAMS



APPLICATIONS INFORMATION



Ripple cascading of four counters with positive-edge triggering.



Synchronous cascading of four binary counters with negative-edge triggering.

SCL4522B, SCL4526B Preliminary



CMOS PROGRAMMABLE DOWN COUNTERS

FEATURES

- Internally Synchronous for High Speed
- BCD Decade (SCL4522B) or 4-Bit Binary (SCL4526B) Down Counters
- Asynchronous Preset Enable
- Asynchronous Reset
- Cascadable
- Logic Edge-Clocked Design
- Static Operation — DC to 5MHz @ 10Vdc
- Trigger from Either Edge of Clock Input
- Balanced Output Drive Current Specifications

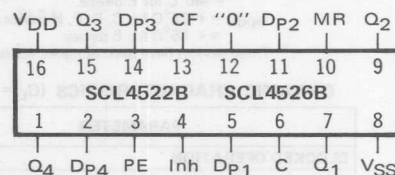
DESCRIPTION

The SCL4522B BCD Counter and the SCL4526B Binary Counter are constructed with MOS P-channel and N-channel enhancement-mode devices in a single monolithic structure.

These devices are programmable, cascadable down counters with a decoded "0" state output for divide-by-N applications. In single stage applications the "0" output is applied to the Preset Enable input. The Cascade Feedback input allows cascade divide-by-N operation with no additional gates required. The Master Reset function provides synchronous initiation of divide-by-N cycles. The Clock Inhibit input allows disabling of the pulse counting function.

These complementary MOS counters can be used in frequency synthesizers, phase-locked loops, and other frequency division applications requiring low power dissipation and/or high noise immunity.

CONNECTION DIAGRAM (all packages)



Add suffix for package:

- C 16-pin Cerdip
- D 16-pin Ceramic
- E 16-pin Epoxy
- F 16-pin Flat
- H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

TRUTH TABLES

Both Types

Clock	Inhibit	Preset Enable	Master Reset	Action
0	0	0	0	No Count
1	0	0	0	Count-1
x	1	0	0	No Count
1	x	0	0	Count-1
x	x	1	0	Preset
x	x	x	1	Reset

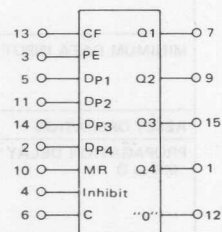
SCL4522B

Count	Output			
	Q4	Q3	Q2	Q1
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

SCL4526B

Count	Output			
	Q4	Q3	Q2	Q1
15	1	1	1	1
14	1	1	1	0
13	1	1	0	1
12	1	1	0	0
11	1	0	1	1
10	1	0	1	0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

BLOCK DIAGRAM



V_{DD} = Pin 16
 V_{SS} = Pin 8

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS^{1, 3}

PARAMETER	V _{DD} (V dc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	V _{IN} = V _{SS} or V _{DD} All valid input combinations	—	5	—	0.05	5	—	150	μAdc
			—	10	—	0.1	10	—	300	
			—	20	—	0.2	20	—	600	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

² T_{LOW} = -55°C for C, D, F, H device.

= -40°C for E device.

T_{HIGH} = +125°C for C, D, F, H device.

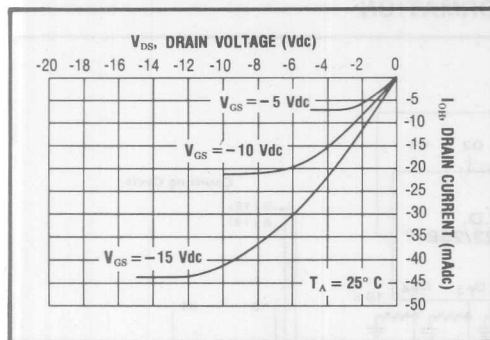
= + 85°C for E device.

³ These devices have been designed for balanced output drive current specifications. Consult Family Specifications.

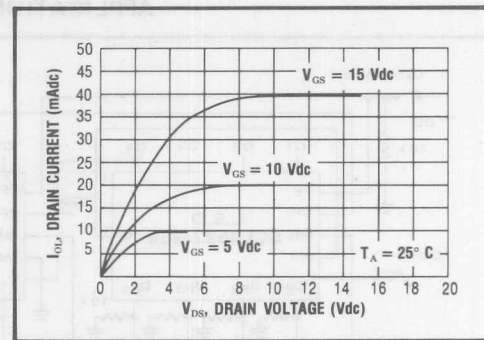
DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V _{DD} (V dc)	Min.	Typ.	Max.	Units	
CLOCKED OPERATION							
PROPAGATION DELAY TIME Clock or Inhibit to Q	t _{PLH} , t _{PHL}	5	—	415	830	ns	
		10	—	160	320		
		15	—	120	240		
	Clock or Inhibit to “O”	5	—	175	350	ns	
		10	—	125	250		
		15	—	100	200		
OUTPUT TRANSITION TIME	t _{TLH} , t _{THL}	5	—	100	200	ns	
10	—	50	100				
15	—	40	80				
MINIMUM CLOCK PULSE WIDTH	PW _{CL}	5	—	125	250	ns	
10	—	50	100				
15	—	40	80				
MAXIMUM CLOCK FREQUENCY	f _{CL}	5	1.5	2.0	—	MHz	
10	3.0	5.0	—				
15	4.0	6.6	—				
MAXIMUM CLOCK OR INHIBIT RISE AND FALL TIME ¹	t _{rCL} , t _{fCL}	5	15	—	—	μs	
10	15	—	—				
15	15	—	—				
PRESET OPERATION							
PROPAGATION DELAY TIME PE to Q	t _{PLH} , t _{PHL}	5	—	415	830	ns	
		10	—	160	320		
		15	—	120	240		
	PE to “O”	5	—	175	350	ns	
		10	—	125	250		
		15	—	100	200		
MINIMUM PRESET ENABLE PULSE WIDTH	PW _{PE}	5	—	125	250	ns	
10	—	50	100				
15	—	40	80				
MINIMUM DATA INPUT HOLD TIME	t _{hold}	5	—	75	125	ns	
10	—	25	50				
15	—	20	40				
RESET OPERATION							
PROPAGATION DELAY TIME MR to Q	t _{PHL}	5	—	415	830	ns	
		10	—	160	320		
		15	—	120	240		
	MR to “O”	t _{PLH}	5	—	175	350	ns
			10	—	125	250	
			15	—	100	200	
MINIMUM MASTER RESET PULSE WIDTH	PW _{MR}	5	—	150	300	ns	
10	—	125	250				
15	—	100	200				

¹ When units are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the transition times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitive load.

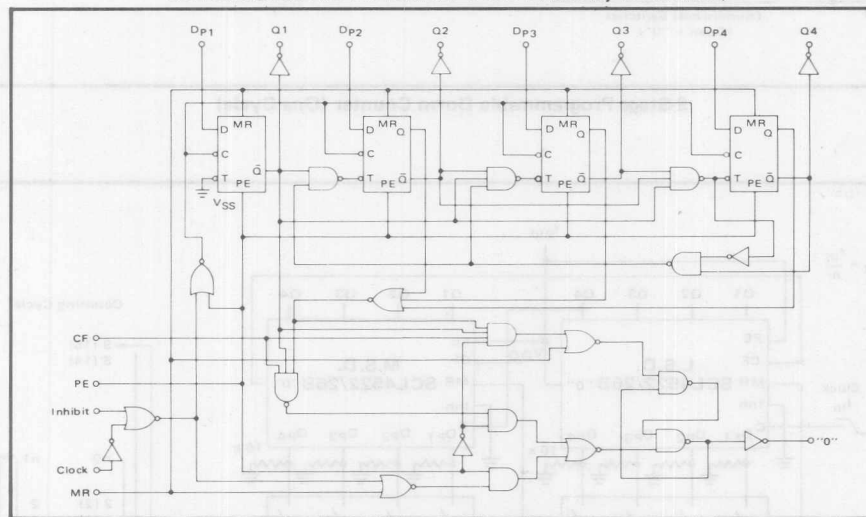


Typical P-Channel
Source Current Characteristics

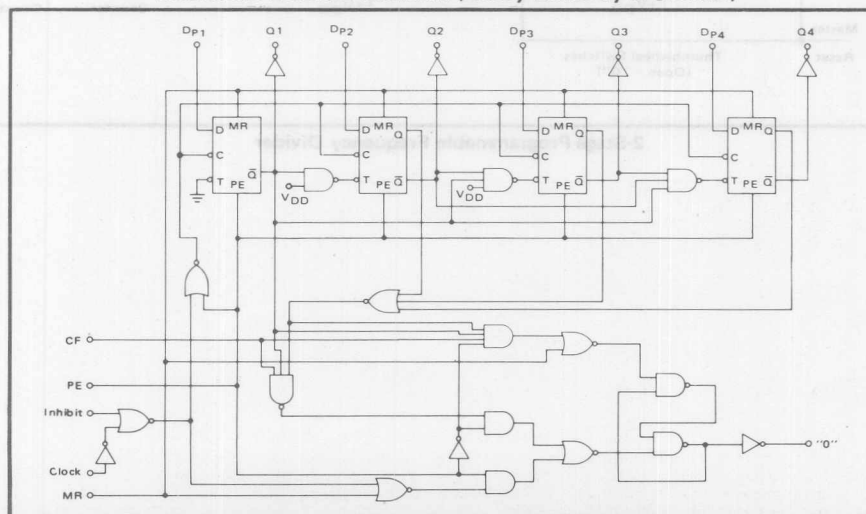


Typical N-Channel
Sink Current Characteristics

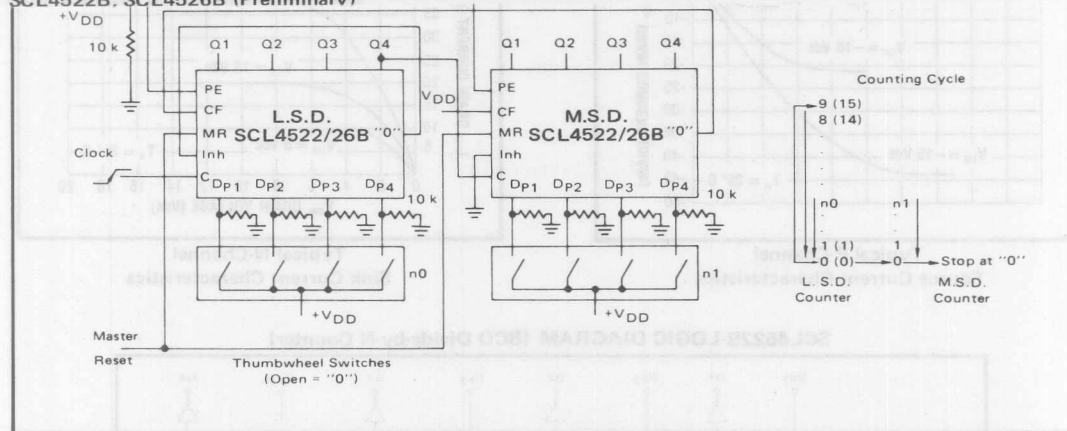
SCL4522B LOGIC DIAGRAM (BCD Divide-by-N Counter)



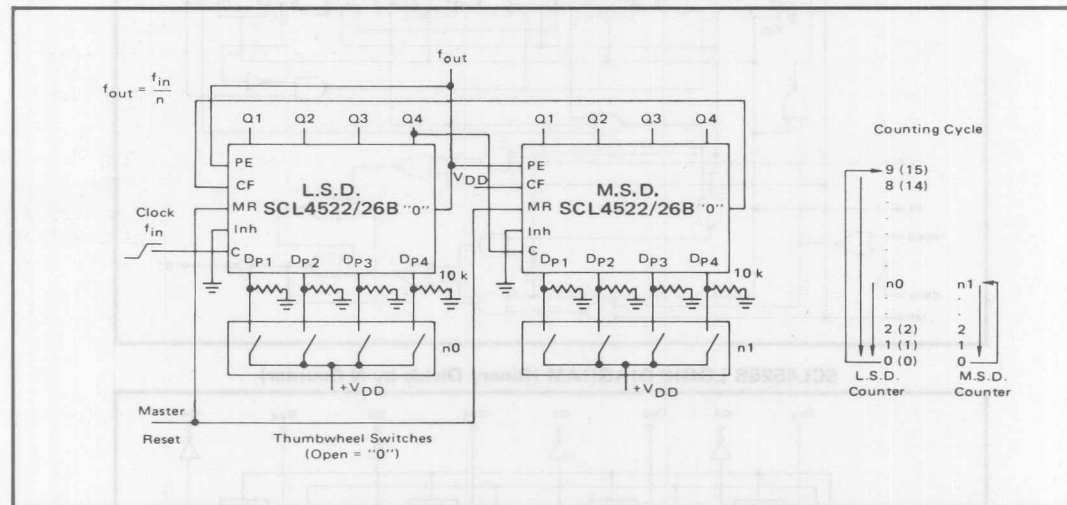
SCL4526B LOGIC DIAGRAM (Binary Divide-by-N Counter)



SCL4522B, SCL4526B (Preliminary)



2-Stage Programmable Down Counter (One Cycle)



2-Stage Programmable Frequency Divider

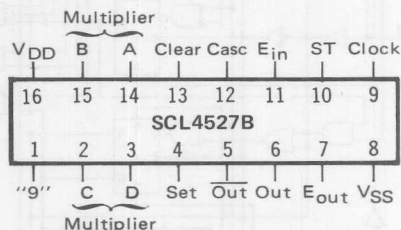


FEATURES

- ◆ Internally Synchronous for High Speed
- ◆ Strobe for Enabling or Inhibiting Outputs
- ◆ Enable and Cascade Inputs
- ◆ "9" Output Available for Cascading
- ◆ Complementary Outputs
- ◆ Clear and Set-To-Nine Inputs

DESCRIPTION

The SCL4527B is a BCD Digital Rate Multiplier (DRM) which provides an output pulse rate of the clock input pulse rate multiplied by 1/10 of the BCD input. For example, when the BCD input is 8, there will be 8 output pulses for every 10 input pulses. The output is clocked on the negative-going edge of the input clock. This device may be used to perform arithmetic operations, solve algebraic and differential equations, generate logarithms and trigonometric functions, A/D and D/A conversion, and frequency division.

CONNECTION DIAGRAM
(all packages)

Add suffix for package:

- C 16-pin Cerdip
- D 16-pin Ceramic
- E 16-pin Epoxy
- F 16-pin Flat
- H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

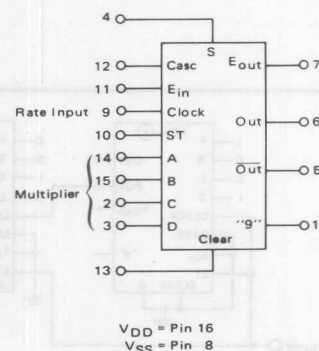
DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A	-55 to +125	°C
C, D, F, H Device		-40 to +85	°C
E Device			

TRUTH TABLE

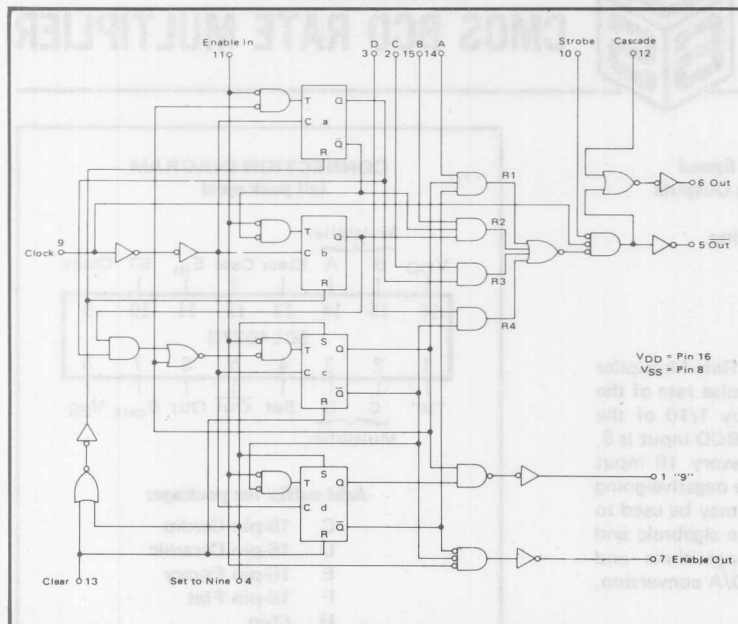
Inputs										Number of Pulses or Output Logic Level (H or L)			
D	C	B	A	No. of Clock Pulses	E_{IN}	Strobe	Cascade	Clear	Set	Pin 6 OUT	Pin 5 OUT	Pin 7 EOUT	Pin 1 "9"
0	0	0	0	10	0	0	0	0	0	0	H	1	1
0	0	0	1	10	0	0	0	0	0	1	1	1	1
0	0	1	0	10	0	0	0	0	0	2	2	1	1
0	0	1	1	10	0	0	0	0	0	3	3	1	1
0	1	0	0	10	0	0	0	0	0	4	4	1	1
0	1	0	1	10	0	0	0	0	0	5	5	1	1
0	1	1	0	10	0	0	0	0	0	6	6	1	1
0	1	1	1	10	0	0	0	0	0	7	7	1	1
1	0	0	0	10	0	0	0	0	0	8	8	1	1
1	0	0	1	10	0	0	0	0	0	9	9	1	1
1	0	1	0	10	0	0	0	0	0	8	8	1	1
1	0	1	1	10	0	0	0	0	0	9	9	1	1
1	1	0	0	10	0	0	0	0	0	8	8	1	1
1	1	0	1	10	0	0	0	0	0	9	9	1	1
1	1	1	0	10	0	0	0	0	0	8	8	1	1
1	1	1	1	10	0	0	0	0	0	9	9	1	1
X	X	X	X	10	1	0	0	0	0	Depends on internal state of counter			
X	X	X	X	10	0	1	0	0	0				
X	X	X	X	10	0	0	1	0	0				
1	X	X	X	10	0	0	0	1	0	H	10	H	L
0	X	X	X	10	0	0	0	1	0	L	H	H	L
X	X	X	X	10	0	0	0	0	1	L	H	L	H

* Output same as the first 16 lines of this truth table (depending on values of A, B, C, D).

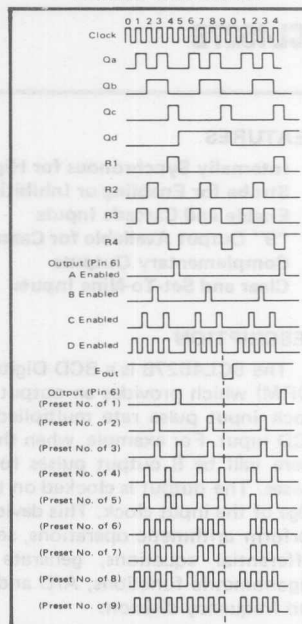
BLOCK DIAGRAM



LOGIC DIAGRAM



TIMING DIAGRAM

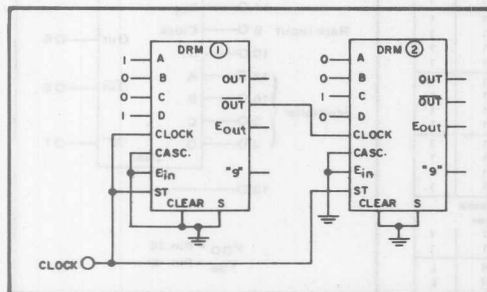


APPLICATIONS INFORMATION

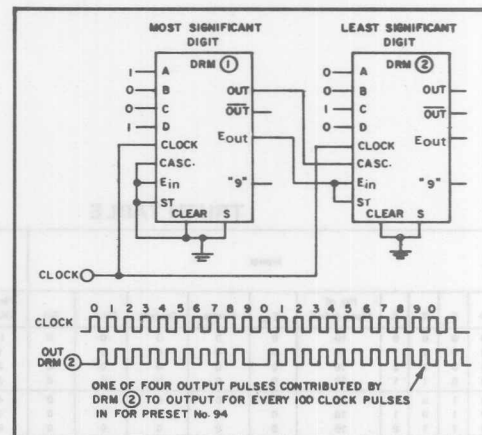
Cascading Connections

For words of more than one digit, SCL4527B devices may be cascaded in two different modes: an Add mode and a Multiply mode.

In the Add mode, some of the gaps left by the more significant unit at the count of 9 are filled in by the less significant units. Output Rate = Clock Rate X (0.1 BCD₁ + 0.01 BCD₂ + ...)



Two SCL4527B's cascaded in the "Multiply" mode with a preset number of 36.



Two SCL4527B's cascaded in the "Add" mode with a preset number of 94.

In the Multiply mode, the fraction programmed into the first DRM is multiplied by the fraction programmed into the second one.

$$\text{Output Rate} = \text{Clock Rate} \times \frac{\text{BCD}_1}{10} \times \frac{\text{BCD}_2}{10} \times \dots$$

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS¹

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	5	—	5	—	0.05	5	—	150	μAdc
		10	—	10	—	0.1	10	—	300	
		15	—	20	—	0.2	20	—	600	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

² T_{LOW} = -55°C for C, D, F, H device.

= -40°C for E device.

T_{HIGH} = +125°C for C, D, F, H device.

= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER	V _{DD} (Vdc)	Min.	Typ.	Max.	Units
CLOCKED OPERATION					
PROPAGATION DELAY TIME	t _{PLH} , t _{PHL}	5	—	150	ns
Clock to Out		10	—	75	150
		15	—	60	120
Clock to Out	5	—	95	190	ns
		10	—	50	100
	15	—	35	70	
Clock to E _{out}	5	—	250	500	ns
		10	—	100	200
	15	—	75	150	
Clock to "g"	5	—	300	600	ns
		10	—	125	250
	15	—	100	200	
Cascade to Out	5	—	95	190	ns
		10	—	50	100
	15	—	35	70	
Strobe to Out	5	—	175	350	ns
		10	—	80	160
	15	—	60	120	
OUTPUT TRANSITION TIME	t _{TLH} , t _{THL}	5	—	130	ns
		10	—	65	130
	15	—	50	100	
MINIMUM CLOCK PULSE WIDTH	PW _{CL}	5	—	165	ns
		10	—	85	170
	15	—	65	130	
MAXIMUM CLOCK FREQUENCY	f _{CL}	5	1.5	3.0	MHz
		10	3.0	6.0	—
	15	4.0	8	—	
MAXIMUM CLOCK RISE AND FALL TIME ¹	t _{rCL} , t _{fCL}	5	15	—	μs
		10	15	—	—
	15	15	—	—	
MINIMUM ENABLE IN SETUP TIME	t _{setup}	5	—	175	ns
		10	—	60	120
	15	—	45	90	
SET OR CLEAR OPERATION					
PROPAGATION DELAY TIME	t _{PLH} , t _{PHL}	5	—	350	ns
		10	—	150	300
	15	—	115	230	
MINIMUM SET OR CLEAR PULSE WIDTH	PW _S , PW _C	5	—	90	ns
		10	—	35	70
	15	—	30	60	
SET OR CLEAR REMOVAL TIME	t _{rem}	5	—	-20	0
		10	—	-10	0
	15	—	-7.5	0	

¹ When units are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the transition times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitive load.

APPLICATIONS INFORMATION

Multiplication of Two Variables

$$R_1 = f_{\text{CLK}} \left(\frac{A}{10} \right)$$

$$R_2 = f_{\text{CLK}} \left(\frac{A}{10} \right) \left(\frac{B}{10} \right) = f_{\text{CLK}} \left(\frac{AB}{100} \right)$$

$$R_3 = f_{CLK} \left(\frac{N}{10} \right)$$

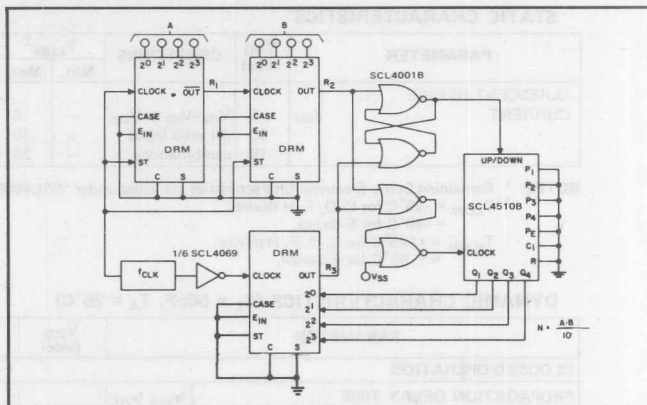
R₂ addresses "up" count, R₃ addresses "down" count. The interface circuit converts to a single clock with mode control. When loop stabilizes,

$$R_2 = R_3$$

$$f_{CLK} \left(\frac{AB}{100} \right) = f_{CLK} \left(\frac{N}{10} \right)$$

$$\text{or } N = \frac{AB}{10}$$

Note: To prevent simultaneous "up" and "down" commands, a multiphase clock input must be used.



Generation of A^{2/3}

$$R_1 = f_{\text{CLK}} \left(\frac{A^2}{100} \right) \left(\frac{1}{10} \right) = f_{\text{CLK}} \left(\frac{A^2}{1000} \right)$$

$$R_2 = f_{CLK} \left(\frac{N^3}{1000} \right)$$

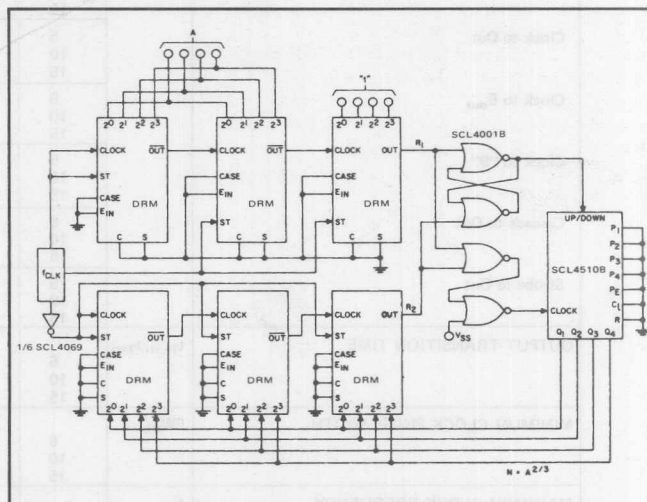
At equilibrium,

$$R_1 = R_2$$

$$N^3 = A^2$$

or $N = A^{2/3}$

Note: To prevent simultaneous "up" and "down" commands, a multiphase clock input must be used.



Frequency Ratios

$$R_1 = f_1/10^n$$

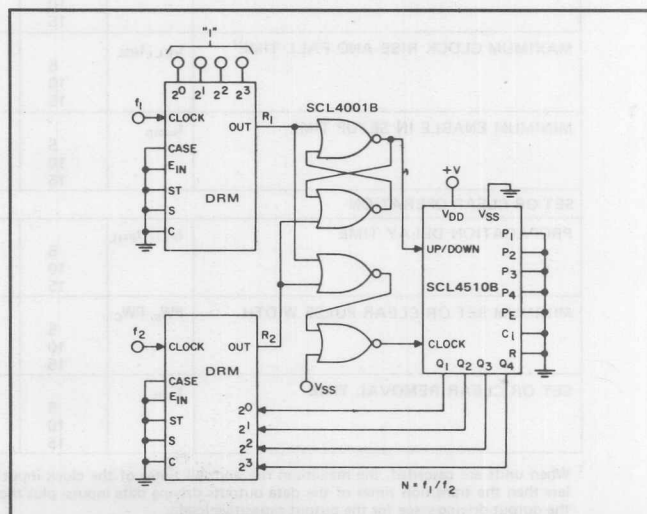
$$R_2 = f_2 N / 10^n \text{ where } n = \text{number of stages}$$

At equilibrium,

$$R_1 = R_2$$

$$N = f_1/f_2$$

Note: To prevent simultaneous commands (overlap), f_1 and f_2 may require preconditioning.





CMOS DUAL MONOSTABLE MULTIVIBRATOR

FEATURES

- ◆ Two Independent Multivibrators on One Chip
- ◆ Triggerable from Leading- or Trailing-Edge Pulse
- ◆ Retriggerable
- ◆ Resettable
- ◆ Q and $\bar{Q}$ Buffered Outputs Available
- ◆ Wide Range of Output Pulse Widths

DESCRIPTION

The SCL4528B Dual Multivibrator provides stable retriggerable/resettable one-shot operation for any fixed-voltage timing application. Timing for the circuit is controlled by an external resistor-capacitor combination (R_X - C_X). Adjustment of these components permits generation of output pulse widths from nanoseconds to minutes. Leading-edge and trailing-edge Trigger inputs are provided, and both positive-going and negative-going pulses are available from complementary outputs.

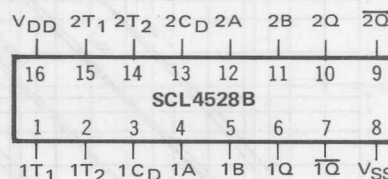
Timing pulses may be terminated at any time by applying a low logic level to the Reset input C_D .

FUNCTION TABLE

INPUTS			OUTPUTS	
C_D	A	B	Q	$\bar{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	↑	H	⌊	⌋
H	L	↓	⌋	⌊

H = High Level (Steady State)
 L = Low Level (Steady State)
 ↑ = Transition, Low-to-High
 ↓ = Transition, High-to-Low
 X = Irrelevant (Inc. Transitions)
 ⌊ = One High-Level Pulse
 ⌋ = One Low-Level Pulse

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

- C 16-pin Cerdip
- D 16-pin Ceramic
- E 16-pin Epoxy
- F 16-pin Flat
- H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

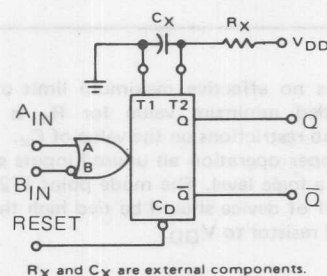
DC Supply Voltage $V_{DD} - V_{SS}$ 3 to 15 Vdc

Operating Temperature T_A

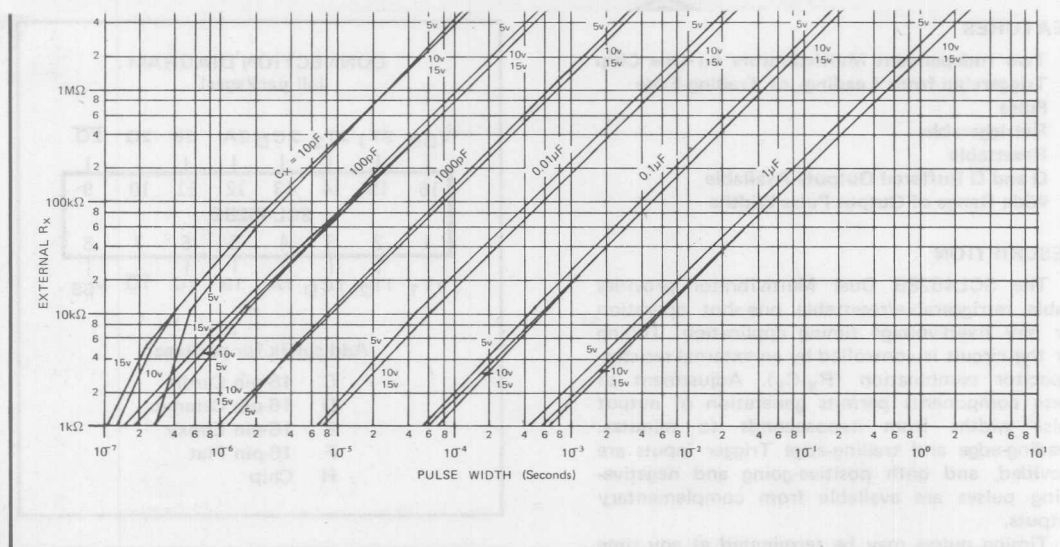
C, D, F, H Device -55 to +125 °C

E Device -40 to +85 °C

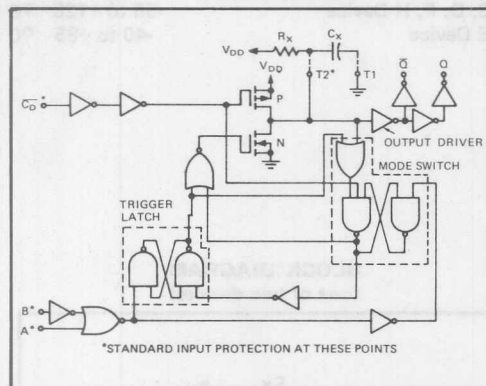
BLOCK DIAGRAM
(one of two devices)



R_X and C_X are external components.



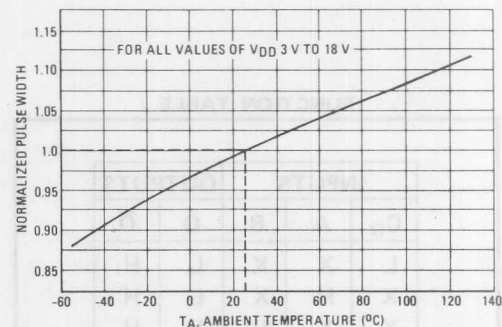
LOGIC DIAGRAM



Notes:

There is no effective maximum limit on R_x ; recommended minimum value for R_x is $1K\Omega$. There are no restrictions on the value of C_x .

For proper operation all unused inputs should be tied to a logic level. The mode point (T2) of a unused half of device should be tied high through an external resistor to V_{DD} .



Normalized Pulse Width versus Temperature

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS¹

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	V _{IN} = V _{SS} or V _{DD} All valid input combinations	—	5	—	0.05	5	—	150	μAdc
			—	10	—	0.1	10	—	300	
			—	20	—	0.2	20	—	600	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

² T_{LOW} = -55°C for C, D, F, H device.

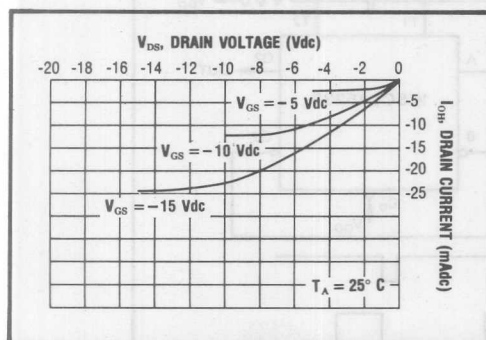
= -40°C for E device.

T_{HIGH} = +125°C for C, D, F, H device.

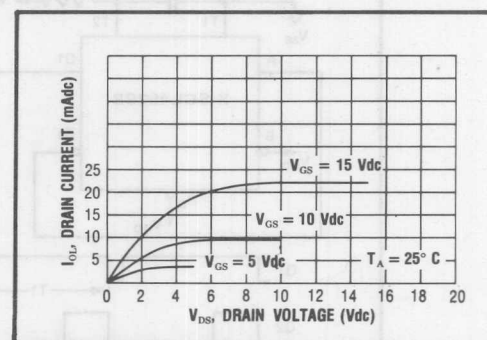
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER	Cx (pF)	Rx (kΩ)	V _{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME From A or B	t _{PLH} , t _{PHL}	15	5	—	270	540	ns
				—	90	180	
				—	70	140	
	1000	10	5	—	510	1020	ns
				—	170	340	
				—	120	240	
From C _D	15	5	5	—	270	540	ns
				—	90	180	
				—	70	140	
	1000	10	5	—	550	1100	ns
				—	300	600	
				—	250	500	
OUTPUT TRANSITION TIME Note: $\bar{Q}$ Output	t _{TLH} , t _{THL}	—	5	—	130	260	ns
				—	65	130	
				—	50	100	
	t _{TLH}	15	5	—	130	260	ns
				—	65	130	
				—	50	100	
MINIMUM INPUT PULSE WIDTH A or B Input	PW _{in}	—	5	—	70	140	ns
				—	30	60	
				—	25	50	
OUTPUT PULSE WIDTH MATCH Same package	1000	10	5	—	± 7.5	±15	%
				—	±10	±20	
				—	±10	±20	
Different packages	1000	10	5	—	—	±50	%
				—	—	±50	
				—	—	±50	

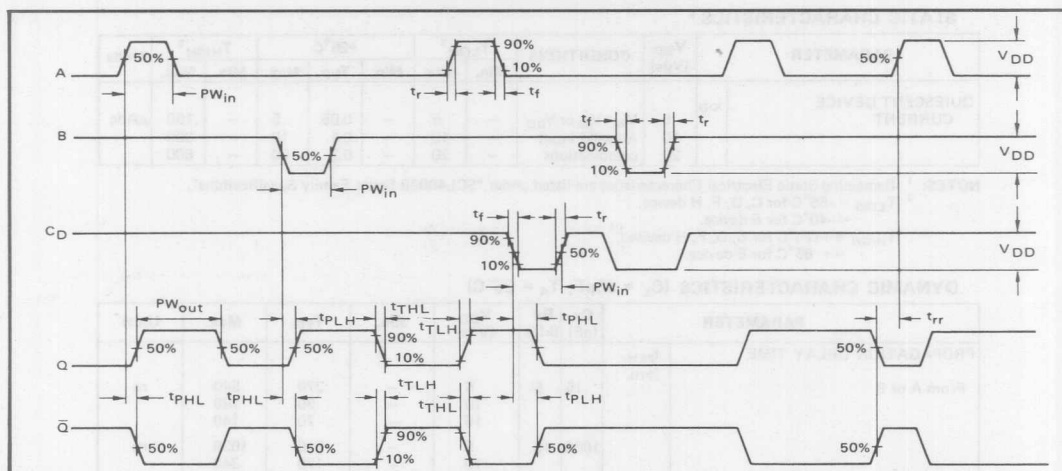


Typical P-Channel
Source Current Characteristics

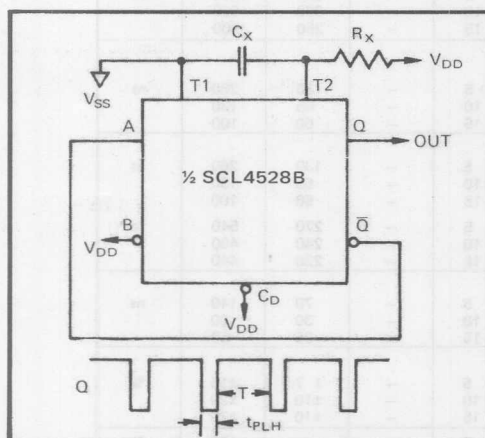


Typical N-Channel
Sink Current Characteristics

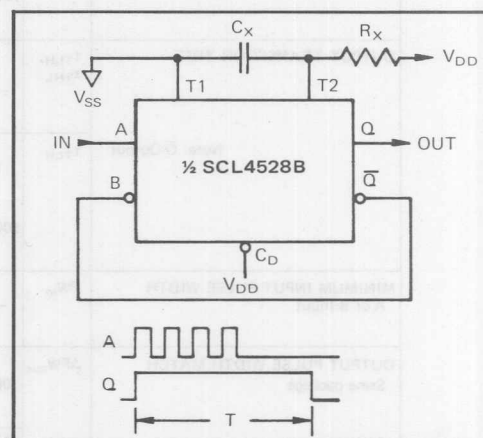
AC TEST WAVEFORMS



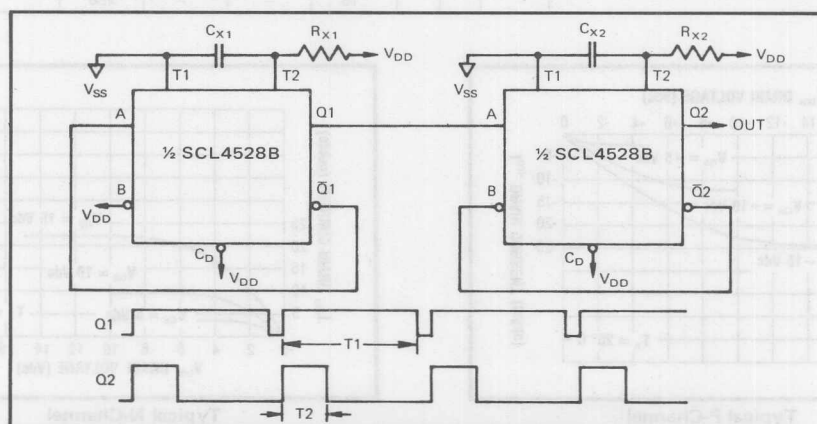
APPLICATIONS INFORMATION



Astable Operation



Connection for Non-Retriggerable Operation



Astable Multivibrator with Adjustable Period and Duty Cycle

SCL4531B



CMOS 12-BIT PARITY TREE

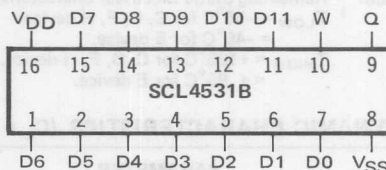
FEATURES

- ◆ Variable Word Length
- ◆ Buffered Output
- ◆ Parity Selection Input

DESCRIPTION

The SCL4531B 12-Bit Parity Tree is constructed with MOS P-channel and N-channel enhancement-mode devices in a single monolithic structure. The circuit consists of 12 Data-bit inputs (D0 thru D11), an even or odd Parity Selection input (W), and an output (Q). The Parity Selection input can be considered as an additional bit. Words of less than 13 bits can generate an even or odd parity output if the remaining inputs are selected to contain an even number of 1's. Words of greater than 12 bits can be accommodated by cascading other SCL4531B devices by using the W input. Applications include checking or including a redundant (parity) bit to a word for error detection/correction systems, controller for remote digital sensors or switches (digital event detection/correction), or as a multiple-input summer without carries.

CONNECTION DIAGRAM (all packages)



Add suffix for package:

- C 16-pin Cerdip
- D 16-pin Ceramic
- E 16-pin Epoxy
- F 16-pin Flat
- H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A	-55 to +125	°C
C, D, F, H Device		-40 to +85	°C
E Device			

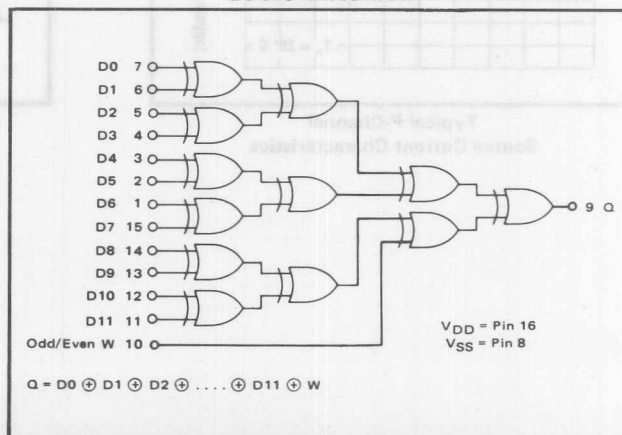
TRUTH TABLE

INPUTS								OUTPUT
W	D11	D10	...	D2	D1	D0	DECIMAL (OCTAL) EQUIVALENT	Q*
0	0	0	...	0	0	0	0 (0)	0
0	0	0	...	0	0	1	1 (1)	1
0	0	0	...	0	1	0	2 (2)	1
0	0	0	...	0	1	1	3 (3)	0
0	0	0	...	1	0	0	4 (4)	1
0	0	0	...	1	0	1	5 (5)	0
0	0	0	...	1	1	0	6 (6)	0
0	0	0	...	1	1	1	7 (7)	1
...	...	...	...	...	...	...	...	...
1	1	1	...	0	0	0	8184 (17770)	0
1	1	1	...	0	0	1	8185 (17771)	1
1	1	1	...	0	1	0	8186 (17772)	1
1	1	1	...	0	1	1	8187 (17773)	0
1	1	1	...	1	0	0	8188 (17774)	1
1	1	1	...	1	0	1	8189 (17775)	0
1	1	1	...	1	1	0	8190 (17776)	0
1	1	1	...	1	1	1	8191 (17777)	1

*0 = Even Parity
1 = Odd Parity

Note: May redefine to suit application by manipulating W and/or other available D's.

LOGIC DIAGRAM



QUIESCENT DEVICE CURRENT	I_{DD}										
	5	$V_{IN} = V_{SS}$ or V_{DD}	—	5	—	0.05	5	—	150	μAdc	
	10	All valid input	—	10	—	0.1	10	—	300		
	15	combinations	—	20	—	0.2	20	—	600		

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

² $T_{LOW} = -55^{\circ}\text{C}$ for C, D, F, H device.

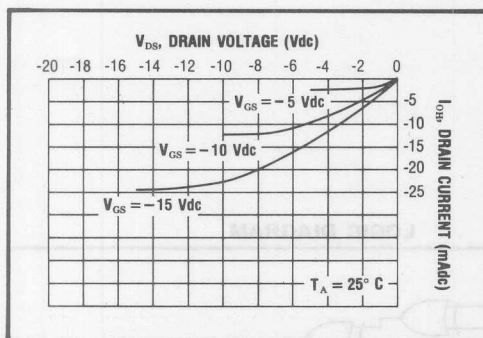
$= -40^{\circ}\text{C}$ for E device.

$T_{HIGH} = +125^{\circ}\text{C}$ for C, D, F, H device.

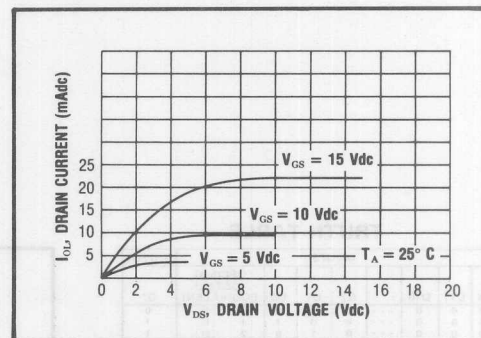
$= +85^{\circ}\text{C}$ for E device.

DYNAMIC CHARACTERISTICS ($C_L = 50\text{pF}$, $T_A = 25^{\circ}\text{C}$)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME From D Inputs	t_{PLH}, t_{PHL}	5	—	420	840	ns
		10	—	175	350	
		15	—	120	240	
	t_{PLH}, t_{PHL}	5	—	250	500	ns
		10	—	100	200	
		15	—	70	140	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	—	130	260	ns
		10	—	65	130	
		15	—	50	100	



Typical P-Channel
Source Current Characteristics



Typical N-Channel
Sink Current Characteristics

SCL4543B Preliminary



BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER

FEATURES

- ◆ Phase Input Signal Reproduced on Outputs for Liquid Crystal Display
- ◆ Latched Storage of Input Code
- ◆ Blanking Input for Display Intensity Modulation
- ◆ Readout Blanking for Illegal Input Combinations
- ◆ Pin Compatible with CD4056A (with Pin 7 Tied to V_{SS})
- ◆ Balanced Output Drive Current Specifications

DESCRIPTION

The SCL4543B BCD-to-7 Segment Latch/Decoder/Driver is designed for use with liquid crystal readouts and is constructed with complementary MOS (CMOS) enhancement-mode devices. The circuit provides the functions of a 4-bit storage latch and a 8421 BCD-to-seven segment decoder and driver. The device has the capability to invert the logic levels of the output combinations. The Phase (Ph), Blanking (BI), and Latch Disable (LD) inputs are used to reverse the truth-table phase, blank the display, and store a BCD code, respectively. For liquid crystal readouts, a square wave is applied to the Ph input of the circuit and the electrically common backplane of the display. The outputs of the circuit are connected directly to the segments of the readout. For other types of readouts, such as light-emitting diode (LED), incandescent, gas discharge, and fluorescent readouts, connection diagrams are given on this data sheet.

Applications include instrument (e.g., counter,

TRUTH TABLE

INPUTS				OUTPUTS						
LD	BI	Ph*	D C B A	a	b	c	d	e	f	g
X	1	0	X X X X	0	0	0	0	0	0	0
1	0	0	0 0 0 0	1	1	1	1	1	1	0
1	0	0	0 0 0 1	0	1	1	0	0	0	0
1	0	0	0 0 1 0	1	1	0	1	0	0	1
1	0	0	0 0 1 1	1	1	1	0	0	0	1
1	0	0	0 1 0 0	0	1	1	0	0	1	1
1	0	0	0 1 0 1	1	0	1	1	0	1	1
1	0	0	0 1 1 0	1	0	1	1	1	1	1
1	0	0	0 1 1 1	1	1	1	0	0	0	0
1	0	0	1 0 0 0	1	1	1	1	1	1	1
1	0	0	1 0 0 1	1	1	1	0	1	1	1
1	0	0	1 0 1 0	0	0	0	0	0	0	0
1	0	0	1 0 1 1	0	0	0	0	0	0	0
1	0	0	1 1 0 0	0	0	0	0	0	0	0
1	0	0	1 1 0 1	0	0	0	0	0	0	0
1	0	0	1 1 1 0	0	0	0	0	0	0	0
1	0	0	1 1 1 1	0	0	0	0	0	0	0
0	0	0	X X X X	**	**	**	**	**	**	**
t	t	t	t	Inverse of Output Combinations Above						Display as above

X = Don't care

t = Above Combinations

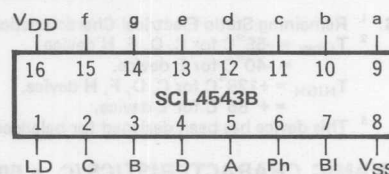
* = For liquid crystal readouts, apply a square wave to Ph.

For common cathode LED readouts, select Ph = 0.

For common anode LED readouts, select Ph = 1.

** = Depends upon the BCD code previously applied when LD = 1.

CONNECTION DIAGRAM (all packages)



Add suffix for package:

- C 16-pin Cerdip
- D 16-pin Ceramic
- E 16-pin Epoxy
- F 16-pin Flat
- H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage $V_{DD} - V_{SS}$ 3 to 15 Vdc

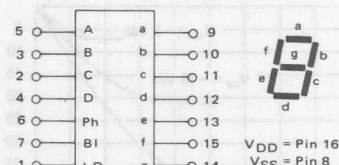
Operating Temperature T_A

C, D, F, H Device -55 to +125 °C

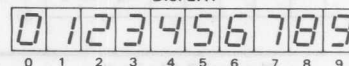
E Device -40 to +85 °C

DVM, etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

BLOCK DIAGRAM



DISPLAY



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS^{1,3}

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	V _{IN} = V _{SS} or V _{DD} All valid input combinations	—	5	—	0.05	5	—	150	μA _{dc}
			—	10	—	0.1	10	—	300	
			—	15	—	0.2	15	—	600	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

² T_{LOW} = -55°C for C, D, F, H device.

= -40°C for E device.

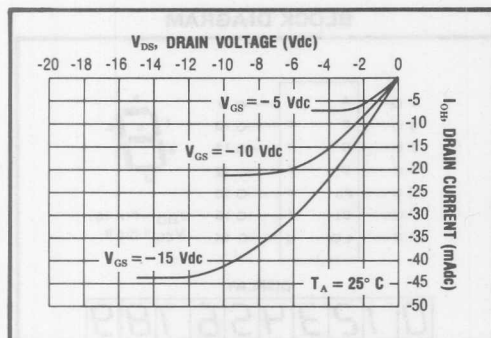
T_{HIGH} = +125°C for C, D, F, H device.

= + 85°C for E device.

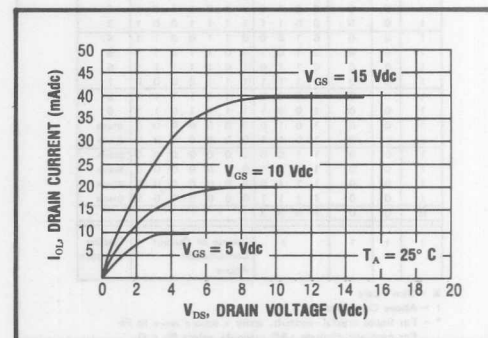
³ This device has been designed for balanced output drive current specifications. Consult Family Specifications.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V _{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME	t _{PLH} , t _{PHL}	5	—	550	1100	ns
		10	—	210	420	
		15	—	160	320	
OUTPUT TRANSITION TIME	t _{TLH} , t _{THL}	5	—	100	200	ns
		10	—	50	100	
		15	—	40	80	
MINIMUM DATA INPUT SETUP TIME	t _{setup}	5	—	-40	0	ns
		10	—	-15	0	
		15	—	-10	0	
MINIMUM DATA INPUT HOLD TIME	t _{hold}	5	—	40	80	ns
		10	—	15	30	
		15	—	10	20	
MINIMUM LD PULSE WIDTH	PW _{LD}	5	—	125	250	ns
		10	—	50	100	
		15	—	40	80	

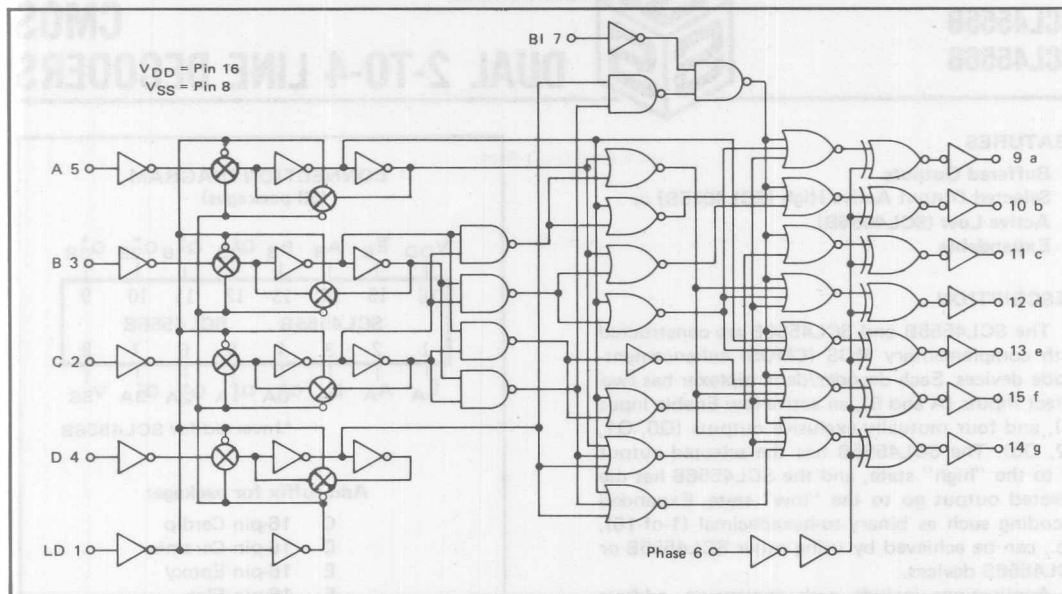


Typical P-Channel
Source Current Characteristics



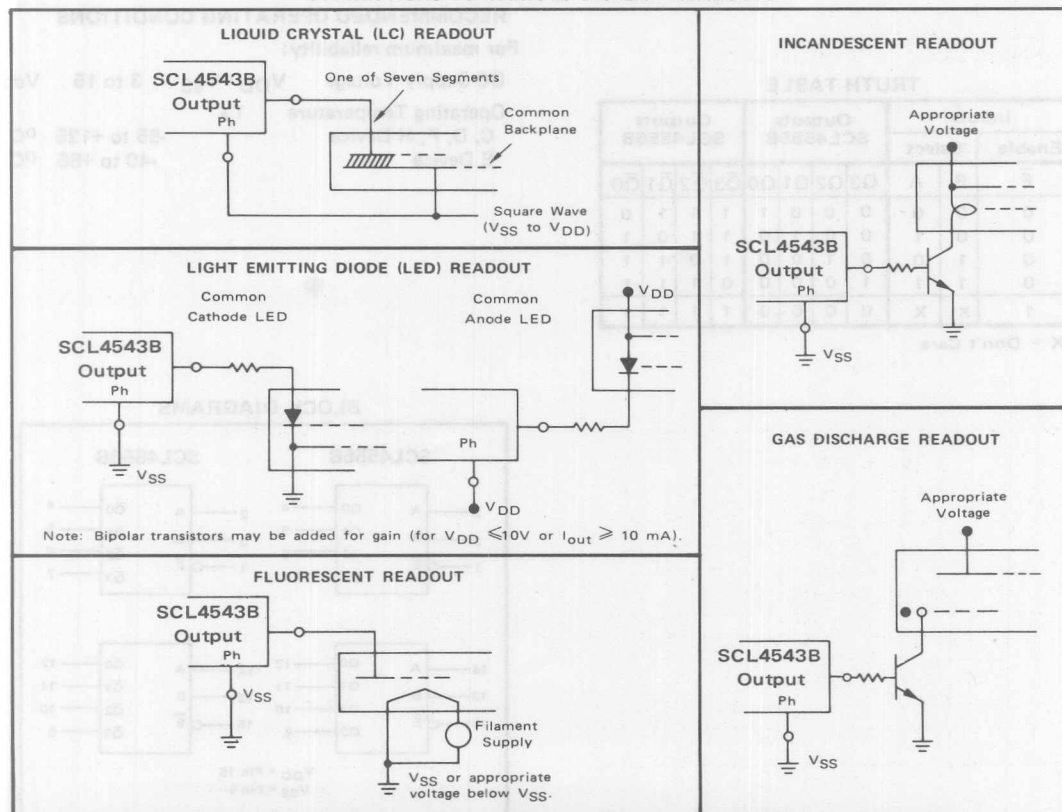
Typical N-Channel
Sink Current Characteristics

LOGIC DIAGRAM



APPLICATIONS INFORMATION

CONNECTIONS TO VARIOUS DISPLAY READOUTS



SCL4555B SCL4556B



CMOS DUAL 2-TO-4 LINE DECODERS

FEATURES

- ◆ Buffered Outputs
- ◆ Selected Output Active High (SCL4555B) or Active Low (SCL4556B)
- ◆ Expandable

DESCRIPTION

The SCL4555B and SCL4556B are constructed with complementary MOS (CMOS) enhancement-mode devices. Each decoder/demultiplexer has two Select inputs (A and B), an active-low Enable input (E), and four mutually-exclusive outputs (Q0, Q1, Q2, Q3). The SCL4555B has the selected output go to the "high" state, and the SCL4556B has the selected output go to the "low" state. Expanded decoding such as binary-to-hexadecimal (1-of-16), etc., can be achieved by using other SCL4555B or SCL4556B devices.

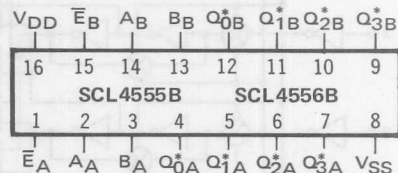
Applications include code conversion, address decoding, memory selection control, and demultiplexing (using the Enable input as a data input) in digital data transmission systems.

TRUTH TABLE

Inputs			Outputs SCL4555B				Outputs SCL4556B			
Enable	Select		Q3	Q2	Q1	Q0	$\bar{Q}3$	$\bar{Q}2$	$\bar{Q}1$	$\bar{Q}0$
$\bar{E}$	B	A								
0	0	0	0	0	0	1	1	1	1	0
0	0	1	0	0	1	0	1	1	0	1
0	1	0	0	1	0	0	1	0	1	1
0	1	1	1	0	0	0	0	1	1	1
1	X	X	0	0	0	0	1	1	1	1

X = Don't Care

CONNECTION DIAGRAM (all packages)



*Inverted for SCL4556B

Add suffix for package:

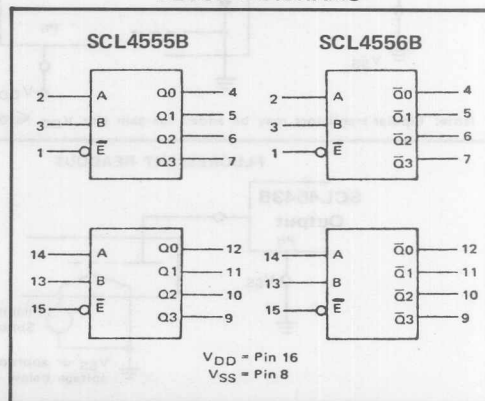
- C 16-pin Cerdip
- D 16-pin Ceramic
- E 16-pin Epoxy
- F 16-pin Flat
- H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A	-55 to +125	°C
C, D, F, H Device		-40 to +85	°C
E Device			

BLOCK DIAGRAMS



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS¹

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C		T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	
QUIESCENT DEVICE CURRENT	I _{DD}	V _{IN} = V _{SS} or V _{DD} All valid inputs combinations	—	5	—	0.05	5	—	μAdc
			—	10	—	0.1	10	—	
			—	20	—	0.2	20	—	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

² T_{LOW} = -55°C for C, D, F, H device.

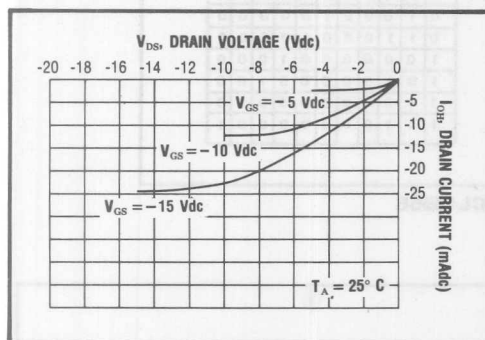
= -40°C for E device.

T_{HIGH} = +125°C for C, D, F, H device.

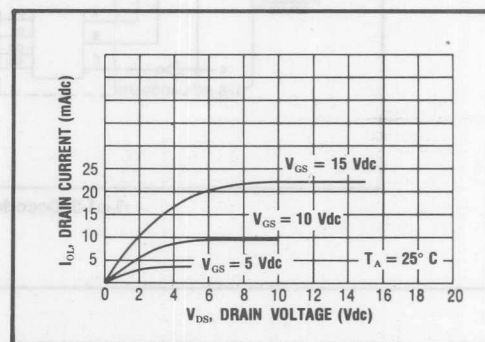
= +85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER	V _{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME SCL4555B	t _{PLH} , t _{PHL}	—	—	—	ns
	5	—	140	280	
	10	—	65	130	
SCL4556B	t _{PLH} , t _{PHL}	—	—	—	ns
	5	—	160	320	
	10	—	75	150	
OUTPUT TRANSITION TIME	t _{TLH} , t _{THL}	—	—	—	ns
	5	—	130	260	
	10	—	65	130	
	15	—	50	100	

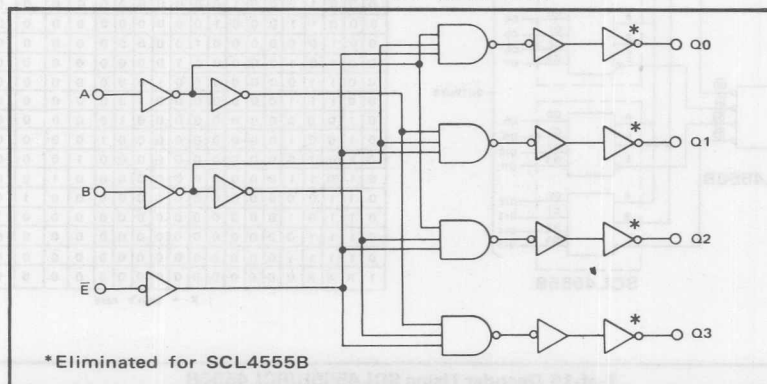


Typical P-Channel
Source Current Characteristics

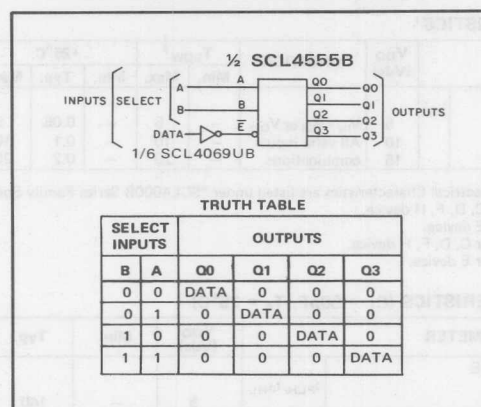


Typical N-Channel
Sink Current Characteristics

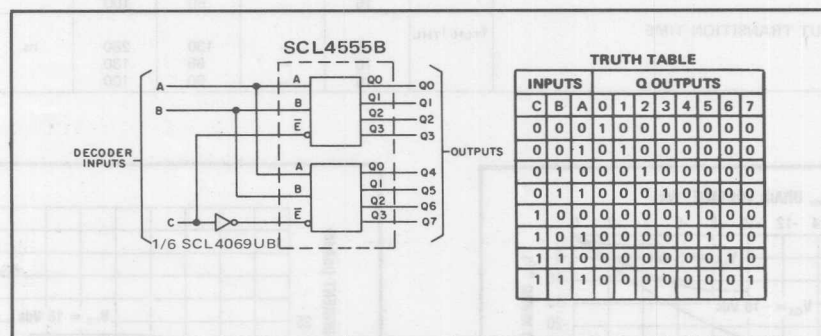
LOGIC DIAGRAM (½ of Dual)



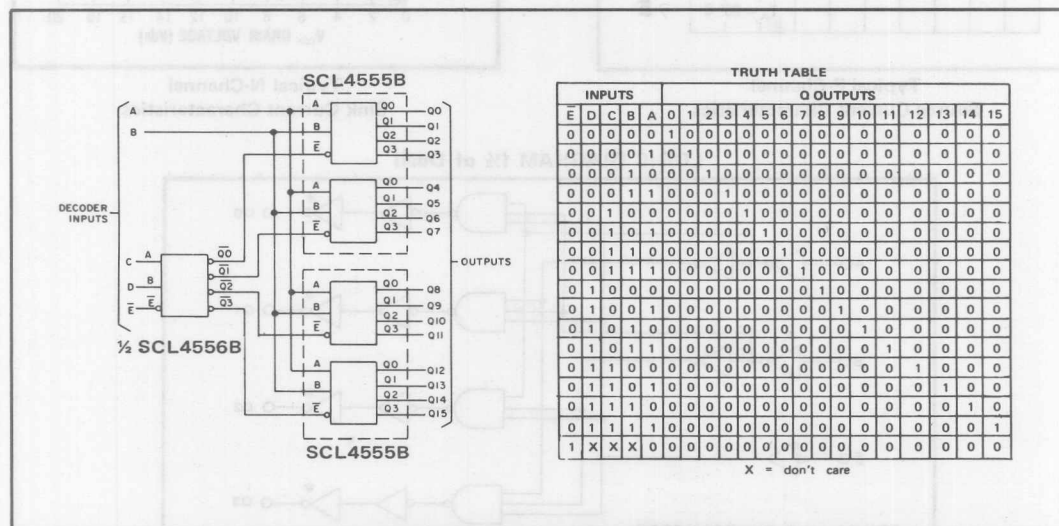
APPLICATIONS INFORMATION



1-of-4 Line Data Demultiplexer Using SCL4555B



1-of-8 Decoder Using SCL4555B



1-of-16 Decoder Using SCL4555B/SCL4556B



CMOS 4-BIT ARITHMETIC LOGIC UNIT

FEATURES

- ◆ Function and Pinout Equivalent to 74181
- ◆ Provides 16 Logic Functions and 16 Arithmetic Functions
- ◆ Comparator Function
- ◆ Positive or Negative Logic
- ◆ Full Look-Ahead for High-Speed Operations on Long Words

DESCRIPTION

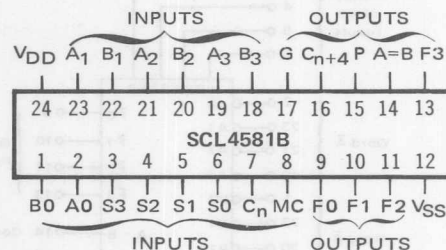
The SCL4581B is a CMOS 4-Bit Arithmetic Logic Unit (ALU) capable of providing 16 functions of two Boolean variables and 16 binary arithmetic operations on two 4-bit words. The level of the Mode Control input determines whether the output function is logic or arithmetic. The desired logic function is selected by applying the appropriate binary word to the Select inputs (S0 thru S3) with the Mode Control input high, while the desired arithmetic operation is selected by applying a low voltage to the Mode Control input, the required level to Carry in, and the appropriate word to the Select inputs. The Word inputs and Function outputs can be operated with either active-high or active-low data.

Carry propagate (P) and Carry generate (G) outputs are provided to allow a full look-ahead carry scheme for fast simultaneous carry generation for the four bits in the package. Fast arithmetic operations on long words are obtainable by using the SCL4582B as a second-order look-ahead block. An inverted Ripple-Carry input (C_n) and a Ripple-Carry output (C_{n+4}) are included for ripple-through operation.

ALU SIGNAL DESIGNATIONS

Designation	Pin Nos.	Function
A3, A2, A1, A0	19, 21, 23, 2	Word A Inputs
B3, B2, B1, B0	18, 20, 22, 1	Word B Inputs
S3, S2, S1, S0	3, 4, 5, 6	Function-Select Inputs
C_n	7	Inv. Carry Input
MC	8	Mode Control Input
F3, F2, F1, F0	13, 11, 10, 9	Function Outputs
A = B	14	Comparator Output
P	15	Carry Propagate Output
C_{n+4}	16	Inv. Carry Output
G	17	Carry Generate Output

CONNECTION DIAGRAM (all packages)



Add suffix for package:

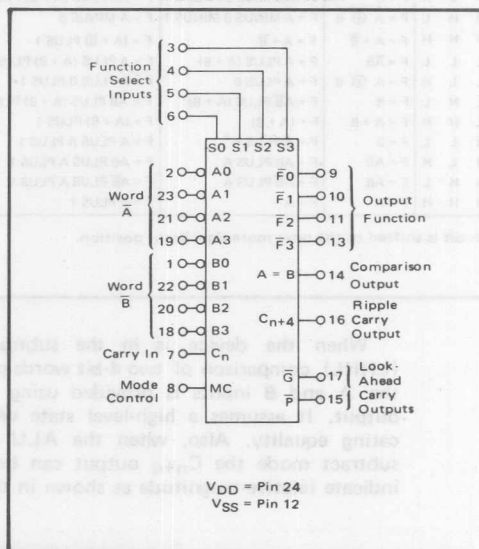
- D 24-pin Ceramic
- E 24-pin Epoxy
- H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A	-55 to +125	°C
D, H Device		-40 to +85	°C
E Device			

BLOCK DIAGRAM



ALU FUNCTION GENERATION

The SCL4581B can be used with the signal designations of either Figure 1 or Figure 2.

The logic functions and arithmetic operations obtained with signal designations as in Figure 1 are given in Table 1; those obtained with the signal designations of Figure 2 are given in Table 2.

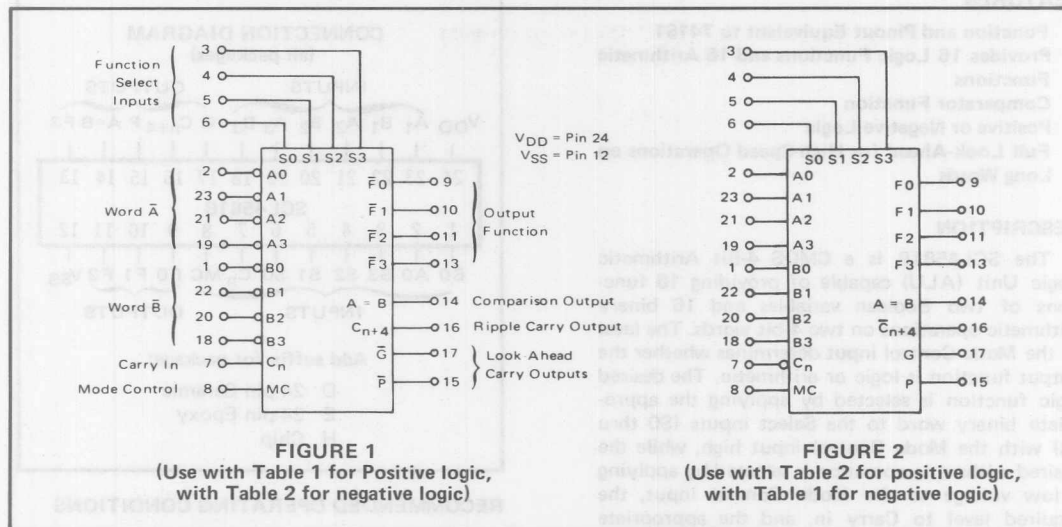


TABLE 1

SELECTION S3 S2 S1 S0	ACTIVE-LOW DATA	
	MC = H	MC = L; ARITHMETIC OPERATIONS
	LOGIC FUNCTIONS	C _n = L (no carry) C _n = H (with carry)
L L L L	F = $\bar{A}$	F = A MINUS 1 F = A
L L L H	F = $\bar{A}\bar{B}$	F = AB MINUS 1 F = AB
L L H L	F = $\bar{A} + B$	F = $\bar{A}\bar{B}$ MINUS 1 F = $\bar{A}\bar{B}$
L L H H	F = 1	F = MINUS 1 (2's COMPL) F = ZERO
L H L L	F = $\bar{A} + \bar{B}$	F = A PLUS (A + $\bar{B}$) F = A PLUS (A + $\bar{B}$) PLUS 1
L H L H	F = $\bar{B}$	F = AB PLUS (A + $\bar{B}$) F = AB PLUS (A + $\bar{B}$) PLUS 1
L H H L	F = A $\oplus$ B	F = A MINUS B MINUS 1 F = A MINUS B
L H H H	F = A + $\bar{B}$	F = A + $\bar{B}$ F = (A + $\bar{B}$) PLUS 1
H L L L	F = $\bar{A}\bar{B}$	F = A PLUS (A + B) F = A PLUS (A + B) PLUS 1
H L L H	F = A $\oplus$ B	F = A PLUS B F = A PLUS B PLUS 1
H L H L	F = B	F = $\bar{A}\bar{B}$ PLUS (A + B) F = $\bar{A}\bar{B}$ PLUS (A + B) PLUS 1
H L H H	F = A + B	F = (A + B) F = (A + B) PLUS 1
H H L L	F = 0	F = A PLUS A* F = A PLUS A PLUS 1
H H L H	F = $\bar{A}\bar{B}$	F = AB PLUS A F = AB PLUS A PLUS 1
H H H L	F = AB	F = $\bar{A}\bar{B}$ PLUS A F = $\bar{A}\bar{B}$ PLUS A PLUS 1
H H H H	F = A	F = A F = A PLUS 1

TABLE 2

SELECTION S3 S2 S1 S0	ACTIVE-HIGH DATA	
	MC = H	MC = L; ARITHMETIC OPERATIONS
	LOGIC FUNCTIONS	C _n = H (no carry) C _n = L (with carry)
L L L L	F = $\bar{A}$	F = A
L L L H	F = $\bar{A} + \bar{B}$	F = A + B
L L H L	F = $\bar{A}\bar{B}$	F = A + $\bar{B}$
L L H H	F = 0	F = MINUS 1 (2's COMPL)
L H L L	F = $\bar{A}\bar{B}$	F = A PLUS $\bar{A}\bar{B}$
L H L H	F = $\bar{B}$	F = (A + B) PLUS $\bar{A}\bar{B}$
L H H L	F = A $\oplus$ B	F = A MINUS B MINUS 1
L H H H	F = $\bar{A}\bar{B}$	F = $\bar{A}\bar{B}$ MINUS 1
H L L L	F = $\bar{A} + B$	F = A PLUS AB
H L L H	F = A $\oplus$ B	F = A PLUS B
H L H L	F = B	F = (A + $\bar{B}$) PLUS AB
H L H H	F = AB	F = AB MINUS 1
H H L L	F = 1	F = A PLUS A*
H H L H	F = A + $\bar{B}$	F = (A + B) PLUS A
H H H L	F = A + B	F = (A + $\bar{B}$) PLUS A
H H H H	F = A	F = A MINUS 1

* Each bit is shifted to the next more significant position.

When the device is in the subtract mode (LHHL), comparison of two 4-bit words present at the A and B inputs is provided using the A=B output. It assumes a high-level state when indicating equality. Also, when the ALU is in the subtract mode the C_n+4 output can be used to indicate relative magnitude as shown in this table:

Data Level	C _n	C _n + 4	Magnitude
Active High	H	H	A ≤ B
	L	H	A < B
Active Low	H	L	A > B
	L	L	A ≥ B

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS¹

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	5 V _{IN} = V _{GS} or V _{DD}	—	5	—	0.05	5	—	150	μAdc
		10 All valid input combinations	—	10	—	0.1	10	—	300	
		15	—	20	—	0.2	20	—	600	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

² T_{LOW} = -55°C for D, H device.

= -40°C for E device.

T_{HIGH} = +125°C for D, H device.

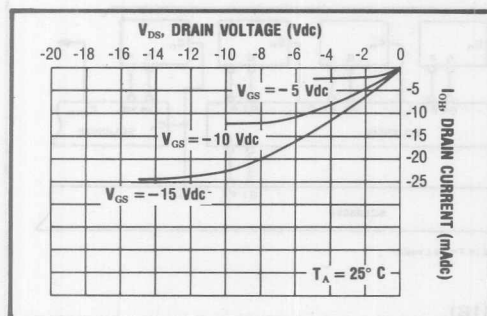
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

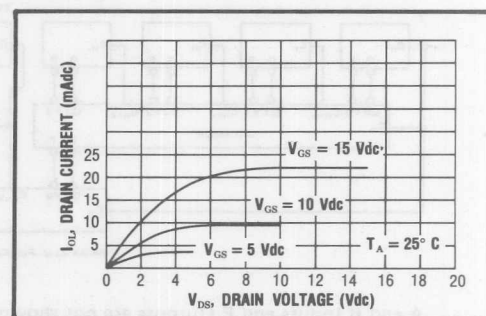
PARAMETER	V _{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME	t _{PLH} , t _{PHL}				
Sum In to Sum Out	5	—	525	1050	ns
	10	—	185	370	
	15	—	135	270	
Sum In to Sum Out (Logic Mode)	5	—	500	1000	ns
	10	—	175	350	
	15	—	135	270	
Sum In to A = B	5	—	750	1500	ns
	10	—	250	500	
	15	—	185	370	
Sum In to $\bar{P}$ or $\bar{G}$	5	—	365	730	ns
	10	—	135	270	
	15	—	95	190	
Sum In to C _{n+4}	5	—	500	1000	ns
	10	—	175	350	
	15	—	130	260	
Carry In to Sum Out	5	—	285	570	ns
	10	—	110	220	
	15	—	80	160	
Carry In to C _{n+4}	5	—	230	460	ns
	10	—	90	180	
	15	—	65	130	
OUTPUT TRANSITION TIME	t _{TLH} , t _{THL}				
	5	—	130	260	ns
	10	—	65	130	
	15	—	50	100	

AC Test Setup Reference Table

TEST	AC PATHS		DC DATA INPUTS		MODE
	INPUTS	OUTPUTS	TO V _{SS}	TO V _{DD}	
Sum _{in} to Sum _{out} Delay Time	$\bar{A}0$	Any $\bar{F}$	Remaining $\bar{A}$'s C _n	All $\bar{B}$'s	Add
Sum _{in} to $\bar{P}$ Delay Time	$\bar{A}0$	$\bar{P}$	Remaining $\bar{A}$'s C _n	All $\bar{B}$'s	Add
Sum _{in} to $\bar{G}$ Delay Time	$\bar{B}0$	C _{n+y}	All $\bar{A}$'s C _n	Remaining $\bar{B}$'s	Add
Sum _{in} to C _{n+4} Delay Time	$\bar{B}0$	$\bar{G}$	All $\bar{A}$'s C _n	Remaining $\bar{B}$'s	Add
C _n to Sum _{out} Delay Time	C _n	Any $\bar{F}$	All $\bar{A}$'s	All $\bar{B}$'s	Add
C _n to C _{n+4} Delay Time	C _n	C _{n+4}	All $\bar{A}$'s	All $\bar{B}$'s	Add
Sum _{in} to A = B Delay Time	$\bar{A}0$	A = B	All $\bar{B}$'s Remaining $\bar{A}$'s	C _n	Sub
Sum _{in} to Sum _{out} Delay Time (Logic Mode)	All $\bar{B}$'s	Any $\bar{F}$	All $\bar{A}$'s	M	Exclusive OR



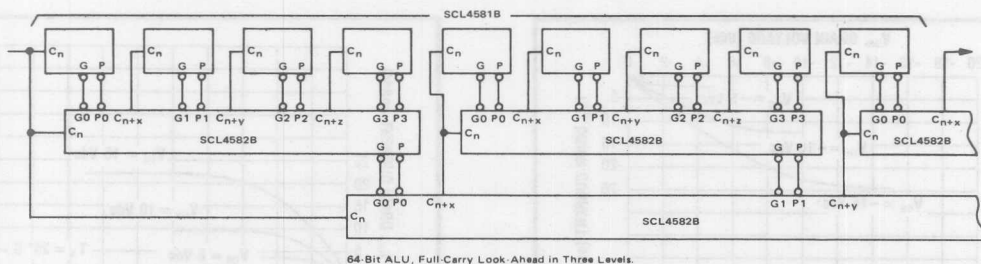
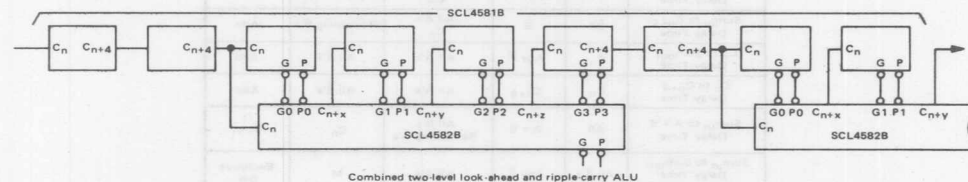
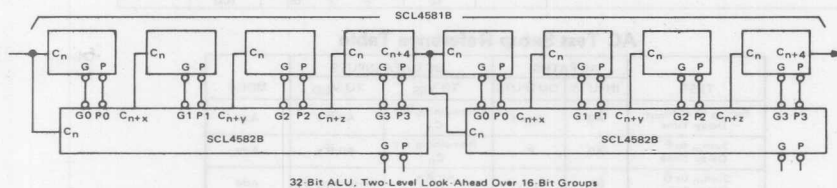
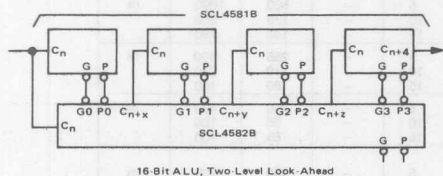
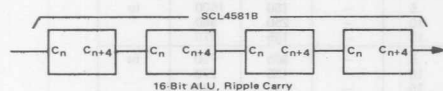
Typical P-Channel
Source Current Characteristics



Typical N-Channel
Sink Current Characteristics

Of Bits	Arithmetic Logic Units	Look-Ahead Carry Generators	Between ALU's
1 to 4	1		None
5 to 8	2		Ripple
9 to 16	3 or 4	1	Full Look-Ahead
17 to 64	5 to 16	2 to 5	Full Look-Ahead

EXPANSION TECHNIQUES



A and B Inputs and F Outputs are not shown (SCL4581B).



CMOS LOOK-AHEAD CARRY BLOCK

FEATURES

- ◆ Expandable to any Number of Bits
- ◆ High-Speed Operation
- ◆ Directly Compatible with SCL4581B ALU

DESCRIPTION

The SCL4582B is a high-speed, Look-Ahead Carry Generator capable of anticipating a carry across four binary adders or group of adders. It is cascadable to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided.

When used in conjunction with the SCL4581B Arithmetic Logic Unit (ALU), these generators provide high-speed carry look-ahead capability for any word length. Each SCL4582B generates the look-ahead (anticipated carry) across a group of four ALU's and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n-bits.

Carry input and output of the SCL4581B ALU are in their true form and the carry propagate (P) and carry generate (G) are in negated form; therefore, the carry functions (inputs, outputs, generate, and propagate) of the look-ahead generators are implemented in the compatible forms for direct connections to the ALU. Reinterpretations of carry functions as explained on the SCL4581B data sheet are also applicable to and compatible with the look-ahead generator.

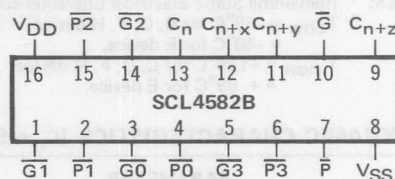
PIN DESIGNATIONS

DESIGNATION	PIN NO's	FUNCTION
$\overline{G_0}, \overline{G_1}, \overline{G_2}, \overline{G_3}$	3, 1, 14, 5	Active-Low Carry-Generate Inputs
$\overline{P_0}, \overline{P_1}, \overline{P_2}, \overline{P_3}$	4, 2, 15, 6	Active-Low Carry-Propagate Inputs
C_n	13	Carry Input
$C_{n+x}, C_{n+y}, C_{n+z}$	12, 11, 9	Carry Outputs
$\overline{G}$	10	Active-Low Group Carry-Generate Output
$\overline{P}$	7	Active-Low Group Carry-Propagate Output

LOGIC EQUATIONS

$$\begin{aligned}
 C_{n+x} &= G_0 + P_0 \cdot C_n \\
 C_{n+y} &= G_1 + P_1 \cdot G_0 + P_1 \cdot P_0 \cdot C_n \\
 C_{n+z} &= G_2 + P_2 \cdot G_1 + P_2 \cdot P_1 \cdot G_0 + P_2 \cdot P_1 \cdot P_0 \cdot C_n \\
 \overline{G} &= G_3 + P_3 \cdot G_2 + P_3 \cdot P_2 \cdot G_1 + P_3 \cdot P_2 \cdot P_1 \cdot G_0 \\
 \overline{P} &= P_3 \cdot P_2 \cdot P_1 \cdot P_0
 \end{aligned}$$

CONNECTION DIAGRAM (all packages)



Add suffix for package:

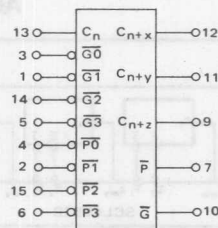
- C 16-pin Cerdip
- D 16-pin Ceramic
- E 16-pin Epoxy
- F 16-pin Flat
- H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A	-55 to +125	°C
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

BLOCK DIAGRAM



V_{DD} = Pin 16
 V_{SS} = Pin 8

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS¹

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	V _{IN} = V _{SS} or V _{DD} All valid input combinations	—	5	—	0.05	5	—	150	μAdc
			—	10	—	0.1	10	—	300	
			—	20	—	0.2	20	—	600	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

² T_{LOW} = -55°C for C, D, F, H device.

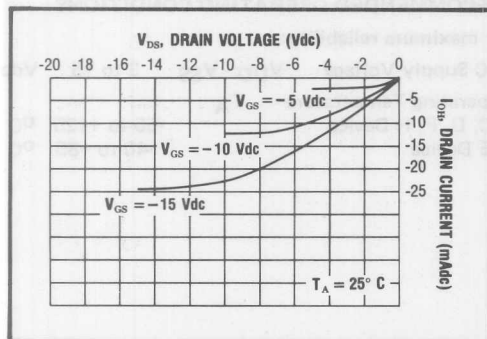
= -40°C for E device.

T_{HIGH} = +125°C for C, D, F, H device.

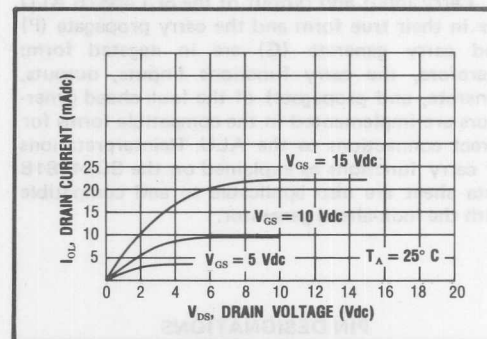
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V _{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME	t _{PLH} , t _{PHL}	5	—	175	350	ns
		10	—	85	170	
		15	—	65	130	
OUTPUT TRANSITION TIME	t _{TLH} , t _{THL}	5	—	130	260	ns
		10	—	65	130	
		15	—	50	100	

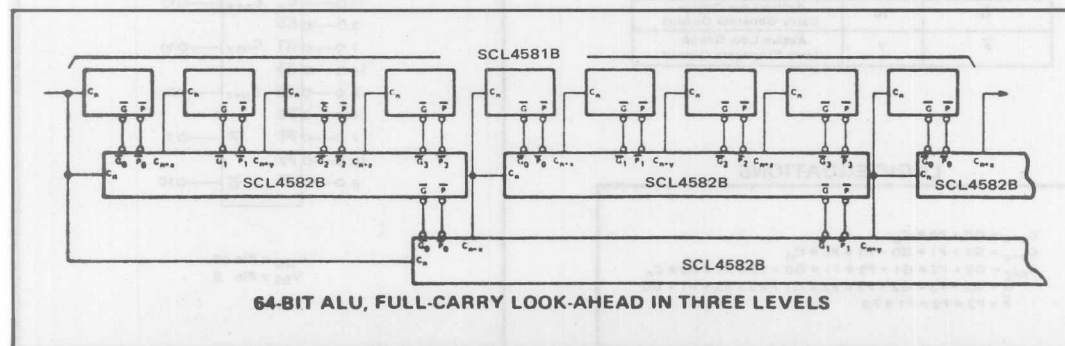


Typical P-Channel
Source Current Characteristics



Typical N-Channel
Sink Current Characteristics

APPLICATIONS INFORMATION





CMOS 4-BIT MAGNITUDE COMPARATOR

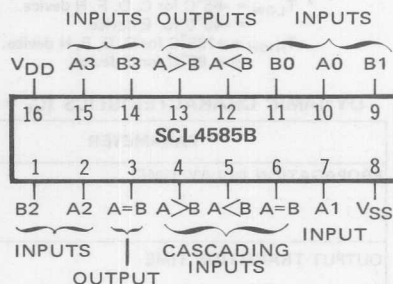
FEATURES

- ◆ Binary or BCD Comparison
- ◆ Expandable
- ◆ $A < B$, $A = B$, $A > B$ Outputs Available

DESCRIPTION

This 4-Bit Magnitude Comparator performs comparison of straight binary and straight BCD (84-2-1) codes. Three decisions about two 4-bit words (A, B) are made and are externally available at three outputs. These devices are fully expandable to any number of bits without external gates. Words of greater length may be compared by connecting comparators in cascade. The $A < B$ and $A = B$ outputs of a stage handling less-significant bits are connected to the corresponding $A < B$ and $A = B$ inputs of the next stage handling more-significant bits. The $A > B$ cascading input is connected to a high level. The stage handling the least-significant bits must have a high-level voltage applied to the $A = B$ and $A > B$ inputs. An alternate method of cascading which reduces the comparison time is shown under Applications Information.

CONNECTION DIAGRAM (all packages)



Add suffix for package:

- C 16-pin Cerdip
- D 16-pin Ceramic
- E 16-pin Epoxy
- F 16-pin Flat
- H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

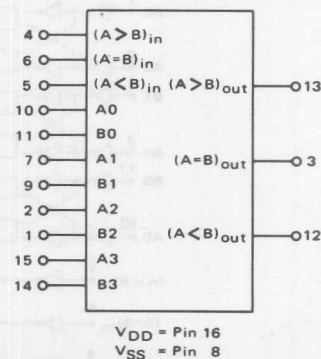
DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A	-55 to +125	°C
C, D, F, H Device		-40 to +85	°C
E Device			

TRUTH TABLE

Inputs				Cascading			Outputs		
Comparing				$A < B$	$A = B$	$A > B$	$A < B$	$A = B$	$A > B$
A3, B3	A2, B2	A1, B1	A0, B0						
A3 > B3	X	X	X	X	X	1	0	0	1
A3 = B3	A2 > B2	X	X	X	X	1	0	0	1
A3 = B3	A2 = B2	A1 > B1	X	X	X	1	0	0	1
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	1	0	0	1
A3 = B3	A2 = B2	A1 = B1	A0 = B0	0	0	1	0	0	1
A3 = B3	A2 = B2	A1 = B1	A0 = B0	0	1	1	0	1	0
A3 = B3	A2 = B2	A1 = B1	A0 = B0	1	0	1	1	0	0
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	1	0	0
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	1	0	0
A3 = B3	A2 < B2	X	X	X	X	X	1	0	0
A3 < B3	X	X	X	X	X	X	1	0	0
X	X	X	X	X	X	0	-	-	0

X = Don't Care

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS¹

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	V _{IN} =V _{SS} or V _{DD} All valid input combinations	—	5	—	0.05	5	—	150	μAdc
			—	10	—	0.1	10	—	300	
			—	20	—	0.2	20	—	600	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

² T_{LOW} = -55°C for C, D, F, H device.

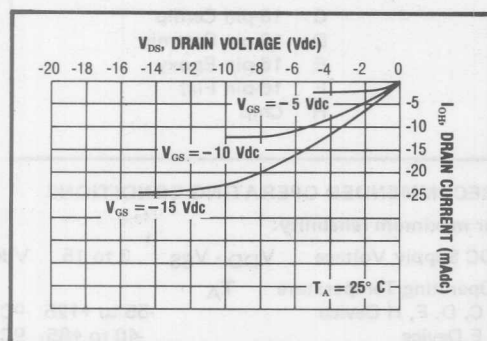
= -40°C for E device.

T_{HIGH} = +125°C for C, D, F, H device.

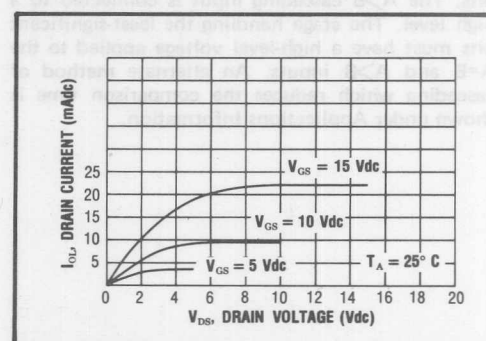
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER	V _{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME	t _{PLH} , t _{PHL}	5	—	300	ns
		10	—	125	
		15	—	90	
		—	—	—	
OUTPUT TRANSITION TIME	t _{TLH} , t _{THL}	5	—	130	ns
		10	—	65	
		15	—	50	
		—	—	—	

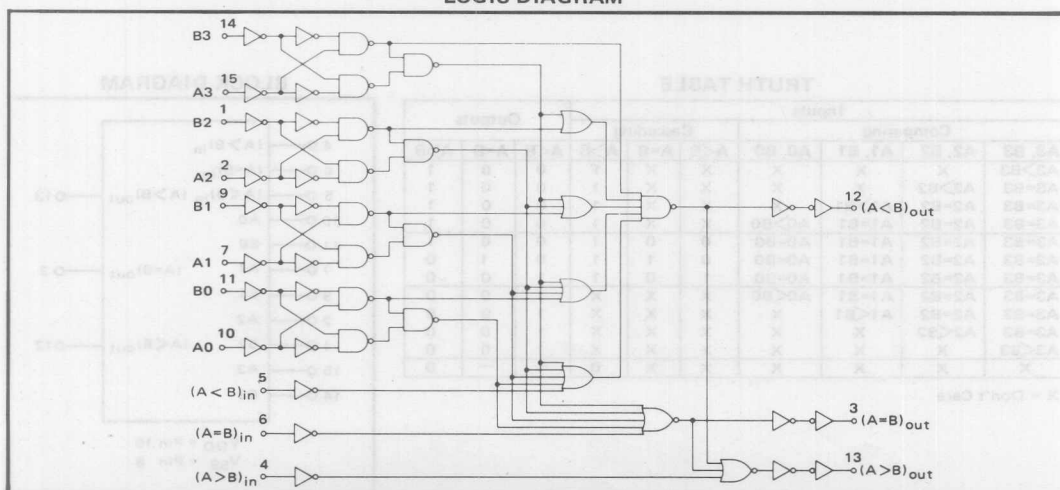


Typical P-Channel
Source Current Characteristics



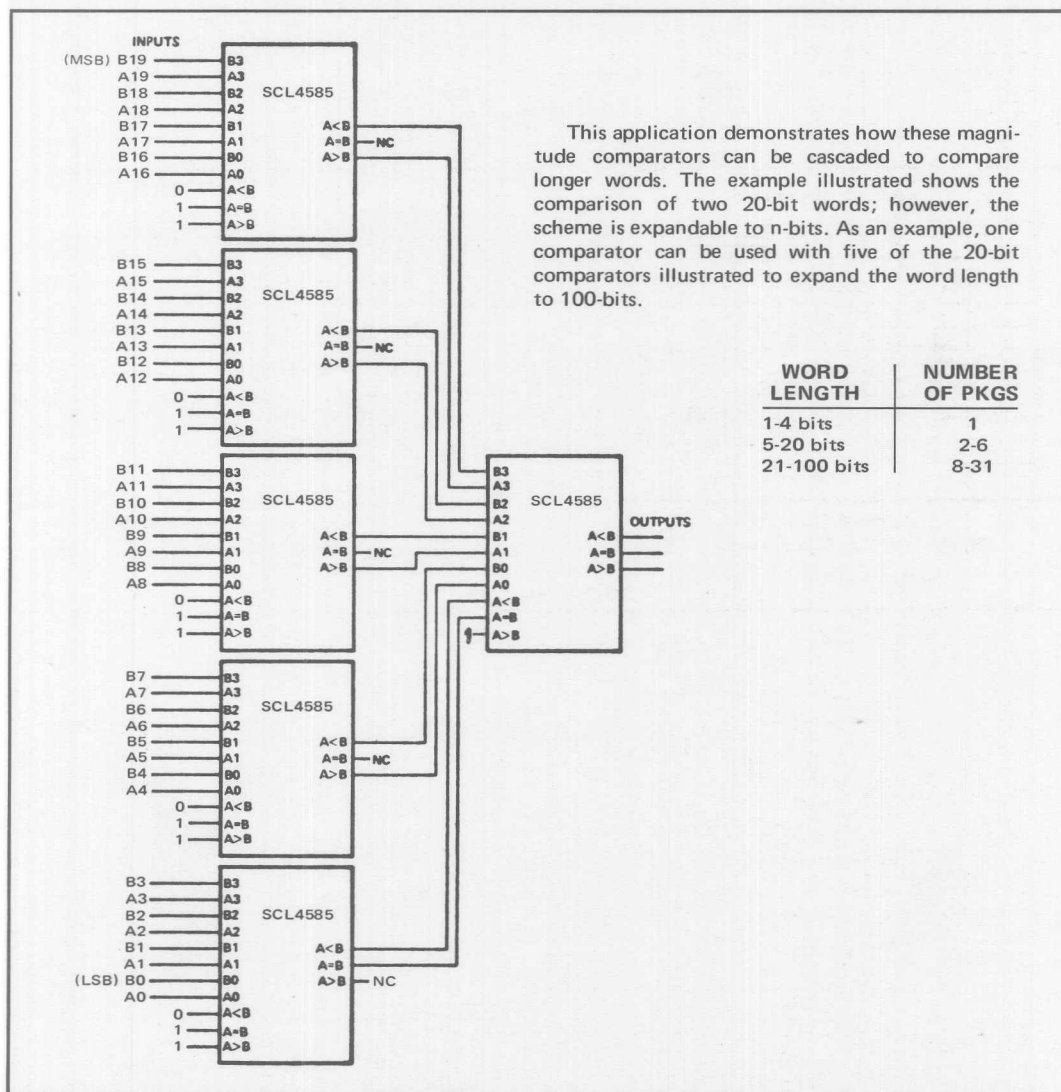
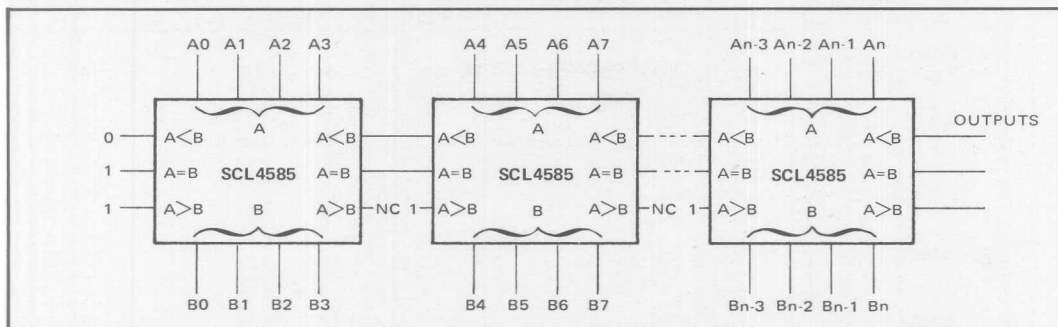
Typical N-Channel
Sink Current Characteristics

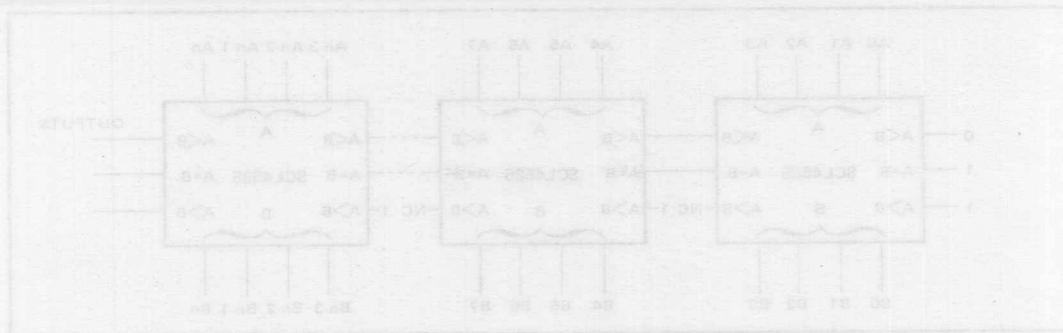
LOGIC DIAGRAM



APPLICATIONS INFORMATION

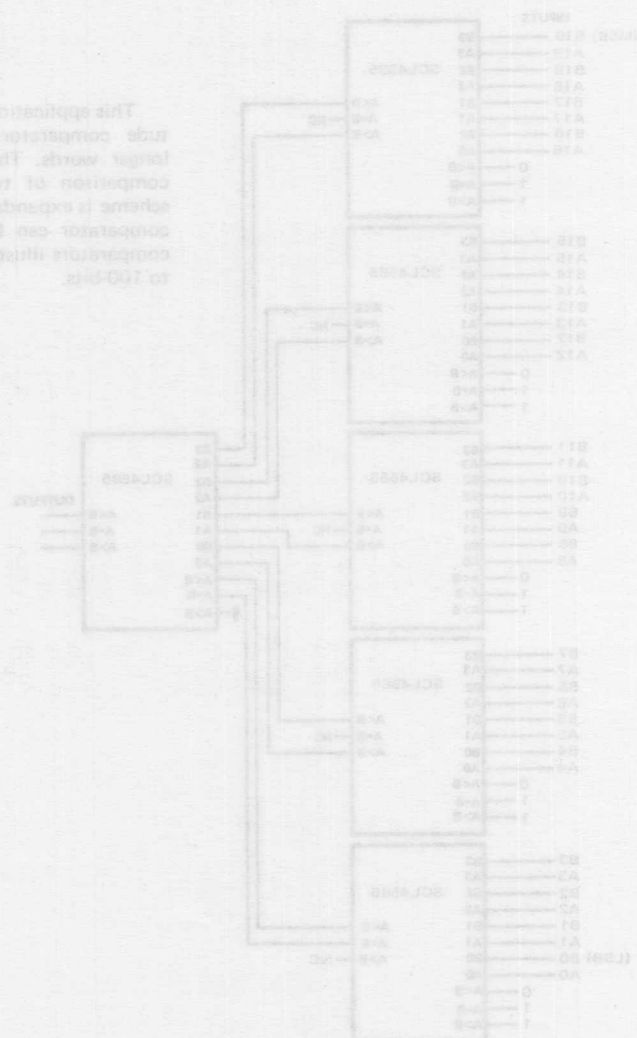
COMPARISON OF TWO N-BIT WORDS

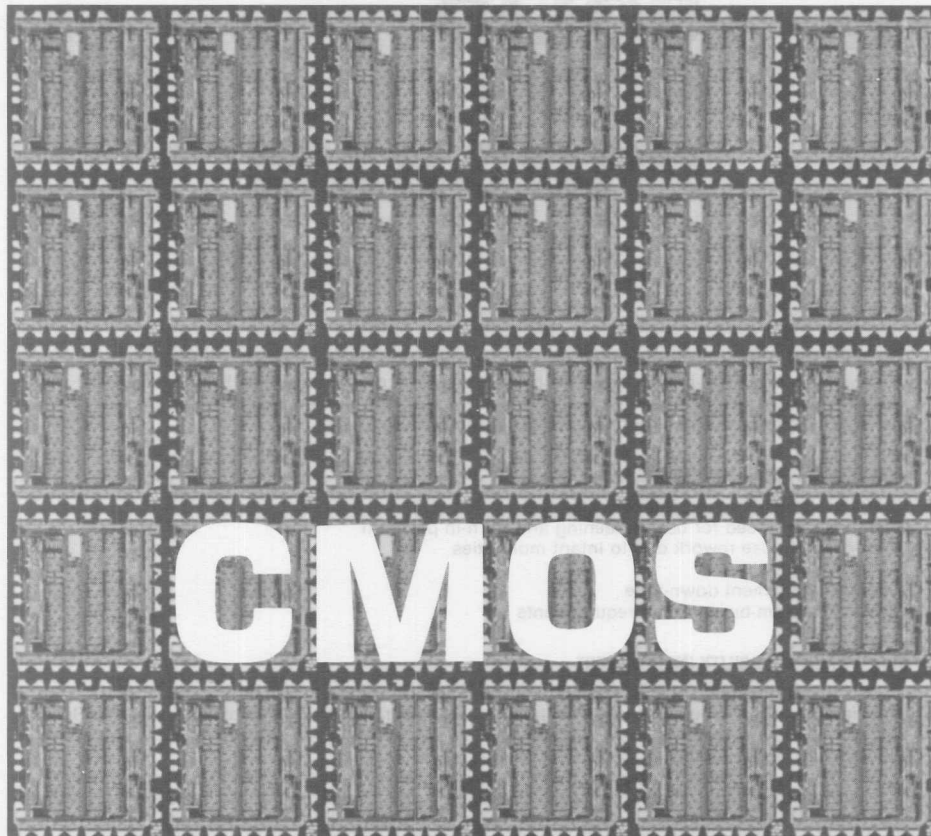




This application demonstrates how three magnitude comparators can be cascaded to compare longer words. The example illustrated shows the comparison of two 20-bit words; however, the scheme is expandable to n-bits. As an example, one comparator can be used with five of the 20-bit comparators illustrated to expand the word length to 100-bits.

WORD LENGTH	NUMBER OF PACKS
1-4 bits	1
5-20 bits	2-5
21-100 bits	5-11



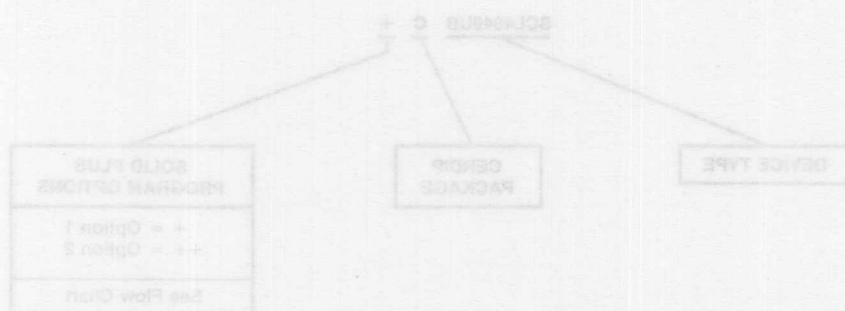


CMOS

Solid Plus, therefore, means both higher quality and higher reliability to the user. This combination of stress and double testing was the first such screening program offered to the CMOS user. For further information, ask for a copy of Brochure SP-5, "Solid Plus CMOS".

AVAILABILITY
All devices
distributed

RELIABILITY PROGRAMS





SOLID PLUS PROGRAM

The Solid Plus Program is a series of screening procedures offered by Solid State Scientific on its cerdip-packaged CMOS line to assure the highest degree of quality and reliability to commercial and industrial users. The options available allow the user the choice of selecting the program which offers the maximum reliability/cost quotient for his particular application.

WHAT SOLID PLUS DOES FOR THE USER

- *Simplifies incoming inspection
- *Eliminates the need for user screening and burn-in program
- *Reduces in-house rework due to infant mortalities
- *Reduces field failures
- *Reduces equipment down-time
- *Reduces system burn-in time requirements

QUALITY AND RELIABILITY IMPROVEMENT

Every production lot of integrated circuits contains a small number of devices which survive the usual test procedures, but, for a variety of reasons, will fail prematurely when placed in service. Solid Plus pre-screening removes these "infant mortalities" at the factory; the tight AQL guarantees substantially higher quality on Solid Plus devices.

Reliability, as opposed to quality, refers to how well a device which is initially good will withstand its environment. While reliability cannot be tested into a device, the stress tests of Solid Plus accelerate the time to failure of weak parts. Because these stress tests cause weak parts to fail prior to shipment, the population received by the user will actually demonstrate higher reliability in use.

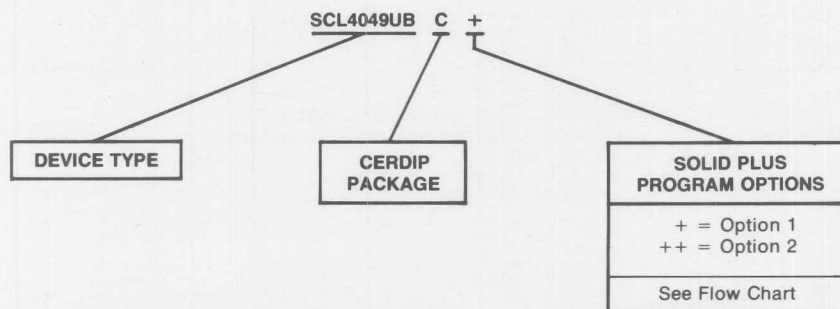
Solid Plus, therefore, means both higher quality and higher reliability to the user. This combination of stress and double testing was the first such screening program offered to the CMOS user.

For further information, ask for a copy of Brochure SP-2, "Solid Plus CMOS".

AVAILABILITY

All devices in the Solid Plus SCL4000 Series are available from local Solid State Scientific distributors.

NOMENCLATURE



SOLID PLUS PROGRAM OPTIONS

SOLID +

VISUAL INSPECTIONS:
Chip, Precap
Per MIL-STD-883

MIL-STD-883 Class B Visual Inspections ensure cosmetic integrity, bond integrity, and freedom from foreign materials.

ENCAPSULATION:
Frit-Seal Ceramic (Cerdip)
Package

The low-cost, high-reliability frit-seal ceramic (cerdip) package is used for Solid Plus devices. (For more information, ask for a copy of the latest Reliability Report.)

STABILIZATION BAKE:
24 hrs. @ 200°C

This long-term high-temperature stress helps eliminate marginal bonds and electrical connections.

TEMPERATURE CYCLING
-65/+150°C, 10 Cycles

Exercising the circuits over this 215°C temperature range further stresses bonds, and generally eliminates those missed during the bake.

GROSS LEAK TEST

FINE LEAK TEST

These tests are hermeticity screens to verify seal integrity. 100% Gross Leak - MIL-STD-883 Method 1014 Cond. C. Sample Fine Leak - MIL-STD-883 Method 1014 Cond. A

CENTRIFUGE

Centrifuge test is done on a sample basis to MIL-STD-883 Method 2001 Condition E. This mechanically stresses package seal, bonding wires, and die attach.

SOLID ++

VISUAL INSPECTIONS:
Chip, Precap
Per MIL-STD-883

ENCAPSULATION:
Frit-Seal Ceramic (Cerdip)
Package

STABILIZATION BAKE:
24 hrs. @ 200°C

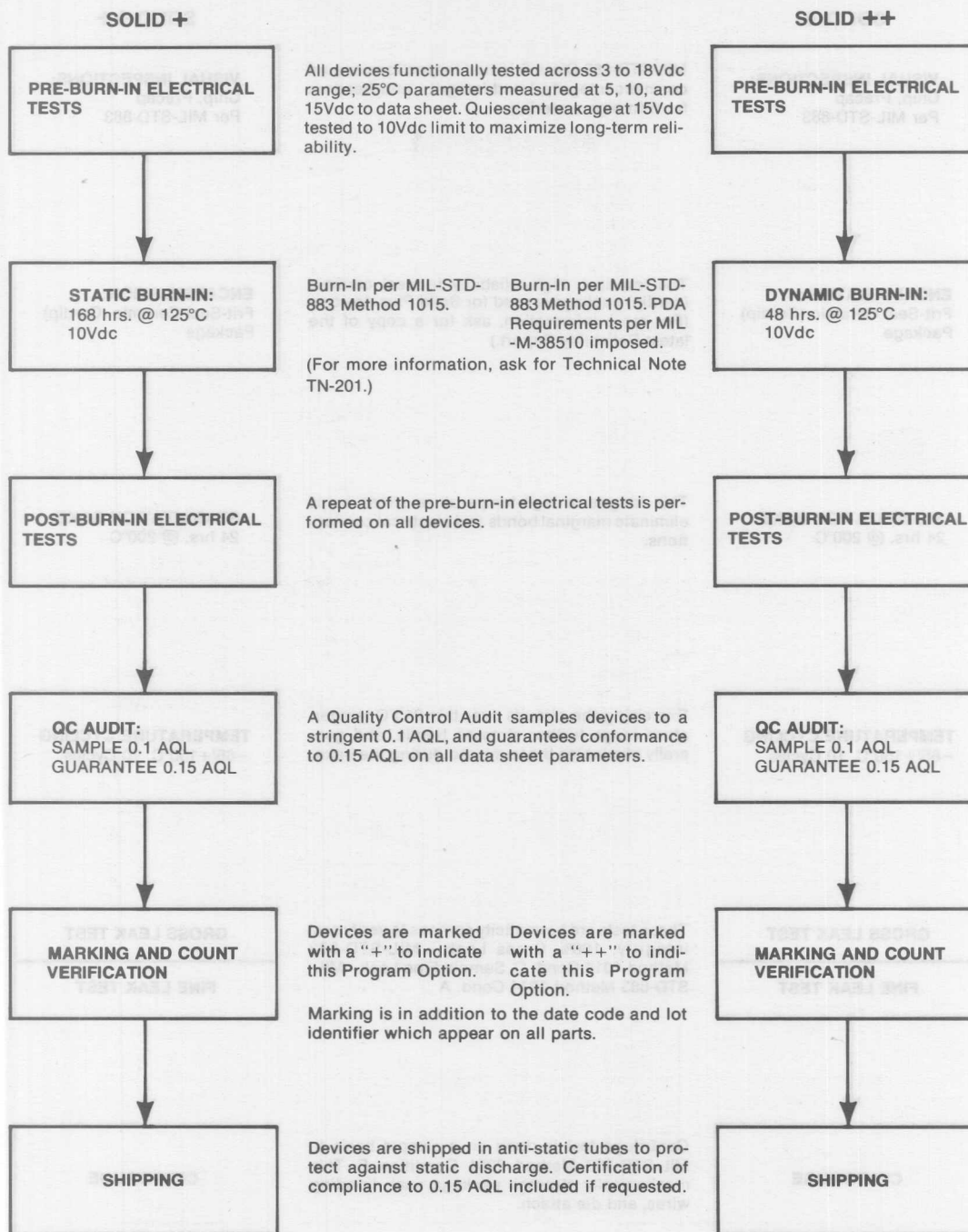
TEMPERATURE CYCLING
-65/+150°C, 10 Cycles

GROSS LEAK TEST

FINE LEAK TEST

CENTRIFUGE

SOLID PLUS PROGRAM OPTIONS (Continued)



HIGH RELIABILITY CMOS

Solid State Scientific offers as part of its standard product line devices which meet various levels of reliability screening requirements. Devices ordered to these requirements meet the need of improved reliability in the military market. Programs adhere to the following military specifications:

A. MIL-M-38510	General Specification for Microcircuits
B. MIL-STD-883	Test Methods and Procedures for Microelectronics
C. MIL-STD-19500	General Specification for Semiconductor Devices
D. MIL-I-45208	Inspection System Requirements
E. MIL-M-55565	Packaging of Microcircuits
F. MIL-STD-1313	Microelectronics Terms and Definitions
G. MIL-Q-9858A	Quality Program Requirements
H. Internal QRA	Specifications

The complete line of SCL4000 Series Devices is available processed and screened in full accordance with MIL-STD-883. The table lists the test conditions and methods applicable to Class A, Class B, and Class C level screening.

Class A devices are intended for applications where maintenance or replacement is extremely difficult or impossible and where reliability is imperative. Typical programs include aerospace and missile applications.

Class B screening is intended for systems where replacement can be performed but is difficult and expensive. Applications include airborne electronics and medical instrumentation.

Class C screened devices are intended for military and industrial applications where replacement can be readily accomplished. Such applications as ground-based communications fall into this category.

Test ¹	Description	MIL-STD-883		Class		
		Method	Condition	A	B	C
SEM Inspection ²	When specified ⁴			X		
Internal Visual ²	Maximum Visual Criteria	2010	A	X		
	Optimum Visual Criteria	2010	B		X	X
Stabilization Bake	24 hrs. min. @150° C min	1008	C	X	X	X
Temperature Cycling	10 cycles, -65/+150° C	1010	C	X	X	X
Constant Acceleration (Centrifuge)	30,000 G's, min Y ₁ plane	2001	E	X	X	X
Seal: Fine Gross	Helium, 5 x 10 ⁻⁸ cc/sec FC78 Vacuum/Pressure FC43 Hot 10 ⁻³ cc/sec	1014	A	X	X	X
		1014	C2	X	X	X
Serialization				X		
Pre-Burn-In Electricals	Per applicable device specification: Read and Record As specified			X		X
Burn-In Test	240 hrs @ 125° C min 160 hrs @ 125° C min	1015		X		
		1015			X	
Post-Burn-In Electricals	Per applicable device specification: Read and Record As specified			X		X
Reverse Bias Burn In	When specified: 72 hrs @ 150° C min	1015	A or C	X		
Post-Reverse Bias Burn-In Electricals	Per applicable device specification: Read and Record			X		

Test ¹	Description	MIL-STD-883		Class		
		Method	Condition	A	B	C
Seal: Fine Gross	Helium, 5×10^{-6} cc/sec FC78 Vacuum/Pressure FC43 Hot 10^{-5} cc/sec	1014 1014	A C2	X ³ X ³		
Final Electrical Test	Per applicable device specification: 25° C static parameters -55/+125° C static parameters 25° C Dynamic and Switching parameters 25° C Functional Test			X X X X	X X X X	X X
Radiographic Inspection	2 views; inspect at 6X - 25X mag.	2012		X		
Qualification or Quality Conform- ance Inspection	Group A, B, C, D as applicable	5005		X	X	X
External Visual	3X - 10X mag: configuration, lead structure, marking, workmanship	2009		X	X	X

- Notes: 1. All tests are 100% screens.
2. These tests apply to packaged devices and chips; remaining tests apply only to packaged devices.
3. Optional test
4. SEM Inspection is done on a monthly basis as part of routine process monitoring.

DEVICE NOMENCLATURE

